INTRODUCTION

Digital low-dropout (D-LDO) regulators are used in portable devices, biomedical devices, and internet-of-things applications [1–10] because of their lower supply-voltage, small power-transistors, stability, and compatible processes. However, D-LDO features a long settling time and a ringing problem while settling the output voltage at large load transitions.

Several D-LDOs have been developed to reduce settling time [2–12] and D-LDOs with proportional-integral (PI) control removed the ringing. These devices used a level-crossing ADC with numerous reference voltages [2] and a delay line ADC with an analog voltage-to-current converter [3]. In [4], a steady-state load current (SLC) estimator was used to reduce ringing but required analog voltage-to-time and time-to-digital converters. Moreover, the PI control and SLC estimator were complex because they required an additional mathematical operator. Successive approximation register (SAR)-type D-LDO [5] improved the transient response with a binary PMOS array and removed ringing by using a proportional-derivative (PD) compensator. However, when the load current is significantly changed, the PD compensator increases or decreases the PMOS array current to match the load current. Here \( V_{OUT} \) reaches a minimum or maximum voltage, resulting in a long settling time. Coarse-fine D-LDOs [6,7] reduced the settling time using a large PMOS array and a high clock frequency in a coarse control loop, but exhibited large ringing in the transient state. In [6], a coarse-fine D-LDO reduced the ringing by using a current-mirror flash analog-to-digital converter and reference changer, but showed a slow transient response. In [7], the coarse-fine
D-LDO improved the transient response by using the peak detector to trigger coarse mode. The D-LDO turns a large PMOS transistor on or off at a fast clock cycle. However, this process causes a large ringing, which continuously re-triggers coarse mode and degrades stability. To prevent the large ringing, the coarse-fine D-LDO requires a guard time, the maximum possible settling time, to reactivate fine mode and stop the coarse mode, thereby increasing the overall time needed. In [8], the D-LDO reduces the transient response time by using a variable-gain accumulator, but exhibited a large undershoot voltage. Herein, a newly proposed coarse-fine D-LDO removes the ringing and reduces settling time by adding an auxiliary power stage. The novel device achieved a low output ripple voltage by using a comparator with a complete comparison signal. Section 2 describes the architecture of the proposed coarse-fine D-LDO and Section 3 shows the measurement results from the fabricated chip with the conclusions presented in Section 4.

2 | ARCHITECTURE

2.1 | Proposed coarse-fine digital low-dropout regulator

Figure 1 shows a conventional D-LDO consisting of a comparator, bidirectional shift-register, and PMOS array. The comparator compares the output voltage ($V_{OUT}$) with the reference voltage ($V_{REF}$). The bidirectional shift-register turns the PMOS transistor on or off in the PMOS array per clock cycle according to the comparator output, resulting in the regulation of $V_{OUT}$ to $V_{REF}$ by the D-LDO. When the load current ($I_{LOAD}$) is changed from light to heavy, as shown in Figure 1B, a large undershoot voltage is generated and the PMOS array output current ($I_{OUT}$) is increased. When $V_{OUT}$ is minimized at time $T_1$, $I_{OUT}$ is equal to $I_{LOAD}$. However, $I_{OUT}$ increases continuously because $V_{OUT}$ remained lower than $V_{REF}$. When $V_{OUT}$ is equal to $V_{REF}$ at time $T_2$, $I_{OUT}$ became almost two times that of $I_{LOAD}$. Therefore, $V_{OUT}$ increases continuously and an unwanted large overshoot voltage was generated. As a result, unwanted overshoot and undershoot voltages were generated until $V_{OUT}$ settled to $V_{REF}$ at time $T_3$, generating ringing and increasing the setting time [2–7].

However, the proposed D-LDO specifies that $I_{OUT}$ is nearly equal to $I_{LOAD}$ at time $T_2$ by turning off half of the turned-on PMOS transistors, as shown in Figure 1C. This process removed the unwanted large overshoot voltage and reduced settling time. The proposed D-LDO also adopted the coarse-fine PMOS arrays to achieve a fast transient response and low quiescent current [6,7].

Figure 2 shows the proposed coarse-fine D-LDO with an auxiliary power stage consisting of an auxiliary PMOS array and auxiliary shift-register (SR) attached to the conventional coarse-fine D-LDO. The proposed D-LDO removed the large unwanted undershoot voltage by using the auxiliary power stage during undershooting. Moreover, the output ripple voltage was reduced and the transient response was enhanced by using a comparator with a complete comparison signal (DONE) (Figure 2B) operating the SR and Bi-SRs immediately after the comparison completes.

The D-LDO supplied a maximum output current when 32 coarse PMOS transistors were turned on. The auxiliary PMOS array increased the output current during the undershoot. When the load current was changed from light to
heavy, the output current increased by as much as two large PMOS transistors per clock cycle by turning on both the auxiliary and coarse PMOS transistors. Therefore, the D-LDO requires 32 auxiliary PMOS transistors to cover the maximum load current changing. The fine PMOS array containing 32 PMOS transistors was designed to cover two coarse PMOS transistors.

In the steady state, the D-LDO finely adjusts the output current ($I_{\text{OUT}}$) using the fine power stage and CMP1 with a slow clock frequency (CLK_F_CMP = CLK_Slow). When the CMP1 compares $V_{\text{OUT}}$ and $V_{\text{REF}}$, the fine 32-bit Bi-SR changes the fine PMOS array current ($I_{\text{FINE}}$) to the comparator output signal (CMP_F) by the complete comparison signal (DONE_F).

When the peak detector detects an overshoot or undershoot outside of $V_{\text{REF_H}}$ and $V_{\text{REF_L}}$, CMP1 is deactivated (CLK_F_CMP = 0) and the coarse mode is triggered. Then, $I_{\text{FINE}}$ becomes halved by the half reset signal (RST_Half). $I_{\text{OUT}}$ is controlled coarsely using the coarse and auxiliary power stages via an asynchronous self-clock signal (CLK_Self_Fast) with a fast clock frequency to prevent the use of a high-frequency clock generator. The coarse PMOS array current ($I_{\text{COARSE}}$) decreased or increased from the coarse 32-bit Bi-SR according to the increased signal (INC) and coarse shift-register clock signal (CLK_Coarse). These two signals were changed according to the CMP2 output signals (CMP_H and DONE_H) or CMP3 output signals (CMP_L and DONE_L), when an overshoot (CMP_H = 1) or undershoot (CMP_L = 1) is generated, respectively. Except for the undershoot, the auxiliary PMOS array current remains at zero ($I_{\text{AUX}} = 0$) because the auxiliary 32-bit SR is set by the auxiliary set signal (SET_AUX = 1). When an undershoot is generated (CMP_L = 1), $I_{\text{AUX}}$ increases from the auxiliary 32-bit SR as governed by the auxiliary clock signal (CLK_AUX) from CMP3 output signals (CMP_L and DONE_L).

Figure 3 shows the transient waveforms of the proposed D-LDO when undershoots and overshoots are generated. The coarse and auxiliary PMOS currents ($I_{\text{COARSE}}$ and $I_{\text{AUX}}$) are 16 times greater than the fine PMOS current ($I_{\text{FINE}}$). The currents ($I_{\text{FINE}}$, $I_{\text{COARSE}}$, and $I_{\text{AUX}}$) increased or decreased as much as a PMOS transistor per clock cycle from the auxiliary and bidirectional shift-registers, as shown in Figure 4. Exceptionally, $I_{\text{COARSE}}$ decreased as much as two PMOS transistors per clock cycle from the coarse bidirectional shift-register during the overshoot.

When the load current ($I_{\text{LOAD}}$) is changed from light to heavy, D-LDO detects the undershoot and operates under the coarse mode with a fast clock frequency. It increases both the $I_{\text{COARSE}}$ and $I_{\text{AUX}}$ until $V_{\text{OUT}}$ reaches $V_{\text{REF_L}}$. When $V_{\text{OUT}} = V_{\text{REF_L}}$, the output current ($I_{\text{OUT}}$) is nearly two times that of $I_{\text{LOAD}}$. Then, $I_{\text{OUT}}$ becomes almost equal to $I_{\text{LOAD}}$ by setting $I_{\text{AUX}}$ to 0. Therefore, $V_{\text{OUT}}$ can be settled within the

**FIGURE 2** (A) Proposed coarse-fine D-LDO and (B) comparator with a comparison complete signal

**FIGURE 3** Transient waveforms of the proposed D-LDO when an undershoot and overshoot are generated.
boundary voltages of $V_{\text{REF}_L}$ and $V_{\text{REF}_H}$. In addition, fine mode is retriggered and $V_{\text{OUT}}$ is finely regulated to $V_{\text{REF}}$.

When $I_{\text{LOAD}}$ is changed from heavy to light, overshoot is detected and coarse mode is triggered. However, the auxiliary power stage is not operative, because $I_{\text{AUX}}$ was set to 0. To improve the transient response, D-LDO decreases $I_{\text{COARSE}}$ as much as two PMOS transistors per clock cycle. After $V_{\text{OUT}}$ reaches the value of $V_{\text{REF}_H}$, $V_{\text{OUT}}$ continually decreases, because $I_{\text{OUT}}$ is smaller than that of $I_{\text{LOAD}}$, causing an undershoot. If the undershoot retriggers coarse mode, D-LDO operates in the same manner as the light-to-heavy load changing. If not, the D-LDO operates under fine mode. As a result, the D-LDO removes ringing, which improves the transient response for both the overshoot and undershoot.

When the coarse-fine D-LDO supplies the maximum or minimum $I_{\text{FINE}}$ in fine mode, $V_{\text{OUT}}$ is not regulated at $V_{\text{REF}}$ because $I_{\text{FINE}}$ does not show any further increases or decreases. The D-LDO requires regulation compensation to generate the large glitch voltage [7]. If $I_{\text{FINE}}$ is fixed to the maximum or minimum before operating in coarse mode, regulation compensation occurs in the transient state. This generates a large glitch and may retrigger initiation of coarse mode. However, after the newly proposed D-LDO settles $V_{\text{OUT}}$ within the boundary voltages of $V_{\text{REF}_H}$ and $V_{\text{REF}_L}$ during coarse tuning time ($\Delta T_1$), the difference between $I_{\text{OUT}}$ and $I_{\text{LOAD}}$ falls between $-\Delta I_{\text{COARSE}}$ and $\Delta I_{\text{COARSE}}$. The fine PMOS array can supply a current of 0-2 $\Delta I_{\text{COARSE}}$ and initially set to $\Delta I_{\text{COARSE}}$ by the half reset signal (RST_Half). Therefore, the novel D-LDO can regulate $V_{\text{OUT}}$ to $V_{\text{REF}}$ using the fine PMOS array in fine mode. This can remove the large glitch voltage of the regulation compensation in the transient state.

Figure 5 shows the digital controller where, in steady state, the fine enable signal (Fine_EN) was high because $\text{CMP}_H = 0$ and $\text{CMP}_L = 0$. $\text{CMP}_1$ in Figure 2A operates by the fine comparator clock signal (CLK_F_CMP) with a slow clock frequency (CLK_Slow). The peak detector operates via asynchronous self-clock signal (CLK_Self_Fast) with a fast clock frequency, as shown in Figure 6. When the CLK_Self_Fast changes from low to high, $\text{CMP}_2$ and $\text{CMP}_3$ compare $V_{\text{OUT}}$ with $V_{\text{REF}_H}$ and $V_{\text{REF}_L}$, respectively. After both comparisons are performed, the complete comparison signals (DONE_H and DONE_L) become low and CLK_Self fast becomes low. This resets $\text{CMP}_2$ and $\text{CMP}_3$ so DONE_H and DONE_L become low again and CLK_Self_fast becomes high. In this manner, a fast-asynchronous self-clock signal is generated. Therefore, D-LDO can operate the peak detector by the fast-asynchronous self-clock signal without the need for a high-frequency clock generator.

When overshoot or undershoot is generated, as shown in Figure 7, the comparator output signal, $\text{CMP}_H$ or $\text{CMP}_L$, respectively increases. Then, Fine_EN becomes lower and the fine PMOS array current ($I_{\text{FINE}}$; described...
in Figure 2A) becomes halved due to the half reset signal (RST_Half). The coarse PMOS array current ($I_{\text{COARSE}}$) decreases or increases according to the increase signal (INC) via the coarse bidirectional shift-register clock signal (CLK_Coarse). The auxiliary PMOS array current ($I_{\text{AUX}}$) increased during the undershoot due to the auxiliary shift-register clock signal (CLK_AUX).

Figure 8 shows the transient waveforms of the newly proposed D-LDO in the start-up state. Initially, the novel D-LDO operates in coarse mode the same manner that caused the undershoot. When $V_{\text{OUT}}$ is settled within the $V_{\text{REF_H}}$ and $V_{\text{REF_L}}$ boundary voltages, the D-LDO operates in fine mode and finely regulates $V_{\text{OUT}}$ to $V_{\text{REF}}$.

Figures 9 and 10 show the ripple voltages ($V_{\text{ripple}}$) of the conventional and novel D-LDOs, respectively. The conventional D-LDO operates both the comparator and bidirectional shift-registers (Bi-SR) using the same clock (CLK). Bi-SR changes the output current ($I_{\text{OUT}}$) according to the comparator output signal CMP_OUT generated at the previous rising edge of CLK. This increases the ripple voltage caused by a single clock delay. However, the proposed D-LDO operates the Bi-SR with a complete comparison signal (DONE), as shown in Figure 10 [10]. Therefore, $I_{\text{OUT}}$ changes as soon as the comparison is completed, reducing the ripple voltage. Table 1 shows a comparison of the ripple voltages of the two devices. The proposed D-LDO reduces the ripple voltage from 50.5 mV to 11.4 mV at CLK = 50 MHz.
3 | EXPERIMENTAL RESULTS

The proposed D-LDO was fabricated using a 65-nm CMOS process with $V_{DD} = 1.2$ V. Figure 11 shows the chip microphotograph of the prepared D-LDO with an area of 0.0056 mm$^2$. The 1 nF output capacitor was incorporated on-chip, occupying 0.59 mm$^2$. The test bench was implemented on-chip to measure the output voltage during the load current changes. Figure 12 shows the measurement setup of the D-LDO at $V_{DD} = 1.2$ V and CLK_Slow = 50 MHz. $V_{REF_H}$ and $V_{REF_L}$ are 15 mV above and below the $V_{REF}$ of 1 V. The off-chip resistor, $R_1$, initially drives the light load current in the D-LDO. The on-chip resistor, $R_2$, and switch, $S_1$, in the test bench change the load current from light to heavy. An auxiliary enabled signal (AUX_EN) was then used to activate the auxiliary power stage.

Figure 13 shows the measurement of transient responses with and without the auxiliary power stage when the load current changed from 10 mA to 100 mA with rising and falling edge times of 20 ns at $V_{IN} = 1.2$ V and $V_{OUT} = 1$ V. In steady state, the D-LDO regulates $V_{OUT}$ to 1 V from an input voltage of 1.2 V. When the load current was changed from 10 mA to 100 mA, the undershoot and overshoot of the proposed D-LDO decreased from 139 mV to 47 mV and 30 mV to 23 mV, respectively. In addition, the settling time decreased from 2.1 μs to 130 ns. The ripple voltage ($V_{ripple}$) was 4 mV only when using the proposed comparator.

Figure 14 shows the measurement of transient responses of the newly proposed D-LDO, when the load current changes from 10 mA to 100 mA with rising and falling edge times of 20 ns at $V_{IN} = 1.2$ V and $V_{OUT} = 0.5$ V. When the load current was changed from 10 mA to 100 mA, the undershoot and overshoot of the proposed D-LDO decreased from 139 mV to 47 mV and 30 mV to 23 mV, respectively. In addition, the settling time decreased from 2.1 μs to 130 ns. The ripple voltage ($V_{ripple}$) was 4 mV only when using the proposed comparator.

Table 1 shows the performance comparisons of various D-LDOs. The maximum output current was 100 mA, quiescent current was 75 μA, and peak current

<table>
<thead>
<tr>
<th>Table 1</th>
<th>Conventional</th>
<th>Proposed</th>
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<tr>
<td>Technology</td>
<td>65 nm CMOS</td>
<td>65 nm CMOS</td>
</tr>
<tr>
<td>Supply voltage</td>
<td>1.2 V</td>
<td>1.2 V</td>
</tr>
<tr>
<td>Clock frequency</td>
<td>50 MHz</td>
<td>50 MHz</td>
</tr>
<tr>
<td>Ripple voltage</td>
<td>50.5 mV</td>
<td>11.4 mV (22.6%)</td>
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<tr>
<td>@ $I_{LOAD} = 10$ mA</td>
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efficiency was 99.93% with a power supply rejection ratio (PSRR) of 53.9 dB at DC.

The widely used figure-of-merit (FoM) for D-LDOs [3,5–7] can be described as follows:

\[
\text{FoM} = \frac{C_{\text{OUT}} \cdot \Delta V_{\text{OUT}}}{\Delta I_{\text{LOAD}}} \cdot \frac{I_{Q}}{\Delta I_{\text{LOAD}}},
\]

where \(C_{\text{OUT}}\) is the output capacitance, \(\Delta V_{\text{OUT}}\) is the maximum undershoot voltage, \(I_{Q}\) is the quiescent current, and \(\Delta I_{\text{LOAD}}\) is the load current change range. Coarse-fine D-LDOs exhibit smaller FoMs than other control-type D-LDOs. The newly proposed D-LDO exhibited the smallest settling time among coarse-fine D-LDOs by removing ringing in the transient state.
A low-ripple coarse-fine D-LDO without ringing in the transient state was proposed herein. It removes the ringing and improves the transient response using an auxiliary power stage, which reduces the output ripple voltage by using a comparator with a complete comparison signal. The undershoot and overshoot decreased from 139 mV to 47 mV and 30 mV to 23 mV, respectively. The settling time decreased from 2.1 μs to 130 ns and the ripple voltage was 4 mV.

ACKNOWLEDGMENTS
This work was supported by the Ministry of Education, Science and Technology through the Basic Science Research Program, National Research Foundation of Korea under Grant 2018R1D1A1B07047986 and the Competency Development Program for Industry Specialists of the Korean Ministry of Trade, Industry and Energy (MOTIE), operated by the Korea Institute for Advancement of Technology (KIAT; No. N0001883, HRD program for Intelligent semiconductor Industry). The chip fabrication and EDA tool were supported by the IC Design Education Center (IDEC), Korea.

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1. Y. Okuma et al., 0.5-V input digital LDO with 98.7% current efficiency and 2.7-μA quiescent current in 65 nm CMOS, Proc. IEEE Custom Integr. Circuits Conf., San Jose, CA, USA, Sept. 2010, pp. 1–4.

TABLE 2 Performance comparisons of previously reported D-LDOs and that developed herein

<table>
<thead>
<tr>
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<th></th>
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<tr>
<td>Technology (nm)</td>
<td>65</td>
<td>130</td>
<td>130</td>
<td>65</td>
<td>28</td>
<td>65</td>
<td>65</td>
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<tr>
<td>Control</td>
<td>SAR/PD/PWM</td>
<td>Adaptive</td>
<td>Delay ADC/PI</td>
<td>S-DLDO</td>
<td>Coarse-fine</td>
<td>Coarse-fine</td>
<td>Coarse-fine</td>
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<tr>
<td>Active area (mm²)</td>
<td>0.0023</td>
<td>0.18</td>
<td>0.0631</td>
<td>0.014</td>
<td>0.021</td>
<td>0.01</td>
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<td>Input voltage (V)</td>
<td>0.5–1.0</td>
<td>0.50–1.22</td>
<td>0.84–1.24</td>
<td>0.7–1.2</td>
<td>1.1</td>
<td>0.6–1.1</td>
<td>0.6–1.2</td>
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<td>Output voltage (V&lt;sub&gt;OUT&lt;/sub&gt;, V)</td>
<td>0.30–0.45</td>
<td>0.35–1.17</td>
<td>0.6–1.0</td>
<td>0.6–1.1</td>
<td>0.9</td>
<td>0.4–1.0</td>
<td>0.5–1.0</td>
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<td>Load current (I&lt;sub&gt;LOAD&lt;/sub&gt;, mA)</td>
<td>2</td>
<td>145</td>
<td>50</td>
<td>25</td>
<td>200</td>
<td>100</td>
<td>100</td>
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<td>Quiescent current (I&lt;sub&gt;Q&lt;/sub&gt;, μA)</td>
<td>14</td>
<td>3.200</td>
<td>400</td>
<td>6</td>
<td>110</td>
<td>82</td>
<td>75</td>
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<td>Peak current efficiency (%)</td>
<td>99.8</td>
<td>97.8</td>
<td>99.2</td>
<td>99.9</td>
<td>99.94</td>
<td>99.92</td>
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<td>N/A</td>
<td>0.06</td>
<td>0.13</td>
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<td>N/A</td>
<td>N/A</td>
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<td>3</td>
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<td>PSRR@DC</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>53.9 dB</td>
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<td>Output capacitance (C&lt;sub&gt;OUT&lt;/sub&gt;, nF)</td>
<td>0.4</td>
<td>1.5</td>
<td>0.5</td>
<td>1.0</td>
<td>23.5</td>
<td>1.0</td>
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<td>Edge time</td>
<td>&lt;1 ns</td>
<td>0.1 ns</td>
<td>10 ns</td>
<td>4 μs</td>
<td>20 ns</td>
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<tr>
<td>ΔV&lt;sub&gt;OUT&lt;/sub&gt;@ΔI&lt;sub&gt;LOAD&lt;/sub&gt;</td>
<td>40 mV @1.06 mA</td>
<td>280 mV @40 mA</td>
<td>250 mV @50 mA</td>
<td>200 mV @23.5 mA</td>
<td>120 mV @180 mA</td>
<td>55 mV @98 mA</td>
<td>47 mV</td>
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<tr>
<td>Setting time (μs)</td>
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<td>0.25</td>
<td>2.08</td>
<td>&gt;10</td>
<td>0.7*</td>
<td>0.13</td>
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<td>FoM (ps)</td>
<td>199</td>
<td>63.9</td>
<td>20</td>
<td>2.17</td>
<td>7.75</td>
<td>0.43</td>
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*Maximum possible settling time ≈1.2 μs.

4 CONCLUSIONS

This work was supported by the Ministry of Education, Science and Technology through the Basic Science Research Program, National Research Foundation of Korea under Grant 2018R1D1A1B07047986 and the Competency Development Program for Industry Specialists of the Korean Ministry of Trade, Industry and Energy (MOTIE), operated by the Korea Institute for Advancement of Technology (KIAT; No. N0001883, HRD program for Intelligent semiconductor Industry). The chip fabrication and EDA tool were supported by the IC Design Education Center (IDEC), Korea.

ORCID
Ki-Chan Woo https://orcid.org/0000-0002-6992-3917


AUTHOR BIOGRAPHIES

Ki-Chan Woo received his BS degrees in electronics engineering from Chungbuk University, Republic of Korea, in 2013. He is currently working toward his PhD degree at the Electrical Engineering and Computer Science of Chungbuk University, Republic of Korea. His research interests include analog circuits, digital circuits, memory circuits, and power IC designs.

Byung-Do Yang received his BS, MS, and PhD degrees in electrical engineering and computer science from Korea Advanced Institute of Science and Technology (KAIST), Republic of Korea, in 1999, 2001, and 2005, respectively. He was a senior engineer in the Memory Division of Samsung Electronics, Kyungki-Do, Republic of Korea, in 2005, where he was involved in the design of DRAM. In 2006, he joined the department of electronics engineering at Chungbuk National University, Republic of Korea, where he is currently a Professor. His research interests include analog circuits, digital circuits, memory circuits, and power IC designs.