A Study on Signal Analysis of the Data Acquisition System for Photosensor

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요 약

슬립링 기술을 가진 스플리트 CT의 주요 장점으로는 X-ray 튜브의 연속적인 휘전에 의해 환자에 대한 정교한 손실 없이 데이터를 연속적으로 획득할 수 있다는 것이다. 또한, X-선원의 인체 손위의 감소를 위해서, 고속기의 저노이즈 및 빠른 데이터 획득 시간을 갖는 시스템이 요구되어 진다. 본 연구에서는, CT 적응을 위해 다채널 포토센서 및 데이터 획득 시스템이 개발되어졌다. 포토센서의 모듈은 16채널 CdWO4 크리스탈 및 실리콘 베이스의 포토다이오드가 사용되었다. 또한, 포토센서로부터 영역 신호에 대한 전기적인 특징을 위해, 트랜스 임피던스 스위치 인테그레이터가 사용되었다. 스위치 인테그레이터는 CT 적응에 대해 적합한 시그널 범위의 노이즈 폐쇄를 갖고 있다. 데이터 획득과 20 bit ADC 의 컨트롤은 FPGA를 이용하였고, 코드는 VHDL을 사용하였다. CdWO4 기반의 실리콘 포토센서와 고SNR 및 좋은 시그널 범위를 가진 광저산 및 FPGA기반의 디지털 하드웨어는 CT적용 이외에도 하드웨어 변경 없이 다른 분야에서도 이용 가능하다.

ABSTRACT

The major advantage of slip-ring technology in Spiral CT is that it facilitates continuous rotation of the x-ray tube, so that volume data can be acquired from a patient quickly. Not only for such a fast scan, but also for the dose reduction purpose, high signal-to-noise ratio and fast data acquisition system is required. In this study, we have built a multi-channel photodetector and multi-channel data acquisition system for CT application. The detector module consisted of CdWO4 crystal and Si photodiode in 16 channels. For the performance test of the preamplifier stage, both the transimpedance and switched integrator types are optimized for the photodetector modules. Switched integrator showed better noise performance in the limited bandwidth which is suitable for the current CT application. The control sequence for data acquisition and 20 bit ADC is designed with VHDL(Very High Speed Integrated Circuit Hardware Description Language) and implemented on FPGA(Field Programmable Gate Array) chip. Our Si photodiode detector module coupled to CdWO4 crystal showed comparable signal with other commercially available photodiode for CT. Switched integrator type showed higher SNR but narrower bandwidth compared to transimpedance preamplifier. Digital hardware is designed by FPGA, so that the control signal could be redesigned without hardware alteration.

Keyword : Signal Analysis, Photo detector, Switched integrator, ADC, SNR

1. INTRODUCTION

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Compared to the conventional single slice or multi-slice X-ray CT, the spiral X-ray CT has advantage so fast scanning time and patient dose reduction. However, in order to achieve these, not only the detector but also the data
acquisition system (DAS) should be fast and have the high signal-to-noise ratio. The DAS, positioned between the detector array and the computer, performs the following three major functions: (1) amplifying the signal from detectors, (2) converting the analog signal into the digital data, (3) transmitting the digital data to the computer for reconstruction and further image processing. The detector signal is generally very weak so it is preamplified before it is converted into digital data.

In this study, a 16-channel data acquisition system with bit resolution is developed. Also a 16 channel detector module consisted of 16 CdWO4 crystal and photodiode array was prepared for the test of the developed DAS.

2. MATERIALS AND METHODS

2.1 CONFIGURATION OF THE SYSTEM

The developed system is made of a 16 channel detector, a 16 channel pre-amplifier, an A/D converter, a digital logic interface and a user interface as shown in Figure 1. common-mode rejection and impedance matching. ADC(ADS1250) was used to digitize the amplified analog signal. For the pre-amplifier stage, we have tested two configurations as in Fig.3, 1) transimpedance amplifier (OPA124) + dual integrator (OPA124) 2) switched dual integrator (ACF2101) as a preamplifier. A dual integrator (an odd integrator and an even integrator) is used in order to achieve the zero integration dead time for maximum utilization of detector signal during the continuous scan. While the detector signal charge is integrated in one integrator, the signal in the other integrators is transmitted into the ADC through a MUX. For the maximum signal-to-noise ratio, the impedance matching between the photodiode and the pre-amplifier is accomplished by feedback capacitor for transimpedance amplifier. The impedance can be matched without feedback resistance for switched integrator. The gain peaking, offset compensation, the bandwidth, noise and phase margin of preamplifier are considered in design. Since switched integrator pre-amplifier showed better performance in our application, this type of pre-amplifier is used for the rest of the experiment. For the pre-amplifier stage, we have tested two configurations as in Fig.3, 1) transimpedance amplifier (OPA124) + dual integrator (OPA124) 2) switched dual integrator (ACF2101) as a preamplifier. A dual integrator (an odd integrator and an even integrator) is used in order to achieve the zero integration dead time for maximum utilization of detector signal during the continuous scan. While the detector signal charge is integrated in one integrator, the signal in the other integrators is transmitted into the ADC through a MUX. For the maximum signal-to-noise ratio, the impedance matching between the photodiode and the pre-amplifier is accomplished by feedback capacitor for transimpedance amplifier. The impedance can be matched without feedback resistance for switched integrator. The gain peaking, offset compensation, the bandwidth, noise and phase margin of preamplifier are considered in design. Since switched integrator pre-amplifier showed better performance in our application, this type of pre-amplifier is used for the rest of the experiment. [2]

The outputs of the 16 integrators (ACF2101) are multiplexed by the select switch to buffer (OPA2107) which prevents the signal crosstalk. Then the signal is delivered to a monolithic gain (+10) differential amplifier (INA106) to control the gain with a potentional-meter. A small resistance is added to both the inverting input and
the noninverting input to maintain good common-mode rejection and impedance matching. ADC (ADS1250) was used to digitize the amplified analog signal. [3]

Finally, the timing and the control signal for the integrators, the address signal of the M, the timing signal of PGA-ADC and the control signal of data transmission are generated in the digital logic board implemented by a FPGA which was coded with VHDL. [6,7]

![Diagram](image)

Fig. 3 (A) Feedback resistance를 이용한 트랜스 임피던스 증폭기 (B) 스위치 듀얼 적분기

2.2 NOISE ANALYSIS

The photodiodes have the junction capacitance of 35pF and shunt resistance of 30MΩ at zero bias(photovoltaic mode). The reverse current at 5 V is around 1 nA. The photovoltaic mode of operation is preferred when a photodiode is used in low frequency application(up to 350kHz) and less sensitive to temperature.

Transimpedance amplifier, which is low-input current FET, is used to monitor photodetector. The noise gain response for the transimpedance amplifier is shown in Fig. 4. The feedback resistance and capacitance control the bandwidth and the noise of the amplifier, which should be optimize to closely match the physical system bandwidth.

![Diagram](image)

Fig. 4 Noise gain response of transimpedance amplifier

The total noise of transimpedance amplifier can be computed by RMS(Root Mean Square) summation of each noise component. Thus the total noise is

\[ E_{total} = \sqrt{E_{n01}^2 + E_{n02}^2 + E_{n03}^2 + E_{n1}^2 + E_{n2}^2} = 35\mu V_s \]  \hspace{1cm} (1)

\[ E_{n01}, E_{n02}, \text{ and } E_{n03} \] represent the output noise component produced by the resistor itself, the amplifier’s input current noise, and the amplifier’s input voltage noise, respectively.

\[ E_{noise1}, E_{noise2}, \text{ and } E_{noise3} \] are input noise voltages defined by pole and zero frequency. [1-4]

Using the feedback capacitance value calculated for a 65 degree phase margin, the effective signal and noise bandwidth is following : [1-4]

\[ BW_{Signal} = \frac{1}{2\pi R_{feedback} C_{feedback}} = 22.7kHz \]  \hspace{1cm} (2)

\[ BW_{Noise} = \frac{1}{2\pi R_{feedback} C_{feedback}} = 71kHz \]  \hspace{1cm} (3)

![Diagram](image)

Fig. 5 Noise gain response of switched integrator amplifier
The noise gain response for the switched integrator during integration mode is shown in Fig. 5. The typical on-resistance of the hold switch is $1.5\Omega$, and the typical open-resistance of the reset is $1000\Omega$.

The low frequency pole of the noise gain is equal to:

$$f_p = \frac{1}{2\pi R_{\text{RESET}} C_{\text{INT}}} = 1.59\text{mHz} \quad (4)$$

where $R_{\text{RESET}} = 1000\Omega$ and $C_{\text{INT}} = 100\text{pF}$ in our circuit. The pole frequency would occur at $1.59\text{mHz}$. This pole is usually found at very low frequencies. The zero frequency of the noise gain plot is equal to:

$$f_z = \frac{1}{2\pi R_1 (R_{\text{RESET}} + C_{\text{INT}})} = 3.5\text{Hz} \quad (5)$$

where $R_1$, shunt resistance, is $30\Omega$, $C_1$, the junction capacitance, is $350\text{pF}$. This zero frequency is also usually found at low frequencies. In our circuit, $f_z = 3.5\text{Hz}$. [1-4]

Since the noise spectrum shows high only in the very low and narrow, e.g. below $3.5\text{Hz}$, the total noise is largely determined by the bandwidth and noise density of the high frequency region.

[1-4]

High frequency noise gain = $\left( 1 + \frac{C_1}{C_{\text{INT}}} \right)$ \quad (6)

The total rms noise is estimated as equal to

Total rms noise = $\left( 1 + \frac{C_1}{C_{\text{INT}}} \right) = 45\mu V$ \quad (7)

3. RESULTS

3.1 Detector module

Our photodiode is made of $280\mu$ thick, $2600\Omega \cdot \text{cm}$ resistivity, n-type substrate wafer. Its p-layer, i-layer (n-type), n"-layer is 3, 77, $200\mu$ thick, respectively. The measured junction capacitance was $5\text{pF}$. However, other commercial module junction capacitance were $350-400\text{pF}$.

Under the tube voltage $100\text{kVp}$, tube current $20\text{mA}$, and X-ray pulse time $8.3\text{ms}$, the signal magnitude was $40\text{nA}$ for our photodiode, and $80\text{nA}$ for the commercial ones. If its signal is normalized to its area, the normalized signal is comparable.

3.2 The pre-amplifier - Transimpedance and Switched Integrator Type

The performance of transimpedance and switched integrator was compared under the tube voltage $100\text{kVp}$, tube current $20\text{mA}$, X-ray pulse time $8.3\text{ms}$.

Table-I is summary of measured value of junction capacitance and dark current of photodiode and calculation result while the signal current of photodiode maintains $30\text{nA}$ at zero bias condition, integration time is $1\text{ms}$, discharge time is $50\text{ms}$. The GBP calculation for the transimpedance amplifier used phase margin. [1]
3.3 Data Acquisition System

For the performance test of the switched integrated type DAS, green LED, which has similar wavelength of scintillating light of CdWO₄ was used as light source instead of X-ray. The DAS gain was set to 10⁶, which is in series connection of 10⁷ gain in switched integrator and 10⁴ gain in the gain controller(INA106). Total noise of the DAS is measured at the output of the ADC with 25kHz bandwidth under constant irradiation of green LED. For the ADC noise measurement, variance value was measured under constant DC voltage applied as ADC input signal. The dynamic range is defined as a reciprocal of standard deviation in ppm.

Table 2. Total noise through a switched integrator, gain controller, multiplexer and ADC.

<table>
<thead>
<tr>
<th>Optimum Performance</th>
<th>Total Gain</th>
<th>10⁶</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standard Deviation under constant irradiation</td>
<td>50ppm</td>
<td></td>
</tr>
<tr>
<td>Standard Deviation of ADC value under constant DC signal</td>
<td>4.3ppm</td>
<td></td>
</tr>
<tr>
<td>Total Noise</td>
<td>200μVrms</td>
<td></td>
</tr>
<tr>
<td>Dynamic Range</td>
<td>86dB</td>
<td></td>
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</tbody>
</table>

4. DISCUSSION

X-ray irradiation experiment showed the Si photodiode comparable signal to other commercial photodiode, yet to be improved. There could be several ways for the improvement. One is to reduce p-layer thickness, since much of light emitted from scintillator is absorbed in p-layer. In this study, photodiode with 3mm thick p-layer is used. Later version is reduced down to 1.8 or less than 1mm by ion implantation process.

This method still could be susceptible to surface contamination. The other is to form a junction underneath the surface by ion implantation, so that less susceptible to the surface contamination. This method also will provide very thin surface layer down to under 1 mm, so that transparent to more light photons.

Since the noise characteristics in a photodiode-preamplifier unit is related to many physical and electric parameters of the photodiode and the preamplifier, it needed to be optimized. By proper choice of feedback capacitor maximize SNR. We compared the detector-preamplifier system between transimpedance amplifier and switched integrator for various parameters. It is important to make proper selection of the component value of circuit through phase analysis and impedance matching. The feedback capacitor used for the transimpedance type was 0.7pF considering 65degree phase margin for stability and increased GBP.

In switched integrator type, a large feedback capacitor, 100pF, is used to improve the noise performance of the circuit. The noise performance of the switched integrator is improved over the transimpedance amplifier, yet the bandwidth is considerably smaller. ADC noise is 4.3ppm which is corresponding to 108dB. This is quite close to ideal dynamic range 120dB. Also, the readout circuit for the DAS should have a uniform frequency response in the wide dynamic range.

5. CONCLUSION

The scintillator-photodiode detector module was developed, yet to be improved. The switched integrator preamplifier type showed better SNR performance in limited frequency bandwidth. Second stage and ADC noise was negligible for the amplified signal. Efficient, flexible and compact design of hardware was possible using FPGA. All the experiment was done with prototype made on breadboard, so that more noise was observed than we expected. We are observing less noise with in digital signal as well as analog signal along the progress we make the electronics in multi-layer PCB. We expect much improved SNR in detector module and DAS with a few improvement.
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