Low Power, Small Chip-size Mobile AM-LCD Drivers Using Time-sharing Output Architecture

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Abstract
We developed new circuit architecture for reducing the power consumption and chip-size of driver ICs. In this paper we describe a new drive scheme, based on the concept of time-sharing output and optimal circuit design based on color resolution. In case of 132 x 176-pixel class, we used only 8 O p-A mps for a 262-k color display.

1. Introduction
Recently, the global growth of mobile phones has increased rapidly. Additional functions such as e-mail and built-in cameras have also become popular. Furthermore, with the development of terrestrial digital broadcasting, the TV function is considered to be a killer application for future products. Thus, AM-LCDs are now a major type of mobile phone panel due to their high picture quality. Driver ICs are key components of mobile AM-LCDs, because they greatly influence the display performance, such as power consumption and system costs.

Some techniques for driver ICs have been proposed and have helped to raise the display performance [1]-[5]. However, further driver IC enhancements are required to meet consumer demands. To meet these objectives, we developed the technologies described here.

2. Chip Architecture
Figure 1 shows a block diagram of our one-chip driver. One of the features is the embedded graphics RAM in the source drive [1]. This architecture can eliminate the need to transfer display data from the external processor, unless it is rewritten. The timing generator automatically produces the RAM data readout signals, thus minimizing power consumption. Furthermore, this system is effective for moving pictures as well as still pictures, because in order to suppress flicker, the LCD requires a frame frequency of 60-90 frames/s, which is much higher than the usual frame rate for moving pictures of 15 or 30 frames/s.

Figure 1. Driver IC Block diagram

The choice of driving method is important in designing driver ICs, because it affects the power consumption, display quality, and cost. Several driving schemes have been proposed for AM-LCDs. From these schemes, we chose the “common inversion method” because of its lower source voltage amplitude of around 5 V. This means small-sized and high-efficiency transistors are available for the source driving circuit.

Another feature is that the operation setting is programmable using fetch instructions from the external processor. The gamma-collection is a typical example. Other drive conditions, such as frame frequency, drive voltage, and scan-mode can be
optimized using this architecture because of the panel characteristics. Therefore, we can easily maximize LCD performance.

3. Drive Technologies
In the driver IC, most power is consumed at the output circuit for the 64-level source voltage, so it is important to design it carefully. Figure 2 shows our first generation circuits [4]. The differences arise from the position of the Op-Amps, and there is a trade-off between drivability and circuit size. For example, Type A has the highest drivability, but its circuit size and power consumption is the largest because of the large number of Op-Amps required. On the other hand, Type C has the lowest drivability because its output impedance is the highest due to the string resistance, but the circuit size and DC power are the smallest. Therefore, we chose the circuit types according to the panel size and resolution, because these parameters determine the drivability requirements. Figure 3 shows the guidelines for selecting the circuit type. We used the low-power circuitry of type-B or type-C for mobile phones, because they are usually smaller than 2.5-inch panels.

As a second-generation circuit to realize the further chip size miniaturization and reduced power consumption, a key factor is to reduce the number of Op-Amps and DAC input bits. Therefore, we focused on type-B, and attempted to improve it. The first approach uses the FRC method. Figure 4 shows the FRC principles. A new gray-tone can be obtained by alternately displaying actual two-tone gray levels. Using this method reduced the number of Op-Amps from 64 to 32, and DAC input bits from 6 to 5.

Next, for lower resolution (conventionally covered by type-C), we developed a new drive method. Figure 5 shows the circuit diagram. During one horizontal period, each Op-Amp outputs several gray levels during time-sharing. The DAC selects one Op-Amp output using high-order bits of display data to
To determine the output phase corresponding to the low-order bits. Therefore, the number of Op-Amps can be reduced. For the 4-phase time-sharing combined with the FRC mentioned above, the number of Op-Amps decreased to 8 and the DAC input bits to 3.

Figure 5. Time-sharing output method

To realize this drive scheme, source lines are required for the voltage holding time called the Hi-Z period, during which source voltage is not applied. Therefore, we carefully studied this scheme to derive the most suitable drive waveform.

Figure 6 shows the drive waveform we considered first. Each drive circuit outputs the source voltage during one phase only when it corresponds to low-order bits of display data. This approach is simple, but we found it to have the following features.

a) The holding voltage in the Hi-Z period fluctuates depending on the output source voltage to the neighboring source line in subsequent phases. Therefore, we need to decrease the source voltage output amplitude as much as possible. However, the amplitude has the potential to reach its maximum value, depending on the display data during any phase.

b) The holding voltage in the Hi-Z period drops due to the leakage current from the source line. In order to avoid this, we need to make the Hi-Z period as short as possible. However, changing the time proportion for each phase is difficult in this scheme, because to cover the maximum voltage change condition, which requires a sufficient settling time, each horizontal period must be evenly divided.

Figure 7 shows the enhanced version we developed. The key feature is that each drive circuit continuously outputs the source voltage until the phase corresponds to the low-order bits of display data. In this case, the first phase has the potential of maximum voltage change, but the rest of the phases have fixed amplitudes that correspond to only one gray-tone. This means that the output period can be reduced in every phase except for the first, because the small voltage change can be completed in a short time. This approach is also useful for reducing the Hi-Z period. In addition to this, we alternated the phase order every frame to enable averaging of the Hi-Z period during each phase and achieve a uniform leakage current influence. These techniques allow us to solve the issues related to the time-sharing drive mentioned above.

Figure 6. Drive waveform (primitive)

Figure 7. Drive waveform (enhanced)
The most suitable division number for one horizontal period depends on the drivability requirements, i.e. panel size and resolution. For lower drivability requirements, more division is preferable. Therefore, we modified the selection guidelines as shown in figure 8. We can apply the 4-phase time-sharing to 132 x 176-pixel class, and 2-phase time-sharing to 176 x 220-pixel class.

b) We developed a new drive and circuit scheme for lower resolution panels. The source voltage is output as the gray levels change during one horizontal period. Therefore, it reduces the number of Op-Amps and DAC input bits. For 132 x 176-pixel class, only 8 Op-Amps enables a 262-k color display.

In addition, for 240 x 320-pixel class, we found the RGB order output method using LTPS-TFT circuits to be reasonable.

Table 1 shows the specifications of our typical driver ICs. Power consumption is extremely low. In addition, the chip size is also small, in spite of the inclusion of a graphics RAM. Therefore, these driver ICs provide an excellent balance between price and performance.

Table 1. Specifications

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<th>Chip-3</th>
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* Result of stand-alone chip on normal operation

5. References