International Journal of Internet, Broadcasting and Communication Vol.16 No.4 265-272 (2024)
http://dx.doi.org/10.7236/IJIBC.2024.16.4.265

IJIBC 24-4-30

Study on Nondestructive Analysis Techniques for Semiconductor Chips in Communication Device Development

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Abstract

Semiconductors are crucial components in communication technology, playing important roles in various communication systems. They are essential for signal processing, data transmission, and ensuring the stability of communication networks. In particular, high-performance semiconductor chipsets and processors enable ultra-fast data transmission and ultra-low latency in communication technology. For example, semiconductors are indispensable in smartphones, wireless networks, and satellite communication systems. For semiconductor packaging products, nondestructive internal analysis for defect analysis and process improvement without causing deformation of system packaging is an important part of the product development process. In this study, nondestructive analysis techniques using X-ray equipment are discussed. The results of this study can provide fast and accurate nondestructive analysis of semiconductor packaging products and can play a significant role in supporting the growth of the communication industry.

Keywords: *Communication Chip, Nondestructive Analysis, Semiconductor Package, Xray Analysis, CT Analysis*

1. Introduction

Semiconductors are crucial components in communication technology, playing vital roles in various communication systems. They are essential for signal processing, data transmission, and ensuring the stability of communication networks. In particular, high-performance semiconductor chipsets and processors enable ultra-fast data transmission and ultra-low latency in 5G communication technology, driving innovation across various industries. For example, semiconductors are indispensable in smartphones, wireless networks, and satellite communication systems. [1-3] The development of technology to implement highly integrated semiconductor devices that meet the low-power and high-performance operating conditions required in communication devices is essential. The direction of semiconductor development, which has focused on miniaturization processes to improve the performance and cost of semiconductor devices, is shifting towards system application fields in response to the demands of the communication industry. As communication devices are increasingly applied across various industries such as automotive, energy, medical, and environmental sectors, the demand for multifunctional semiconductors is rising. In communication devices,

Manuscript Received: October. 3, 2024 / Revised: October. 10, 2024 / Accepted: October. 15, 2024
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the rapid increase in demand for digitalization and multifunctionality of new devices necessitates the single packaging of individual components. System semiconductors must meet durability conditions, requiring the development of high-durability and high-efficiency system packaging technologies. The structure and design of semiconductor packages must satisfy performance requirements such as mechanical stability, electrical speed and stability, thermal dissipation capability, and reliability. The cycle time is determined by the delay between the semiconductor and the package, so to reduce package signal delay occurring in the connections between chips, it is necessary to increase the circuit integration, shorten the connection length, or improve the package materials to enhance package performance. [4-6]

Reducing the size of semiconductor packages to increase package efficiency (chip area/package area) significantly impacts the miniaturization and performance of semiconductor packages. To reduce package size, peripheral connections are being replaced with area array connections, or the pitch of leads is being reduced, although this can lead to handling difficulties and decreased productivity. Low-cost production technology determines the competitiveness of packages, making the design, materials, processes, and continuous productivity improvements of cost-competitive packages crucial. The reliability of the system is determined by the defect rate of each component, and the reliability of the package is determined by thermal and electrical reliability. The lifespan of a device decreases by 10% for every 10°C increase in semiconductor temperature, with approximately 2% switching delay occurring, making it important to maintain the temperature below 115°C. The reliability of the package is determined by electrical reliability, such as noise and signal stability, requiring optimization of the structure or appropriate material selection to improve the electrical reliability of the package. [1,7,8] Research is being conducted on the structure and material selection for system packaging methods such as Multichip Module (MCM), System-In-Package (SIP), or System-On-Package (SOP). SIP technology is a core packaging technology for communication products such as RF wireless communication, Bluetooth modules, high-performance PC cards, mobile video phone camera modules, mobile phones, and PDAs. [9-11] For semiconductor system packaging products, various analysis methods are used to analyze defects in finished products. In the past, pre-processing methods were mainly used for internal analysis of system packaging products, but these methods inevitably caused product deformation. Therefore, nondestructive internal analysis for defect analysis and process improvement without causing deformation of system packaging is an important part of the product development process. This study aims to develop semiconductor device technology for communication devices by analyzing physical issues through nondestructive analysis of semiconductor system packaging products.

2. Experiments and Discussions

The Nikon XTH 225 system is highly effective for the analysis of semiconductor packaging due to its advanced X-ray and CT inspection capabilities. The system′s high-resolution imaging, facilitated by a 3μm microfocus X-ray source, allows for detailed examination of fine structures within semiconductor packages. Additionally, the nondestructive testing feature, combined with real-time X-ray visualization, enables comprehensive analysis without damaging the samples. The fast reconstruction program generates high-quality 3D images, which are essential for identifying internal defects and ensuring the integrity of complex semiconductor packages. These attributes make the Nikon XTH 225 a highly suitable tool for maintaining the quality and reliability of semiconductor packaging in various applications. Figure 1 shows the equipment used in the experiments. Figure 1 (a) shows the overall view of the Nikon XTH 225 system, and Figure 1 (b) shows the X-ray beam generation unit, and the sample mounted on sample holder.

Figure 1. (a) Nikon XTH 225 system, and 1 (b) X-ray beam generation unit.

To generate 3D CT images from X-ray scans, it is essential to develop high-resolution X-ray measurement techniques that can capture detailed information for more precise data. The penetration degree of X-rays varies depending on the density and type of atoms in the material, allowing internal structures to be visualized through contrast differences. When X-rays pass through atoms, energy changes occur due to interactions with electrons around the nucleus, resulting in contrast variations detected by the detector. [12, 13]

The energy and amount of X-rays generated by electrons from the filament is determined by two adjustable conditions during measurement: the voltage applied between the filament and the metal anode, and the current flowing through the filament. [14, 15] The equipment used in the experiment can operate at a maximum voltage of 225kV and a current up to 450W. In this experiment, we first analyzed the optimal voltage and current values for the semiconductor packaging sample. Figure 2 shows the X-ray images of sample at various voltage and current conditions.

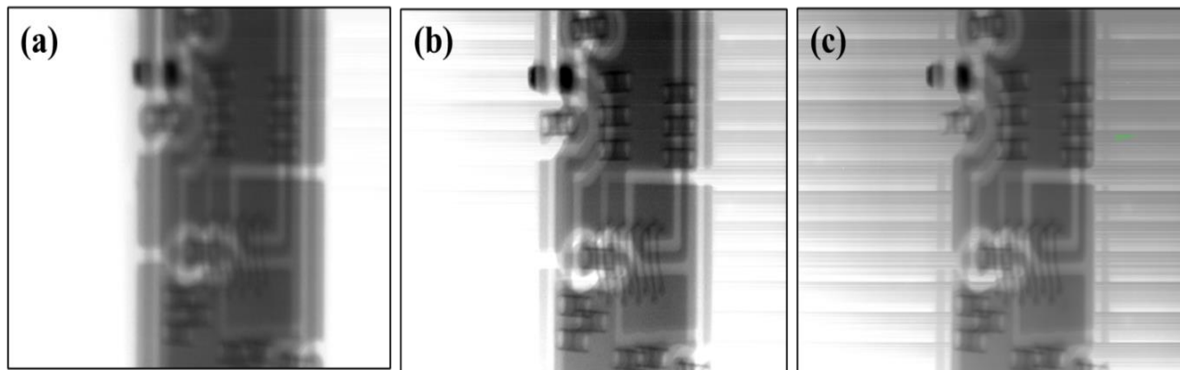

Figure 2. X-ray images of sample at various voltage and current conditions (a) 130kV and 250μA, (b) 160kV and 210μA, and (c) 190kV and 170μA.

The series of measurements were conducted on the same sample at identical locations using various voltage and current settings to determine the optimal conditions for X-ray imaging and CT analysis. Initially, at 130kV and 250μA, the low voltage resulted in insufficient X-ray penetration, which limited the amount of useful information that could be obtained. The relationship between current and X-ray generation was evident; however, increasing the current did not significantly enhance the data quality under low penetration conditions.

When the voltage was adjusted to 160kV and the current to 210μA, we observed the highest contrast ratio among the components within the sample. This setting provided the most detailed and informative images, indicating that an appropriate voltage level is crucial for achieving high penetration and contrast. Further adjustments in current at this voltage level showed that both increasing and decreasing the current led to a reduction in contrast ratio, highlighting the importance of maintaining an optimal balance.

At a higher setting of 190kV and 170μA, the increased voltage resulted in excessive X-ray penetration, which adversely affected the contrast ratio of the sample′s internal components. This result shows that fine-tuning both voltage and current are essential to avoid over-penetration and ensure high-quality imaging.

To obtain the most comprehensive information and enable precise CT imaging, high contrast ratios in X-ray measurements is a prerequisite. However, the optimal voltage and current values are not universal but vary depending on the sample′s thickness and material composition. Therefore, to conduct accurate CT analysis, it is imperative to first perform a series of measurements with varying voltage and current settings to identify the optimal conditions for each specific sample. This approach ensures that the X-ray imaging process yields the highest possible resolution and detail, facilitating more accurate and reliable analysis.

Although the equipment is capable of achieving a resolution of up to 3μm, the numerous contact points and small size of semiconductor packages present challenges. Inspecting each part individually is time-consuming and prone to errors, highlighting the need for the development of advanced CT analysis techniques.

Figure 3 shows the CT measurement result providing comprehensive visualizations of the sample, including top, front, side, and 3D images. This allows for detailed layer-by-layer analysis, enabling the examination of substrate interface conditions, detection of chip shorts, and identification of delamination. When performing CT measurements, you can set the measurement time and the number of cross-sections and more. For accurate analysis, it is essential to apply suitable values depending on the sample′s size and material. The 3D analysis software used was VGSTUDIO MAX.

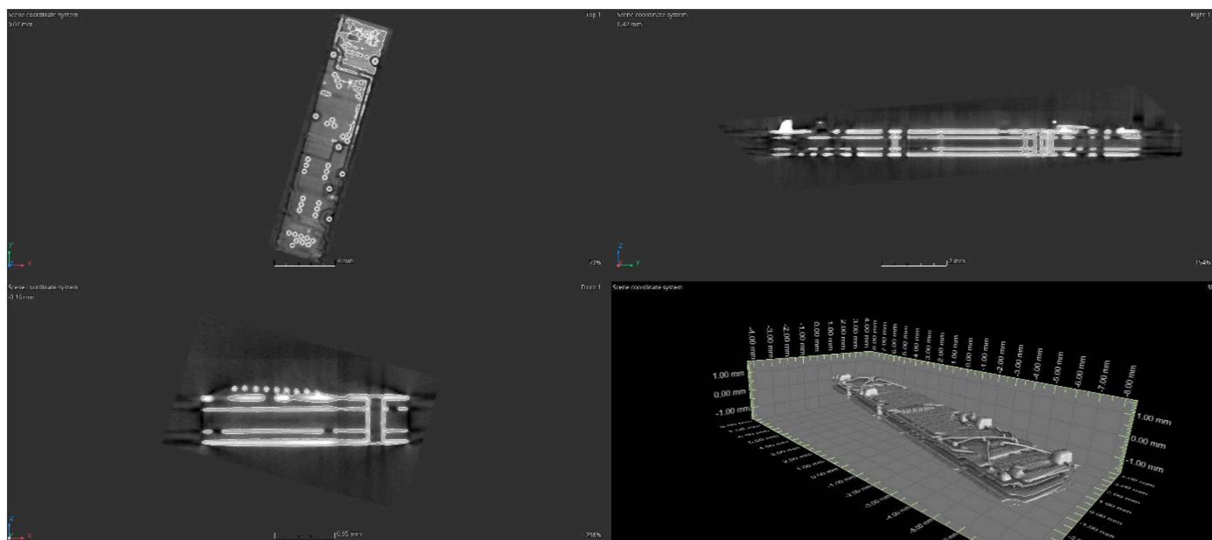

Figure 3. Basic CT images of sample.

Figure 4 shows the porosity analysis result. Porosity analysis is essential for identifying defects within samples and is closely linked to their durability.

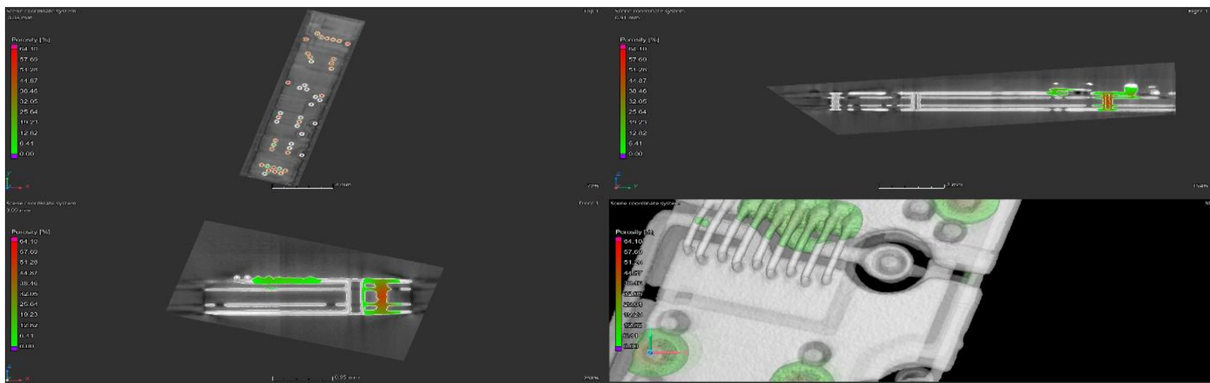

Figure 4. Porosity analysis images.

Traditional surface measurement tools, such as optical and electron microscopes, are less effective for porosity analysis compared to internal analysis using X-ray transmission. Porosity is calculated as the ratio of the total volume of the material to the pore volume. A porosity level of 20% or less is generally considered acceptable for maintaining durability. However, in this sample, numerous areas exhibited porosity levels exceeding 50%, indicating significant room for improvement. High porosity was particularly observed at the wire connection points and the internal metal connections of the PCB, as highlighted in red. These findings suggest that the sample requires substantial enhancements to meet durability standards. The ability to conduct detailed porosity analysis using CT imaging is crucial for ensuring the reliability and performance of semiconductor packages. By identifying and addressing areas with high porosity, manufacturers can improve the overall quality and longevity of their products. This underscores the importance of optimizing CT measurement conditions and developing more sophisticated analysis techniques to achieve accurate and reliable results. Figure 5 shows the defect analysis result. The software provides detailed measurements of defect size, shape, and distribution, which are essential for thorough quality control and failure analysis.

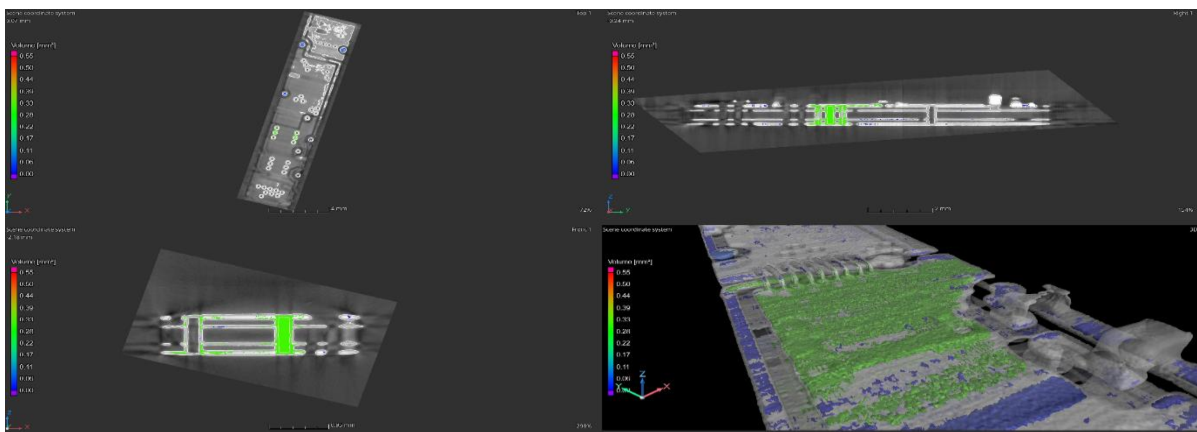

Figure 5. Defect analysis images.

These precise measurements enable manufacturers to identify and address defects early in the production process, thereby improving the overall reliability and integrity of their products. The defect analysis algorithm uses porosity data to identify defect indications. It compares shading value differences with the surrounding material. Areas where this difference exceeds an absolute threshold value are marked as defect indications.

Figure 6 shows the wall thickness analysis result. The wall thickness analysis is a critical aspect of evaluating the structural integrity of components, particularly in relation to their size. This analysis focuses on

the relative size associated with the smallest local wall thickness, providing a detailed understanding of the material's distribution and potential weak points. By conducting this analysis, it is possible to quickly identify specific areas within the sample that may require further attention or adjustment. Moreover, the wall thickness analysis plays a vital role in ensuring the reliability and performance of the final product. Nondestructive analysis techniques allow for the examination of via holes, bumps, and wiring to verify that these elements have been processed according to design specifications. This verification process is crucial for maintaining the integrity of the semiconductor package, as any deviations from the design can lead to failures or reduced performance. Through the wall thickness analysis, manufacturers can ensure that each component meets the required standards, thereby enhancing the overall reliability of the product. This approach not only helps in identifying potential issues early in the production process but also contributes to the continuous improvement of manufacturing techniques. As a result, the use of wall thickness analysis in semiconductor packaging is a valuable tool for achieving high-quality, reliable products that meet the stringent demands of modern technology.

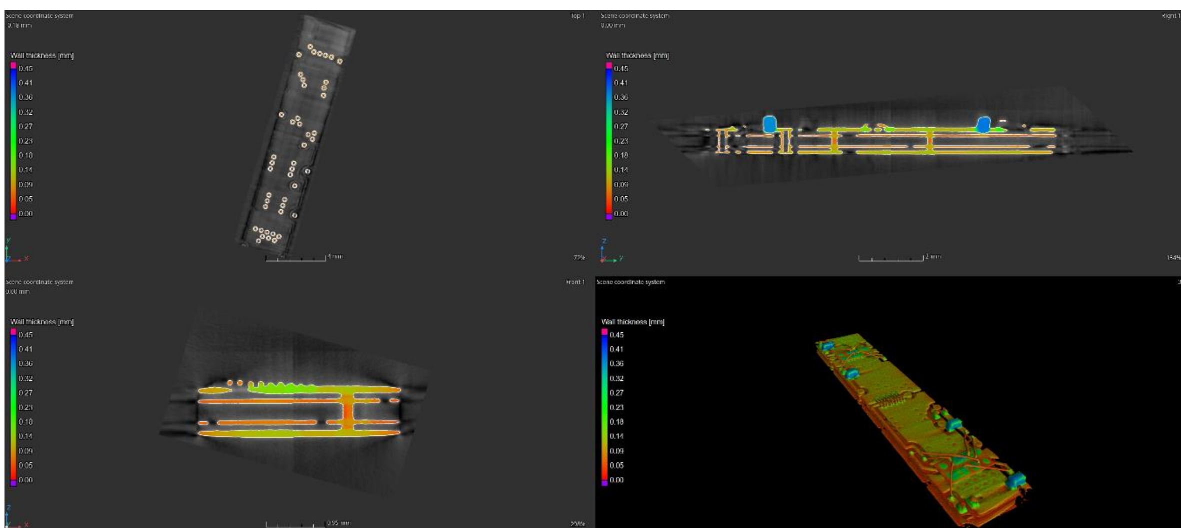

Figure 6. Wall thickness analysis images.

Figure 7 shows the material analysis result. After selecting the sample area, the maximum porosity or minimum inclusion shading values are specified to indicate the types of materials presents in the sample. One can find the same material throughout the comprehensive compositional analysis of the sample.

Material analysis can be utilized independently, but it is particularly beneficial when combined with other analyses such as porosity, defect, and wall thickness analysis. This integrated approach enhances the overall understanding of the sample, providing a more detailed and accurate assessment of its properties and potential issues. Utilizing various analysis methods allows for a comprehensive understanding of the sample′s composition and structural integrity. This approach facilitates more informed decision-making and enhances quality control.

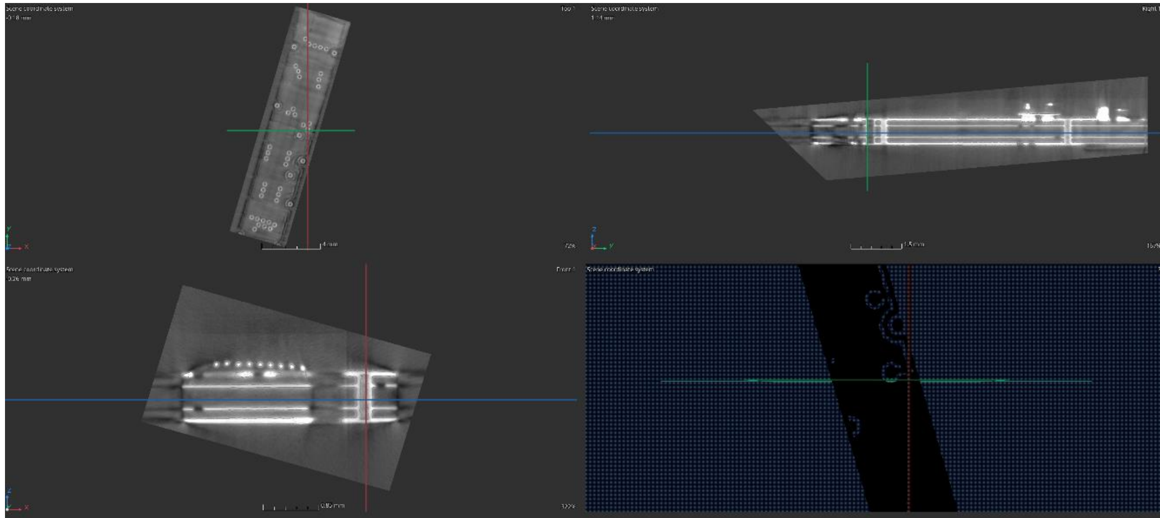

Figure 7. Material analysis images.

3. Conclusion

The role of packaging technology for semiconductor devices in communication equipment has evolved significantly. It is no longer just about protecting circuits; it has become a crucial technology for overcoming the limitations of device miniaturization and enhancing performance. This evolution is driven by the need to integrate more functions and achieve higher density in semiconductor devices. There is a noticeable trend towards advanced packaging technologies that move away from traditional lead frame and solder ball-based methods. These new technologies aim to achieve multifunctionality and high integration simultaneously. The packaging technologies for semiconductor devices used in communication equipment have diversified to meet various market demands, including different application fields and cost considerations. The market for advanced packaging technologies is expected to grow significantly in the future. Packaging technologies do not completely replace existing ones but continue to evolve through the development of new materials and processes for each specific technology.

The importance of nondestructive testing for inspecting defects and performance in semiconductor packaging products has increased. This is crucial for ensuring the reliability of the products after production. Packaging technologies are diversified according to their application fields, making the market entry barrier relatively lower compared to front-end semiconductor processes. Therefore, the development of nondestructive testing technologies to support packaging technology development is essential. In the communication equipment industry, semiconductors are transitioning to a paradigm of manufacturing multifunctional and highly integrated devices to achieve low power consumption and high performance. The co-development of semiconductor packaging technologies is essential for maximizing the efficiency of semiconductor memory and other chips, as well as for developing new chips. Providing fast and accurate nondestructive analysis of semiconductor packaging will play a significant role in supporting the growth of the communication equipment industry.

Acknowledgement

This research was supported by "Regional Innovation Strategy (RIS)" through the National Research Foundation of Korea(NRF) funded by the Ministry of Education(MOE) (2021RIS-001)

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