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우주항공 응용을 위한 내방사선 10T SRAM

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Radiation-Hardened 10T SRAM Cell for Aerospace Applications

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요 약

우주 방사선은 전자 장치의 신뢰성에 상당한 위협을 주고있다. 우주 방사선은 주로 태양에서 방출되는 고에너지 입자등으로 구성되며, 우주의 진공 상태에서는 이러한 입자를 흡수하거나 분산시킬 보호 장치가 부족하다. 이러한 고에너지 입자에 노출되면 반도체 장치, 특히 메모리 장치에 치명적인 손상을 일으킬 수 있으며, 이는 우주 산업 전반에 심각한 영향을 미칠 수 있다. 따라서 본 논문에서는 우주 방사선 환경에서 높은 신뢰성을 유지할 수 있는 새로운 메모리 비트 셀 설계 방식을 제안한다.

ABSTRACT

Cosmic radiation poses a significant threat to the reliability of electronic devices. Cosmic radiation mainly consists of high-energy particles emitted from the sun, and there is no protection device to absorb or disperse these particles in the vacuum of space. Exposure to these high-energy particles can cause fatal damage to semiconductor devices, especially memory devices, and this can have serious implications for the entire space industry. Therefore, in this paper, we propose a new memory bit cell design method that can maintain high reliability in a space radiation environment.

키워드

Aerospace, Radiation, SEU, SRAM

Ⅰ. Introduction

The modern space industry and space exploration are becoming increasingly complex and require a high level of reliability and durability for electronic devices used in spacecraft and satellites. In particular, radiation in space environments can have a devastating effect on electronic devices, so reinforcement technology is essential to overcome this. Space radiation is composed of high-energy particles, which can cause malfunctions of semiconductor devices. These malfunctions can lead to data loss and system errors.

Traditional radiation enhancement technologies have mainly relied on physical shielding and software error correction methods. However, these

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methods are inefficient in terms of the weight and cost of the equipment, and are not particularly suitable for the latest space exploration equipment, which is miniaturized and lightweight. Therefore, the design of new semiconductor devices with radiation resistance is required.

The proposed 10T bit-cell provides higher durability and reliability compared to other architectures used so far, and is particularly robust against Single Event Upset(SEU) errors caused by radiation. This is because it utilizes additional transistors to enable stable operation. In addition, SRAM cells are widely used to design storage blocks for digital processing systems such as cache memory and register files. Therefore, they occupy a large part of the processor [1], [2].

SEU and other similar Single Event Effects (SEE) are considered when designing for space applications and also high radiation environments; however, due to the reduction of Qcrit with technology scaling, SEU can also occur in standard terrestrial environments at non-negligible rates [3]. Architectural solutions, such as error correction (ECC), are often not effective for small arrays in ultra-low power systems operated at low supply voltages, due to their complexity and performance requirements. Technology solutions, such as SOI, can improve the data reliability but do not entirely solve the SEE problems, and often volume manufacturing is not feasible.

In this study, we intend to design a 10T-architectured bit-cell that is highly durable in a space radiation environment and evaluate its performance. To do this, we will first analyze the operating mechanism of electronic devices in a radiation environment and discuss the design principles of the 10T-architectured bit-cell and its superiority. Subsequently, we will verify the performance of the proposed bit-cell through simulation and experiment and demonstrate its superiority through comparison with existing technologies.

II. Proposed Architecture

2.1 Single Event Upset(SEU) Operation

SEUs occur when an energetic particle hits and passes through a semiconductor material, potentially causing a bit-flip in the memory cell [4]. SEU is a kind of soft error, which means that the logical state of data is temporarily changed, not the physical damage of the memory cell.

A SEU, changing the data value stored in the SRAM cell, happens when the charge deposited by a particle strike at a hit node is greater than Qcrit. Qcrit is proportional to supply voltage as well as to the node capacitance and is an accepted metric used to evaluate SEU occurrence [5].

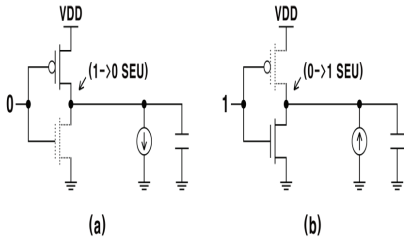

Fig. 1 (a) 1->0 SEU, (b) 0->1 SEU

Figure 1 shows an equivalent circuit for the simulation of 1->0, 0->1 noise by particle collisions. To construct negative noise, a current such as 1->0 is injected into the drain of the NMOS. Similarly, to construct positive noise, a current such as 0->1 is injected into the drain of the PMOS.

2.2 Proposed Bit-Cell architecture

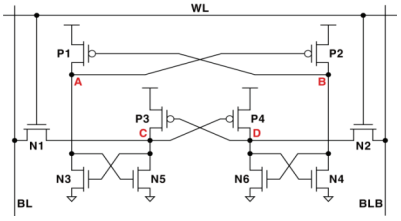

Fig. 2 Proposed 10T bit-cell schematic

Proposed 10T bit-cell is shown in Fig. 2. The proposed 10T architecture is designed by additionally placing PMOS (P1), PMOS (P2), NMOS (N3), and NMOS (N4) in the existing 6T architecture. The added transistor operates as a feedback circuit inside, enabling the recovery of the SEU by cosmic radiation. It also increased the efficiency of 10T bit-cell by properly adjusting the width of PMOS and NMOS transistors.

Table 1. Transistor sizes

Cell Type	Transistor Sizes
Nwise	$W_{P1}=W_{P2}=200nm$, $W_{N1}=W_{N2}=200nm$, $W_{N3}=W_{N4}=170nm$, $W_{N5}=W_{N6}=W_{N7}=W_{N8}=120nm$
Pwise	$W_{P1}=W_{P2}=120nm$, $W_{P3}=W_{P4}=400nm$, $W_{P5}=W_{P6}=300nm$, $W_{N1}=W_{N2}=W_{N3}=W_{N4}=120nm$
SRAM_6T	$W_{P1}=W_{P2}=120nm$, $W_{N1}=W_{N2}=200nm$, $W_{N3}=W_{N4}=120nm$,
Quatro	$W_{P1}=W_{P2}=W_{P3}=W_{P4}=120nm$, $W_{N1}=W_{N3}=200nm$, $W_{N2}=W_{N4}=150nm$, $W_{N5}=W_{N6}=120nm$
RHBD	$W_{P1}=W_{P2}=120nm$, $W_{P3}=W_{P4}=200nm$, $W_{P5}=W_{P6}=340nm$, $W_{N1}=W_{N2}=180nm$, $W_{N3}=W_{N4}=120nm$
Proposed 10T	$W_{P1}=W_{P2}=170nm$, $W_{P3}=W_{P4}=150nm$, $W_{N1}=W_{N2}=120nm$, $W_{N3}=W_{N4}=120nm$, $W_{N5}=W_{N6}=200nm$

Transistor capacitances are combinations of extrinsic, intrinsic, and overlap parts, mostly dependent on the bias and geometry of transistors. Table 1 shows the width of the bit-cell individual transistors for comparison with the proposed 10T bit-cell architecture. Increasing the efficiency of the bit-cell by adjusting the width of the transistor is one of the important technologies for optimizing the performance of semiconductor devices. The width of the transistor refers to the width of the channel through which current flows. Increasing the width of the transistor increases the current capacity, improving the transistor's drive capability. Conversely, narrowing the width can reduce power consumption. These adjustments can be performed fluidly to optimize the performance of the transistor.

In the proposed 10T bit-cell architecture, the width of NMOS (N1) and NMOS (N2), which are the access transistor that determine the status with the WL signal and receive the signals of BL and BLB first, was set to 120nm, the minimum value available in this process, to reduce the power consumption of the access train.

2.3 Read&Write Operation

All operations in the 10T SRAM use a set of 1 columns with bit-cell and peripheral circuits with pre-charge circuits, write circuits, and output sense amplifiers. During Read operation, both capacitors in BL and BLB are pre-charged to Vdd using the Pre-charge circuit. WL is set to High as well as the active state for Read operation. Suppose node C is set to "0". The left side of the bit-cell shows Vds=Vdd and there is some current flow in that area. Therefore, the charge of the capacitor is reduced little by little. Finally, a signal is created in BL and BLB and sent to the sense amplifier, where the sense amplifier acts as a comparator to sense the signal.

During Write operation in 10T SRAM, BL is pre-charged to Vdd and BL remains floating. Suppose either "1" or "0" is stored at node C. The Access Transistor is operated by WL and the data stored inside changes accordingly. The lines entered as data are BL and BLB. Therefore, the values stored at node C change depending on the values entered at BL and BLB.

III. SEU Recovery Simulation

3.1 SEU Simulation

The SEU simulation of the internal nodes A, B, C, and D of the proposed 10T architecture was conducted. Figure 2 shows that the proposed bit-cell architecture's internal nodes are A, B, C, and D. In order to prove that 0 ->1 SEU and 1->0 SEU recovery are possible in a total of 4 nodes, the results shown in Figures 3 and 4 are presented. In both graphs, it was confirmed that SEU occurred at the 10ns part and all signals were recovered normally within 2ns thereafter.

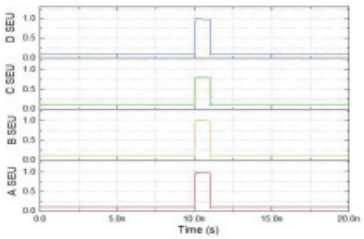

Fig. 3 Node to 0->1 SEU Simulation

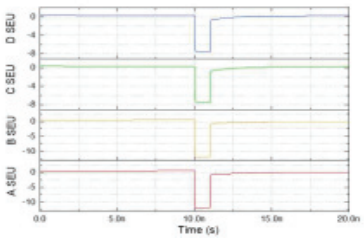

Fig. 4 Node to 1->0 SEU Simulation

Ⅳ. Performance Comparison

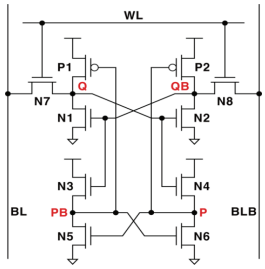

Fig. 5 Nwise circuit

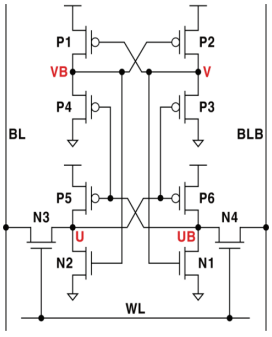

Fig. 6 Pwise circuit

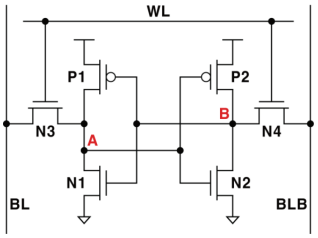

Fig. 7 SRAM_6T circuit

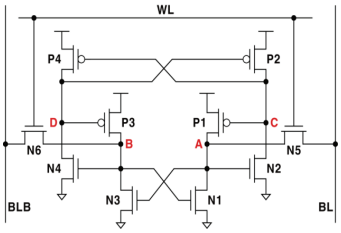

Fig. 8 Quatro circuit

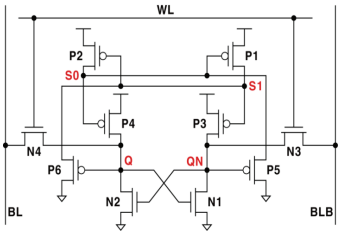

Fig. 9 RHBD circuit

Figure 5, 6, 7, 8, and 9 are circuit diagrams of bit-cell architectures that have been presented in other papers or are commonly used.

4.1 Area comparison

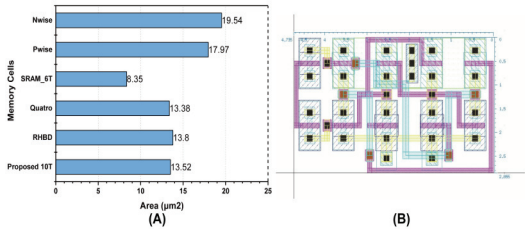

Fig. 10 (A) Bit-cell area comparison, (B) Proposed 10T area

Figure 10 (A) shows bit-cell area comparison with previous architectures. The SRAM_6T [6], Quatro [7], RHBD [8], [9], and Nwise and Pwise [10] bit-cell architectures are compared. The Nwise and Pwise bit-cells have high area consumption due to internal feedback.

4.2 Power consumption comparison

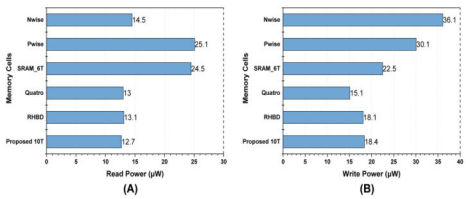

Fig. 11 (A) Read power, (B) Write power

Figure 11 (A) is a graph comparing the maximum power consumption when a read operation is performed within a single bit-cell. A large number of transistors increases the power consumption, and a small number of transistors decreases the power consumption. According to this logic, the SRAM_6T with six transistors should have the lowest read power consumption. However, we can see that SRAM_6T has the second largest read power consumption of 24.5 μW. You can find out why by checking the contents in Table 1. The power consumption of the bit-cell depends not only on the number of transistors but also on the width of each transistor. In addition, we can see that the read power consumption of Quatro, RHBD, and proposed 10T using the same number of transistors is different. This indicates that the proposed 10T bit-cell is performantly superior. Figure 11 (B) is a graph comparing the maximum power consumption when a write operation is performed within a single bit-cell. As with the read power consumption, we can see that the proposed 10T bit-cell's performance is compliant.

4.3 Access time comparison

Access Time refers to the time taken by SRAM to read or write data. This is one of the important indicators of memory performance, indicating how quickly a memory device can provide data. Access Time can generally be divided into two main components: Read Access Time and Write Access Time.

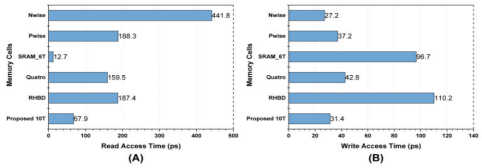

Fig. 12 (A) Read access time (B) Write access time

Figure 12 (A) is a comparison graph of Read Access Time. The proposed 10T's Read Access Time was 67.9 ps, the second lowest. The lower the Read Access Time, the less time it takes to read data from memory cells, indicating that the proposed 10T's read performance is more compliant than other bit-cells. Figure 12 (B) shows a comparison of Write Access Time. The proposed 10T's Write Access Time was 31.4ps, which is the second lowest number, like Read Access Time. Write Access Time represents the time it takes to write data to a memory cell. Similarly, you can see that the proposed 10T's write performance is superior to other bit-cells.

Table 2. Performance summary

	Nwise	Pwise	SRAM_6T	Quatro	RHBD	Proposed
CMOS Technology	90nm	90nm	90nm	90nm	90nm	90nm
Cell Type	10T	10T	6T	10T	10T	10T
Area(μm^2)	19.54	17.97	8.35	13.38	13.8	13.52
Read Power(μW)	14.5	25.1	24.5	13	13.1	12.7
Write Power(μW)	36.1	30.1	22.5	15.1	18.1	18.4
Read Access Time(ps)	441.8	188.3	12.7	159.5	187.4	67.9
Write Access Time(ps)	27.2	37.2	96.7	42.8	110.2	31.4
RSNM(mV)	230	270	150	210	180	382
WSNM(mV)	400	180	340	460	140	404
FoM	7.48	5.11	90.22	53.88	3.73	229.11

4.4 Static noise margin comparison

Static noise margin is a critical indicator for evaluating the stability of memory cells, especially SRAM cells. The SNM represents how much memory cells can withstand external noise or voltage fluctuations, and plays an important role in ensuring stable data storage and read/write.

SNM is usually measured using the voltage transfer characteristic curve (VTC). After drawing the VTC of the two inverters, define SNM by the size of the largest square of the "butterfly curve" formed at their intersection. Larger areas of these squares allow memory cells to have higher noise margins and operate more reliably.

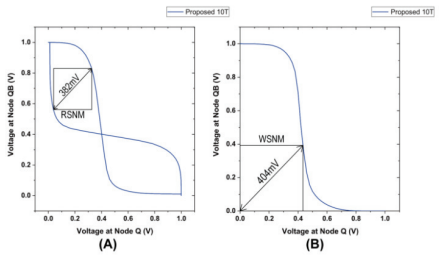

Fig. 13 (A) Proposed 10T RSNM
(B) Proposed 10T WSNM

Figure 13 (A) is a graph measuring the RSNM of proposed 10T and measured at 392 mV. Figure 13 (B) is a graph measuring the WNSNM of proposed 10T and measured at 404 mV.

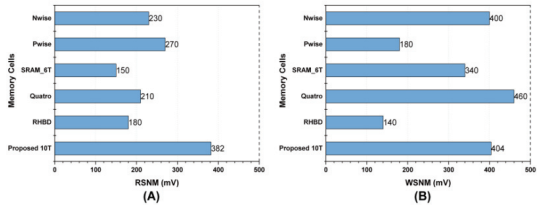

Fig 14. (A) RSNM Comparison (B) WSNM Comparison

Figure 14 (A) is a comparison graph of RSNM. It can be seen that RSNM has the best performance of proposed 10T at 382 mV compared to other bit-cell. Figure 14(B) is a comparison graph of WNSNM. WNSNM did not have the best performance of proposed 10T compared to other bit-cells. Performance summary is represented in Table 2.

4.5 FoM Comparison

Equation 1. shows Figure-of-Merit(FoM) of radiation-hardened SRAM cell.

$$\frac{WSNM \times RSNM}{P_{Write} \times P_{Read} \times AT_{Write} \times AT_{Read} \times Area} \quad \cdots(1)$$

The FoM of the proposed 10T bit-cell is approximately 230. Based on this FoM analysis, it can be seen that the proposed 10T bit-cell has high-level performance.

Ⅴ. Conclusions

In this paper, we developed a 10T-architectured SRAM bit-cell resistant to space radiation and evaluated its performance. The proposed bit-cell showed superior radiation resistance compared to other previously devised architectures, which demonstrated its potential as a reliable data storage device in space environments.

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