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40MHz에서 1.6 dB 최소잡음지수를 얻는 잡음소거 기술에 근거한 광대역 저항성 LNA

최 광 석*

Wideband Resistive LNA based on Noise-Cancellation Technique Achieving Minimum NF of 1.6 dB for 40MHz

Choi Goangseog

〈Abstract〉

This Paper presents a resistive wideband fully differential low-noise amplifier (LNA) designed using a noise-cancellation technique for TV tuner applications. The front-end of the LNA employs a cascode common-gate (CG) configuration, and cross-coupled local feedback is employed between the CG and common-source (CS) stages. The moderate gain at the source of the cascode transistor in the CS stage is utilized to boost the transconductance of the cascode CG stage. This produces higher gain and lower noise figure (NF) than a conventional LNA with inductor. The NF can be further optimized by adjusting the local open-loop gain, thereby distributing the power consumption among the transistors and resistors. Finally, an optimized DC gain is obtained by designing the output resistive network. The proposed LNA, designed in SK Hynix 180 nm CMOS, exhibits improved linearity with a voltage gain of 10.7 dB, and minimum NF of 1.6 - 1.9 dB over a signal bandwidth of 40 MHz to 1 GHz.

Key Words : LNA, Noise Cancellation, NF, CMOS, SoC

Ⅰ. Introduction

Many efforts have been exerted, to overcome the challenge to implement fully integrated Chip for TV tuner applications in a system-on-Chip (SoC). The TV tuner standards demand services for the wideband of 40MHz to 1GHz. The LNA remains an unavoidable and critical block. Due to the first active building block in TV tuners, the low-noise-amplifier (LNA) needs to have enough gain, high linearity, low noise-figure (NF), and good input/output matching over the signal bandwidth. As the LNA for TV tuner ranging from

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40MHz to 1 GHz, the performance of the required LNA should have sufficiently high gain and low NF for higher sensitivity. Recent literature on wideband LNA with off-chip balun have shown good performance like low NF, high linearity and excellent matching [1,2]. The on-chip balun results in large die area and not be acceptable for low frequency and wideband applications. Also, a single-to-differential stage is adopted in order to replace the balun for less area without degrade the performance[3-6]. The wideband LNA design approach for TV tuner can be either with inductors or inductorless. Also, inductors, needed in RF circuit design, are bottleneck to achieve small area and do not scale well with low power digital CMOS technology. The wideband LNA design constrained by few of the concerns: achieving high gain, input matching and low NF.

In nanoscale CMOS technologies, the transistors must have excellent f_T, to serve as wideband LNAs with low NF, high gain, and high linearity. The resistive LNAs are useful in many applications. The LNAs should accommodate large signals without distortion and offer matching to their input and output networks.

This paper presents a wideband resistive LNA design for a signal bandwidth of 40 MHz to 1 GHz. Simulations are performed to discuss, in detail. A two-stage design is selected, wherein the front-end stage employs a cascode CG configuration, and the second stage uses a CS configuration to achieve noise cancellation. The third stage is composed of output drivers that implement a CS configuration and local feedback.

Ⅱ. Resistive Feedback LNA Design

Many studies have been conducted on LNAs, with and without inductors, designed in nanoscale CMOS technologies. A linear wideband LNA using current amplification for digital TV tuner applications was designed. In this design, to improve the linearity and exploit the noise-cancellation effects, a CG stage with positive current feedback was integrated in parallel with the CS stage, using a current-mirror amplifier. It also helped to achieve high gain and good linearity. The LNA exhibited a power gain of 20.5 dB, input referred third-order intercept point (IIP3) of 2.7 dBm, and input referred second-order intercept point (IIP2) of 43 dBm. The proposed design had an active core area of 0.12 mm^2, dissipated 32.4 mW power, and exhibited an average NF of 3.3 dB, for a supply voltage of 1.8 V in 0.18 μm CMOS technology [7]. A current-reusing technique utilizing transconductance g_m-boosting was used to design a resistive LNA to achieve a gain of 21 dB with an NF of 2.6 dB at 5 GHz. The design could also achieve an output-IP3 of 12.3 dBm at 5 GHz, and had an active core area of 0.012 mm^2 [8].

A CG configuration, while being suitable for input matching, does not provide high gain. A self-biased g_m-boosted CG technique presented by utilizing active-feedback to boost the transconductance of the CG to reduce noise and improve input power matching. However, the circuit contained a large inductor, and it was difficult to integrate it for system-on-chip applications. It could achieve a minimum NF of 4 dB and an IIP3 of −11.3 dB, while

dissipating 10 mW from a supply voltage of 1.8 V and had an active core area of 0.11 μm^2 [9].

Another g_m-boosted CG LNA on the system-on-chip applications was reported. This technique could improve the performance of the LNA by using a g_m-boosted CG configuration, in 0.18 μm CMOS technology, to achieve good noise reduction and allowed easy integration on chip [10].

An inductor-less double g_m-enhancement technique was used to reduce the power for wireless sensor networks for signal bandwidths of 2.45 GHz. This technique was provided high gain and reduced NF, despite the low intrinsic g_m of the transistors used in nanoscale CMOS technology. It achieved a gain of 20 dB with an NF of 4 dB while dissipating 1.32 mW power. The proposed circuit included a CG circuit, which was g_m-boosted by another CG circuit, instead of a CS amplifier. Both active and passive g_m-boosting effects were used to achieve a very low NF of 4 with high voltage gain. It had good stability as well as a very small active core area of 0.007 mm^2 implemented in 0.13 μm CMOS technology [11].

The source degeneration topology used in the cascode amplifier was proposed to design an efficient LNA for wideband applications. A cascode amplifier was employed with large inductors at the output and input for accurate matching. This allowed the use of a generic input matching network and could achieve very low NF for signal bandwidths of 3.2 to 4.8 GHz. The circuit was implemented in 0.25 μm CMOS technology, and exhibited a power consumption of 20 mW. Using a quasi-static transistor model, the proposed technique showed that the minimum NF could be made independent of the transistor width by properly selecting the source degeneration reactance. The measured NF ranged from 2.7 dB to 3.7 dB, over a signal bandwidth of 3.2 to 4.8 GHz [12].

A CG amplifier with capacitor cross-coupled technique was proposed to design an LNA in 0.18 μm CMOS. The fully integrated capacitor cross-coupled LNA validated the g_m-boosting technique. Although the voltage gain was only 7.1 dB, the proposed design could achieve an NF of 3 dB at 6 GHz and consumed only 3.6 mW from a 1.8 V supply [13].

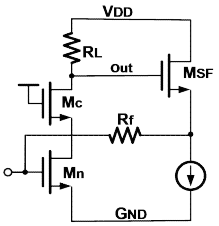
A fully integrated ultra-wideband LNA with systematic design methodology was proposed. The feedback technique was proposed to attain a better design trade-off between gain and noise. A fully integrated wideband design could achieve an NF lower than 3.8 dB from 3 to 7.5 GHz, and the circuit had a total active core area of 1.37 × 1.19 mm^2 [14].

Due to the reason of better bandwidth, linearity, and stability of the CG topology, compared to the CS topology, capacitor-cross-coupled negative feedback was used to boost the g_m of the CG stage to achieve high gain and low NF without sacrificing the bandwidth and linearity. The proposed design could achieve maximum voltage gain of 21 dB, and a minimum NF of 2dB with power consumption of 3.6mW for a signal bandwidth of 300MHz to 920MHz [15].

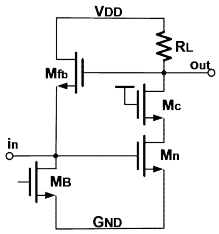
An inductor-less low-power g_m-boosted design based on CG could achieve a high gain of 22 dB and minimum NF of 7 topology was proposed. The circuits combined gain-boosting techniques to achieve high gain. It could achieve a voltage gain of 20 dB and NF of 4, with a layout active core area of 0.007 mm^2 for a signal bandwidth of 0.1 GHz to 2.7 GHz, using the 0.13 μm CMOS technology [16].

A low-power wideband LNA was designed for a

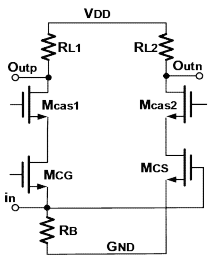
signal band of 0.01 to 1.4 GHz. The input stage, consisting of a CG NMOS transistor, CS shunt-feedback PMOS transistor, and resistor, employed the shunt－shunt feedback topology to achieve wideband input impedance matching. Compared to simple CG or CS stage resistor architectures, the CG shunt－shunt feedback topology could achieve a 50 input impedance matching with much lower power consumption. The proposed structure dB, with a power consumption of only 0.9 mW from a supply voltage of 1.8 V. The circuit had an active core area of 0.03 mm^2 and was implemented using the 0.18 μm CMOS technology [17].



〈Figure 1〉 Resistive feedback topology



〈Figure 2〉 Active feedback topology



〈Figure 3〉 Common-gate(CG) Common-source(CS) topology

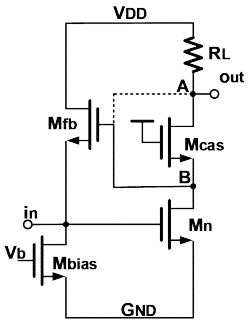
Important part of LNA design is impedance matching. Figure 1 shows the resistive feedback provides good impedance matching for the CS configuration [18, 19]. The active feedback shown in Figure 2 also provide good performance [20]. The feedback is provided from the output of the LNA to the input. In the case of the active feedback, the condition for impedance matching can be expressed as,

$$R_s = \frac{1}{g_{mfb}(1 + A_v)} \quad (1)$$

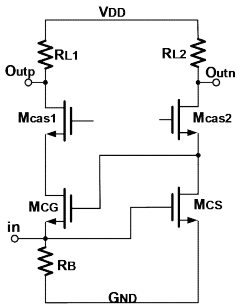
A_v is the open-loop gain at the output node. The impedance degrades due to gain roll-off at higher frequencies, as the feedback signal is taken from the output, which has high gain and low bandwidth.

Another approach using a CG-CS topology, combined with noise-cancelling, exhibits good impedance matching and low NF as shown in Figure 3 [20]. The g_m of CG is set for 50 Ω impedance matching. Although the output balancing and noise-cancelling of the CG transistor can achieve good performance given the condition of g_{mCG} R_{L1} = $g_{mCS}R_{L2}$, this topology demands higher supply voltage to reduces the NF, which is challenging in nanoscale CMOS designing. In CS-feedback topology, the output node of the LNA is overburdened by the limited bandwidth and large gain. To overcome this issue, a local feedback approach is proposed to replace global feedback. The feedback signal is taken from the source of the cascode transistor at point B, instead of from the output at point A, as shown in Figure 4. Because of the high bandwidth at point B, the local feedback will be effective at high frequencies. To address the problem of the CG－CS LNA shown in Figure 3, the same local feedback can be applied to boost the CG transistor, as shown in Figure 5. The CG transconductance benefits

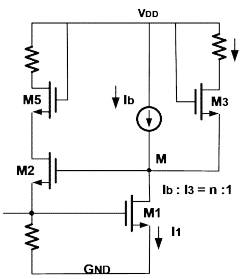
from negative feedback and is boosted by a factor. The current of the CG can also be reduced by the same factor, and much large resistor can be adopted. This topology can be used to implement the noise-cancellation in the CG transistor. To further improve this topology, a current source is proposed to be add in parallel to M_3 as shown in Figure 6.



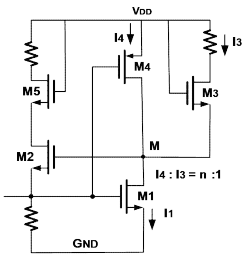
〈Figure 4〉 CS topology with local feedback



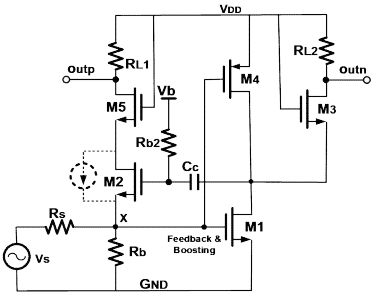
〈Figure 5〉 CG-CS topology with local feedback



〈Figure 6〉 Local feedback from current source



〈Figure 7〉 Cascode CG stage



〈Figure 8〉 LNA with noise-cancellation

The current source can be replaced by a PMOS, to reuse the current in the CS stage with amplification, as shown in Figure 7. The circuit employing the noise-cancellation technique, shown in Figure 8, can eliminate the noise from the main CG transistor M_2 and cascode transistor M_3. The channel noise of the transistor M_2, shown by the dotted current source, is subtracted at the output nodes outp and outn because of the two correlated but out-of-phase noise voltages at points V_X and V_{outp}. The CG stage g_m of M_2 uses the advantage from the negative feedback and is boosted by a factor $1+A_v$.

$$R_s = \frac{1}{g_{m2}(1+A_v)} \quad (2)$$

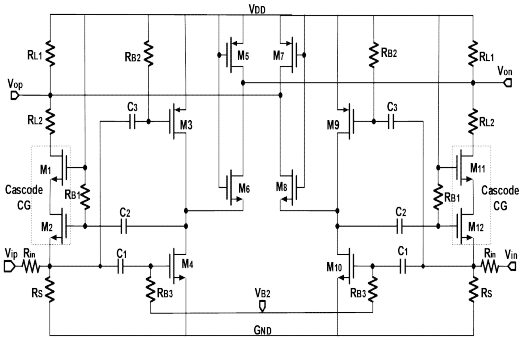
Rs is the source resistance, which is typically equal to 50Ω. The transconductance needed for input impedance matching is reduced by a factor of $(1+A_v)$. The voltage gain within the negative feedback loop is given by

$$A_v = \frac{R_{L1}}{R_s} + (g_{m1} + g_{m4})R_{L2} \quad (3)$$

The differential output will be balanced when

$$\frac{R_{L1}}{R_s} = (g_{m1} + g_{m4})R_{L2} \quad (4)$$

The equation (4) is also the condition of noise-cancellation. To improve the performance further, this work proposes using the cascode CG as an alternative to the traditional CG stage [21]. The third-stage resistor is removed completely and is replaced by a PMOS stage. The NMOS reuses the current of the PMOS stage by adjusting the width of this stage to obtain a low NF. A fully differential LNA is designed using SK Hynix 180nm CMOS, for a supply voltage of 1.8V. The DC gain of the LNA designed first, considering the target of required bandwidth and the NF. Then, the transconductance and current of the cascode CG stage adjusted according to the input impedance matching condition. The current of M4 is determined under the power constraints. Figure 9 shows the proposed differential LNA. Input matching uses 75Ω resistor for Balun matching at input while at the output have 50Ω matching with buffer. With the LNA arranged as a differential circuit, the sizing of all components is the last step to be done before the starting the simulation. The values of the passive components used in the design of LNA are shown in Table 1. The lengths of all transistors were set to 180nm in order to keep the sizes of all transistors small, to minimize and reduce the layout area.



〈Figure 9〉 Proposed LNA differential with cascode CG

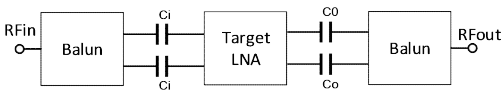
〈Table 1〉 Design values of the LNA

Component	Values
R_{in}	75 Ω
R_s	1.25 kΩ
R_{L1}	40 Ω
R_{L2}	27 Ω
R_{B1}	2.3 kΩ
R_{B2}	4.8 kΩ
R_{B3}	2.3 kΩ
C_1	10.7 pF
C_2	10.7 pF
C_3	10.7 pF

Ⅲ. Simulation Results

A fully differential LNA was designed in SK Hynix 0.18 μm CMOS, at a supply voltage 1.8V. To facilitate single-ended simulation, a single-to-differential balun was used at the input, and a differential to single-ended output balun was used at the output of LNA as shown in Figure 10. The DC gain of the LNA was implemented first, considering the targets of signal

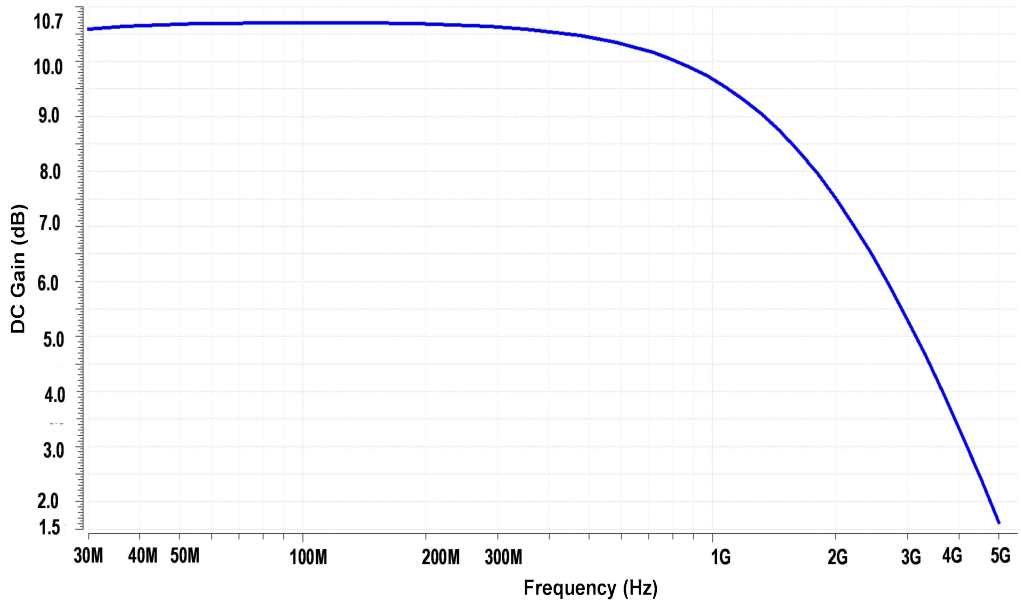
bandwidth from 40 MHz to 1 GHz and considering low NF. Figure 11 shows that a simulated DC voltage gain of 10.7 dB implementation. Table 2 shows all process corner for the DC gain of the fully differential LNA. The LNA DC gain shown to be stable as there are no sharp decrease in the DC gain at any process corner values. The simulated NF shown in Figure 12 indicates that the LNA can achieve minimum NF of 1.6 dB and a maximum NF of 2.9 dB over the signal bandwidth of 40 MHz to 1 GHz. The S-parameter simulation was also performed for signal bandwidth of 40 MHz to 1 GHz. The simulated S-parameters for the proposed LNA, with S_{21} (voltage gain of 10.7 dB) also provided. The input matching S_{11} is from －9 dB to -17 dB, as shown in Figure 13. The S12 parameter also shown in Figure 14. The layout of proposed LNA including the output buffer had an active core area of 0.12 mm^2 and as shown in Figure 15.



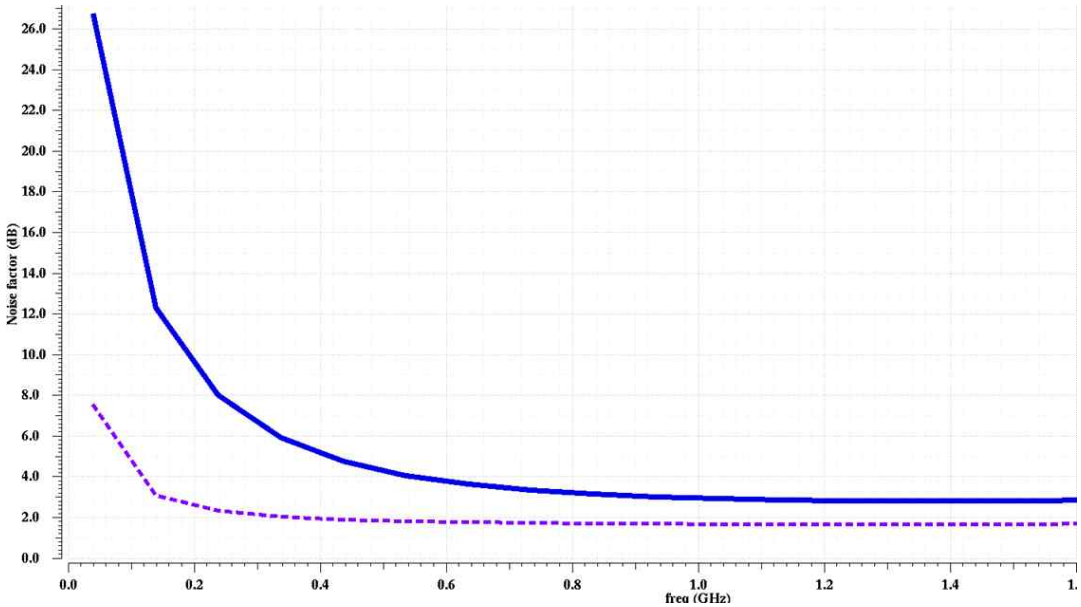
〈Figure 10〉 LNA with Balun

〈Table 2〉 LNA process corner value for Gain

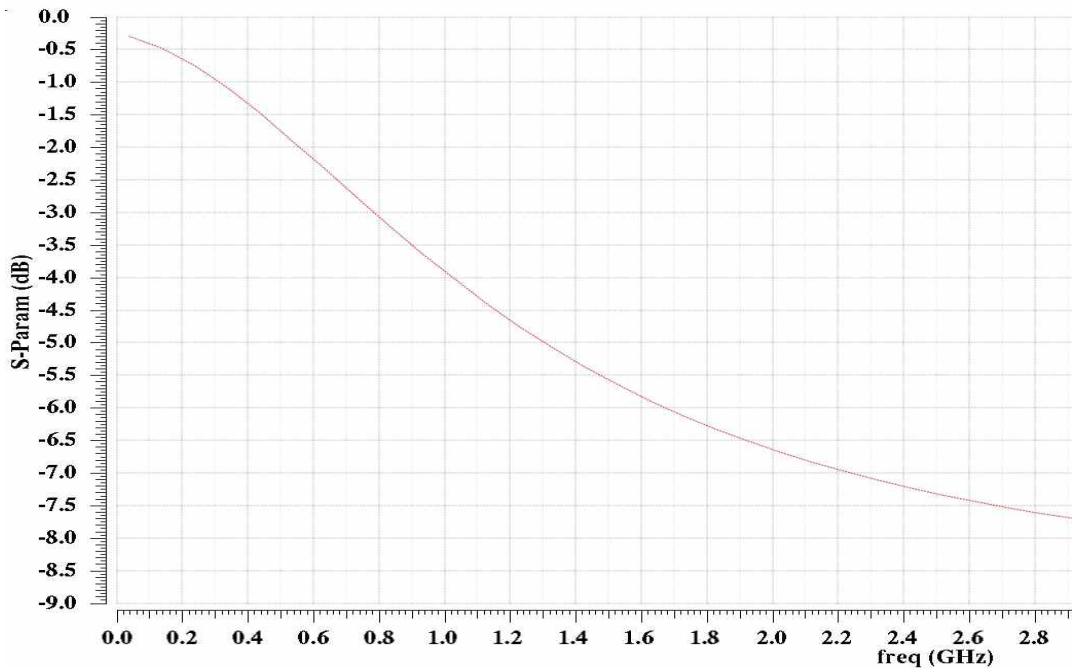
Corner	Value[dB]
TTT	10.7
FFF	9.98
SSS	12.97
SFT	12.54
FST	10.55
SFS	13.54
SFF	11.25
FSF	9.8



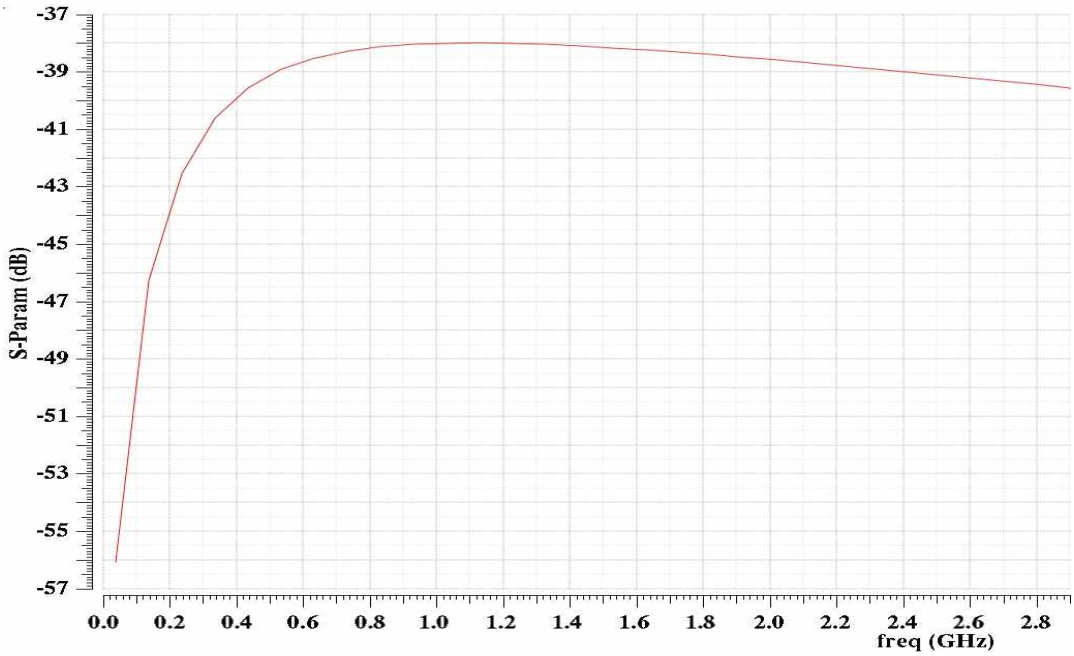
〈Figure 11〉 Simulated DC Gain



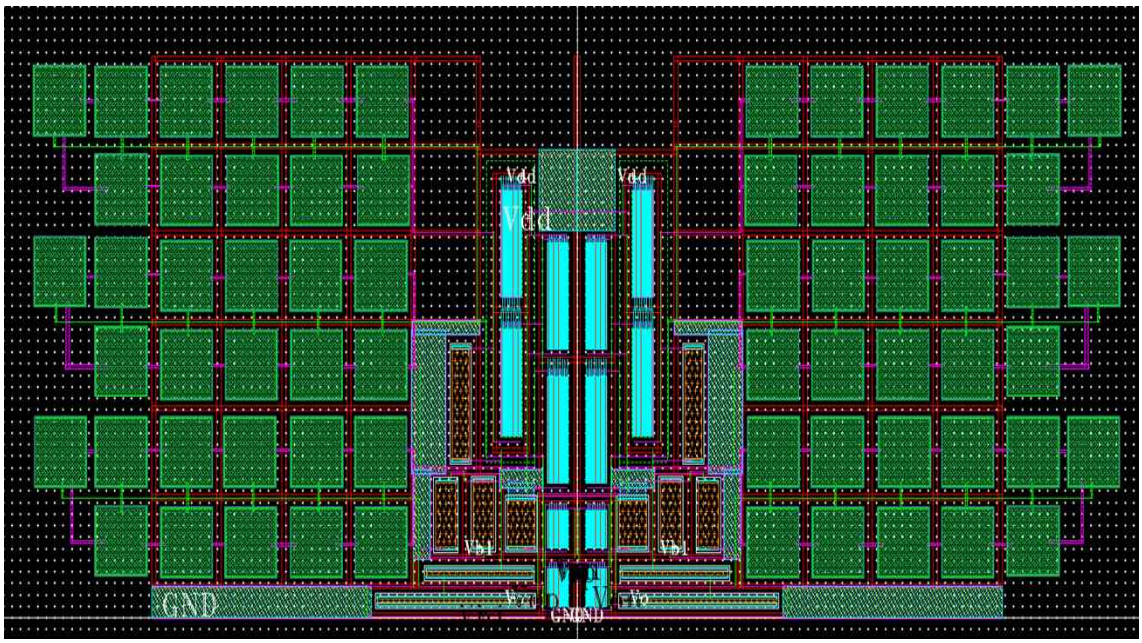
〈Figure 12〉 Simulated Noise Figure (NF)



〈Figure 13〉 S-parameter plot for S_{11}



〈Figure 14〉 S-parameter plot for S_{12}



〈Figure 15〉 Layout of the proposed LNA

Ⅳ. Conclusion

A broadband LNA was designed without using inductors, in SK Hynix 180nm CMOS for TV tuner applications. The proposed LNA implemented the noise cancellation technique by utilizing cascode CG configuration in the front-end. The second stage employed a cascade CS structure to boost the gain. In the proposed structure, thermal noise of cascode CG transistor was cancelled at the second stage, which helped the LNA achieve higher gain and much lower noise. A local cross-coupled feedback mechanism was adopted to improve the performance of the LNA. The wideband LNA achieved DC gain of 10.7 dB, minimum NF of 1.6 dB, and maximum NF of 2.9 dB at the circuit level and 2.5 dB to 3.2 dB at the post-layout simulation, for a signal bandwidth of 40 MHz to 1 GHz. The designed LNA consumed 10 mA at 1.8 V power supply and had an active core size 0.12 mm^2.

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