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Original Article

System-on-chip single event effect hardening design and validation using proton irradiation

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ABSTRACT

A multi-layer design is applied to mitigate single event effect (SEE) in a 28 nm System-on-Chip (SoC). It depends on asymmetric multiprocessing (AMP), redundancy and system watchdog. Irradiation tests utilized 70 and 90 MeV proton beams to examine its performance through comparative analysis. Via examining SEEs in on-chip memory (OCM), compared with the trial without applying the multi-layer design, the test results demonstrate that the adopted multi-layer design can effectively mitigate SEEs in the SoC.

1. Introduction

When the nanoscale System-on-Chip (SoC) is applied in a terrestrial or aerospace environment, it encounters Single Event Effect (SEE) induced by neutron, electron, proton, or heavy ion [1–5]. SEE can occur in various components in an SoC, leading to data corrupted even system breakdown [6]. Therefore, SEE hardening is urgent.

SEE can be tolerated at different levels with multiple strategies. For instance, new technology is adopted at the device level, such as FinFET [7]. A specific structure is applied at the circuit level, for example, the delay-adjustable D-Flip-Flop reported in [8]. Compared with the device or circuit level, SEE analysis and hardening are more complicated at system level.

As the Xilinx Zynq-7000 SoC is considered as a candidate option for aerospace applications, various SEE irradiation tests have been performed, involving heavy ion, proton, neutron, electrons, and others [9–14]. We took advantage of multiple irradiation facilities in China to explore SEE on the 28 nm SoC [15–22]. In [19], it reported the failure rate in the atmospheric reaches about 22 FIT/Mbit. In [17] and [20], that illustrated the low energy proton as well as MeV level electron can also induce SEEs in the device. These prove that an effective mitigation strategy against SEEs in the SoC is indeed necessary. However, as an extensively integrated system, it is challenging to apply hardening techniques through changing SoC architecture or circuit layout. It is feasible to take measures using available resources in the SoC, for example, the embedded dual-core ARM processor in the SoC. With the dual-core, applications can be executed in a lockstep or asymmetric multiprocessing (AMP) pattern accompanied by software-based hardening techniques. The lockstep pattern signifies the two cores execute instructions in a synchronized manner, while the AMP pattern suggests the dual-core can be divided into the master and the slave [23,24].

In [25], the lockstep pattern's hardening performance in the same series targets was examined. Since the lockstep pattern runs applications using the duplicated resources, the dual-core processor is fully occupied. However, the application can be divided and assigned to different cores according to different criticality levels in the AMP pattern. And master or slave core can be selectively hardened to a better trade-off between overhead and reliability. The dual-core processor in the chip makes it possible to harden SEE using the AMP pattern, but the related irradiation tests, especially combined with other mitigating measures simultaneously, have not been reported comprehensively yet. It is different from the

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traditional redundancy and tests relying on the sole processor, and it is also different from the published dual-core designs. In the current study, a multi-layer design is applied to mitigate SEEs in the 28 nm SoC based on the AMP pattern combining with redundancy and watchdog monitor.

More important, in order to examine the performance of the design, two times proton irradiation tests were performed, one with the multi-layer design and the other without it. The results regarding SEEs in the test without any hardening were reported in [18]. In [18], we discussed the SEEs induced by the secondary particles from 90 and 70 MeV protons interacting with silicon in the nanoscale SoC, too. In this manuscript, we focus on the AMP pattern combining with redundancy and watchdog monitor.

2. Multi-layer design

Numerous solutions can be applied to mitigate SEE at the system level, for example, hardware-level instrumentation, software/hardware-based redundancy techniques, and watchdog monitor. For a commercial off the shelf (COTS) SoC, it is impossible to mitigate SEE through modifying hardware. Therefore, software-based redundancy and watchdog monitor techniques are more favored.

Redundancy and watchdog monitor are traditional hardening measures against SEE in SoC. In this paper, however, we apply them cooperating with the AMP pattern utilizing the dual-core processor. It makes the slave core (Core1) dedicated to mitigating SEE to guarantee data correctness for the master core (Core0). This measure is the most significant difference and contribution of our work compared with others. In this study, Xilinx Zynq-7000 SoC manufactured with the 28 nm Complementary Metal Oxide Semiconductor (CMOS) technology is the device under test (DUT). Restricted by accelerator hours and budget, we only examined the On-Chip Memory (OCM) block during the irradiation test. Hence, the mitigation strategies described here mainly focus on OCM. It should be noticed that the adopted multi-layer design is available for all dual-core shared resources.

2.1. Redundancy layer

Redundancy means replication or repetition operations. It is a measure to mitigate Single Event Upset (SEU) and Single Event Transient (SET) utilizing spatial and/or temporal redundancy. That can be achieved from spatial or temporal backup and replication operations. Spatial redundancy, stands for repetition and more resource occupation, while temporal redundancy, underlies the repetition operations and more duty cycles. Temporal redundancy can be applied in complicated systems by repeating the same operations or instructions more than once in continuous periods. Then, comparing the results in each execution to decide the possible soft errors. In this work, both spatial and temporal redundancies are used. In spatial redundancy, data in OCM are replicated in two different double data rate (DDR) memory spaces. And data are read out from OCM and other two separate addresses and compared by a majority voter during checking. Fig. 1 shows the architecture of spatial triple modular redundancy for OCM data in this layer.

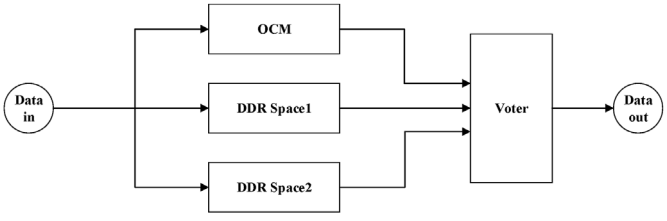

Fig. 1. Architecture of spatial triple modular redundancy for OCM data.

Besides spatial redundancy, we also take advantage of temporal redundancy to guarantee data correctness in OCM. For a datum in OCM, The processor reads three times consecutively in three cycles to decide a datum status. It better detects that data upsets occur between two consecutive access cycles to the same datum. For instance, the same datum in the previous period is correct, while encounters upset in next period accessing. The temporal redundancy can react in this case immediately. In this layer, temporal redundancy takes precedence over spatial redundancy. It means temporal redundancy is firstly used to determine data correctness. If the datum is not correct during the temporal redundancy examination, it does not enter the spatial redundancy check. This way, it saves time cycle to detect the corrupted data, because the redundant data are stored in DDR and accessing them extends the read routine and time. For an example, for a datum, if it is reported an incorrect one by temporal redundancy directly, following read back, comparison, and give a judgement, it takes about 1 μs However, it is about 2 μs employing temporal redundancy and spatial redundancy checking together. Then, for the data considered correct by temporal redundancy, it will step into spatial redundancy examination to eliminate misjudgment on the data corrupted before reading.

2.2. Watchdog monitor layer

For the SoC, Single Event Functional Interruption (SEFI) events can disturb the processor's proper running or function, leading to a program exception. The watchdog monitor is the most employed mitigation technique to detect and ease SEFI in the processor [26]. In this work, both cores run in the AMP pattern, and they can reset the watchdog timer. The timer duration is about 12.9 s for 667 MHz corresponding to the maximum value 0xFFFFFFFF for the 32-bit counter.

2.3. AMP layer

Usually, for the dual core system, Core0 is the processor that initializes and boots the system configuration, thus, which is the master core in the AMP pattern, and Core1 is the slave one. In the design, Core0 is the master processor in the AMP pattern, and Core1 is the slave that the master awakens at the initialization stage. Then, Core1 starts code execution to detect and mitigate SEU in OCM, cooperating with the redundancy layer when recognizing the effective flag. Fig. 2 displays the workflow, and more detail are described as follows.

In our setup, the OCM is used as data memory, and we test only 32 KB out of the 256 KB OCM on the device. First of all, Core0 writes 0xA5A5A5A5, which can be used to investigate 0-1 and 1–0 upset at the same time, to all the 32 KB memory space. (The check pattern data can also be others, such as 0xFAFAFAFA, 0xFFFFFFFF even random). And a flag variable is stored in another place outside of the 32 KB range. The flag is set by both cores alternately at the end of their examinations. Core0 checks whether the flag is 0xF0 to start its examination. This flag is set by Core1 when it checks the data over. Core1 begins operation when the flag is 0x0F, set by Core0 when it finishes the examination. It can also be viewed in Fig. 2.

Then, when the 32 KB OCM writing is over by Core0, and the flag is set for the first time, Core1 launches its check. It copies OCM data to two DDR spaces and enters the redundancy layer. Core1 reads the OCM data consecutively in three cycles firstly. To guarantee data correctness in OCM, if Core1 detects one datum different from others in temporal redundancy examination, it will correct errors

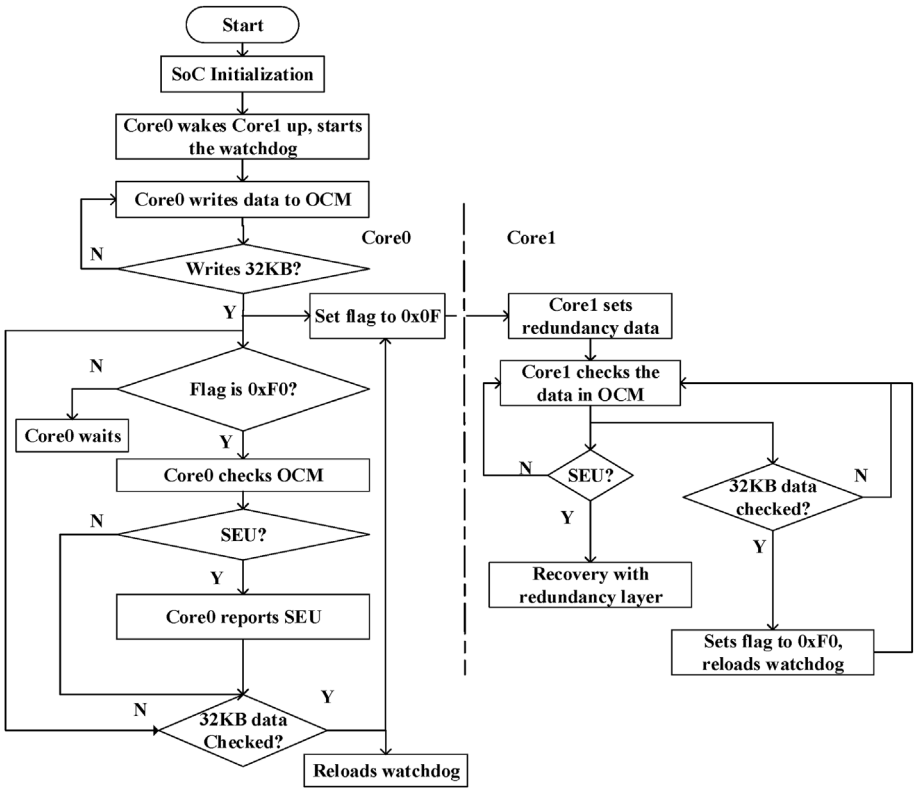

Fig. 2. Workflow of the AMP layer.

directly using redundant data. Otherwise, if the temporal redundancy check did not detect any data corruption, then the spatial redundancy check will be performed. If the OCM datum is different from the two redundant copies in DDR, it is considered a corrupted one. The mechanism will try to correct the corrupted data via copying the redundant ones. If all three copies are different, Core1 will keep the datum in OCM. During Core0 check, it will examine the data again through making XOR operation with the expected 0xA5A5A5A5. If it is indeed corrupted or not corrected by Core1, the upset data and address will be reported by Core0 and stored in the log file.

During Core1 checking, Core0 is available for other workloads, such as logic or algorithm applications. Compared with a single processor system, this improves the efficiency and performance of the entire system. It can be considered as the Core1 is dedicated to detecting SEU and SET in OCM.

Meanwhile, when each Core finishes the examination, they also reload the watchdog besides setting the flag. The watchdog will be activated no matter which Core encounters SEFI leading to operation halt or exceptions, and the system will be re-launched. The cooperation of these layers keeps the correctness of data in OCM. Proton irradiation tests are performed to examine the design performance.

3. Irradiation tests

Two proton irradiation tests were conducted at the National Innovation Center of Radiation Application (NICRA), China Institution Atomic Energy (CIAE). In the first irradiation test, OCM has been tested without any SEE mitigation measures. In the second irradiation test, OCM adopted the abovementioned multi-layer design.

3.1. Device overview

The Xilinx Zynq-7000 SoC is the DUT, fabricated with Taiwan Semiconductor Manufacturing Company (TSMC) 28 nm high-k metal gate technology. Two critical parts are integrated into it. One is the Processing System (PS), and the other is Programmable Logic (PL) [27]. Table 1 lists vital parameters of the SoC [28]. The chip package is a ball grid array (BGA), which was de-capped before the irradiation. Since the medium and high energy protons result in SEE on the DUT relying on the generated secondary energetic particles with silicon, instead of the direct ionization from striking protons. De-capping or not is usually considered to have no influence on the results. For two irradiation tests, SoC components, such as processors, OCM, and other interfaces, run in nominal conditions without any biased operation.

3.2. Test setup

The irradiation test facility locates in a shielding room, which is away from the main hall more than 10 m, where the monitor and power are placed. The host computer and programmable power

Table 1
Key device parameters of 28 nm SoC.

PS.	Dual-core ARM Cortex-A9	667 MHz
	On-chip memory	256 KB
	L1 Instruction/Data Cache	32 KB
	L2 Cache	512 KB
PL.	Programmable logic cell	28 K
	Look-Up Table	17600
	Flip-Flops	35200
	Block RAM	2.1 Mb
	DSP Slice	80

remotely connect the test board that is mounted on the facility holder. The host computer communicates with the device through a fiber USB cable. Once the program exception appears during irradiation, the particle beam is halted immediately. The programmable power supplied the test board through a cable during the irradiations, and it is also used to detect current abnormality. The nominal current of the board is about 0.33 A. The running messages are logged from the UART interface in real-time.

3.3. Proton beam

Ejected from the accelerator, following a series of processing measures, including homogenization, energy adjustment, and collimation, then the proton beam hits the DUT. The beam spot is adjustable and can be adjusted from 1 cm × 1 cm–10 cm × 10 cm, and the proton energy range is 30~100 MeV [29,30]. The minimum spot can cover the entire de-capped chip, about 1 cm × 1 cm in size. The adopted beam spot covered the whole SoC chip and the DDR memory regions during the irradiation. Fig. 3 shows the photo of the irradiation worksite. It can be viewed, only the SoC chip is de-capped, other components are in normal conditions.

Two irradiation tests were performed using the same facility at different times. 90 and 70 MeV proton beams are both used in two irradiation tests. Beam fluxes and fluences of two tests are listed in Table 2. Referring the fluence and linear energy transfers, the accumulative doses in the current irradiation are about 5.06 and 6.08 krad for the 90 and 70 MeV irradiaitons, respectively.

The irradiation begins when the beam switches on, the host computer displays the real-time information. During the irradiation, the AMP dual-core, the temporal redundancy, spatial redundancy and watchdog cooperate to process the detected SEE as introduced.

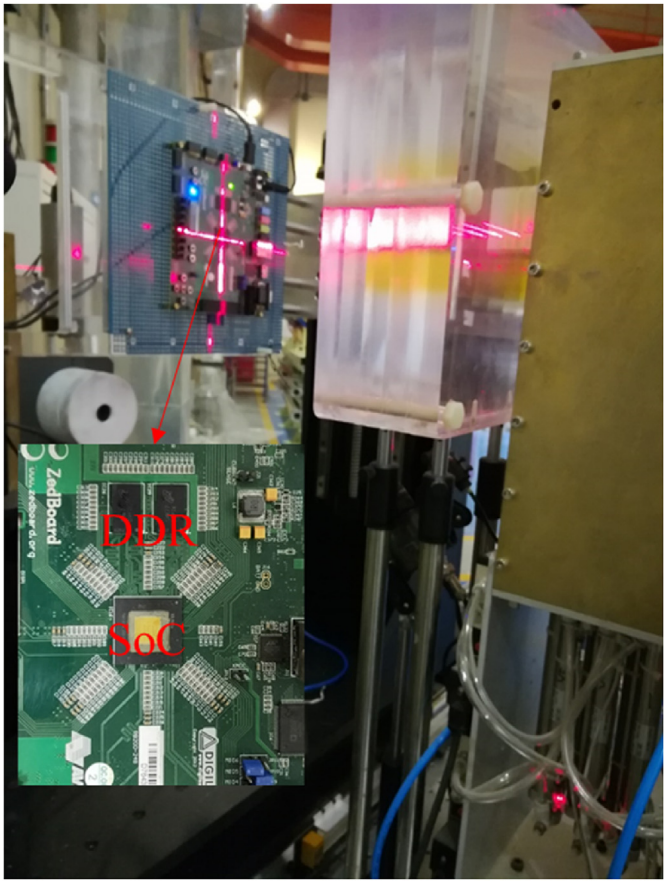

Fig. 3. Photo of the irradiation worksite.

4. Results and discussions

In the first irradiation tests, both SEU and SEFI were detected in 90 and 70 MeV irradiations without utilizing any mitigation. However, no SEU was observed in the second irradiation tests when OCM adopted the multi-layer design. SEFI events just emerged in 90 and 70 MeV proton irradiations. No abnormal currents were detected in two irradiation tests.

4.1. Test results

The detail of SEU and SEFI events of first irradiation tests is presented in Table 3. For SEU, it contains single bit upset (SBU) and multi-cell upset. For SEFI events, the test system is recovered by the power cycle.

For the second irradiation test, the number of SEFI events in 90 and 70 MeV irradiations are listed in Table 4. It is different from the SEFI events processing in the first irradiation test. Watchdog recovered them in this irradiation test.

4.2. Results analysis

During both tests, phenomena, such as halt in the output terminal, were regarded as SEFI. The discrepancy was that the SEFI events are monitored by the watchdog, and handled via soft-reset, during the second irradiation test. In contrast, they were solved by manual power-cycle of the system in the first irradiation test.

For the observed SEFI events in the second irradiation test, as outlined in Table 5, the majority appeared as the hang, characterized by messages stopping output. The one Output garbled manifests continuously unknown messages output. The SEFI cross sections of the two irradiation tests are displayed in Fig. 4. In the first irradiation test, the SEFI cross sections are $(6 \pm 2.45) \times 10^{-11}$ cm^2 and $(7 \pm 2.65) \times 10^{-11}$ cm^2 for 70 and 90 MeV irradiations, respectively. For the second irradiation test, the SEFI cross sections are $(8 \pm 4) \times 10^{-11}$ cm^2 and $(12 \pm 5) \times 10^{-11}$ cm^2 for 70 and 90 MeV irradiations, respectively. Compared with the first irradiation test, the ratios are 1.3 and 1.7, respectively.

Because the proton fluxes for two irradiation tests and the fluxes for 90 and 70 MeV proton irradiations were different, the flux influence was checked. As Table 6 presents, two fluxes irradiation tests were performed for 70 MeV proton, the results show there is no difference in SEE cross section for the same fluence, verifying that the proton flux does not influence the SEE cross section. Because two processors are utilized in this design, expanding the number of utilized registers, the SEFI probability is increased, however, the system can be recovered from SEFI by soft-reset automatically, different from manual power-cycle in the first irradiation test without hardening. Register refreshing, can be adopted in this multi-layer design to improve system resilience against the SEFI events, too.

Multi factors can cause SEFI, although it appears as hang or output garbled. For example, it may be caused by data corruption in processor registers or interface registers. It is difficult to predict them immediately during irradiation, and watchdog is a solution to solve. In this design, as mentioned above, the watchdog is reloaded by both ARM cores interactively. It processes the SEFI events in time without repowering the test board.

The irradiation tests illustrate the adopted multi-layer design mitigates SEU in 28 nm SoC effectively. For the redundancy layer,

Table 2
Beam fluxes and fluences in two irradiation tests.

Test	Energy /MeV	Flux /10^{8}p·cm^{-2}·s^{-1}	Fluence /10^{11} p·cm^{-2}
First test [18] (Without mitigation)	90	1.30	1.00
	70	2.30	1.00
Second test (With multi-layer design)	90	0.28	0.50
	70	0.20	0.50

Table 3
Observed events in the first irradiation test [18].

Effect		SEU					SEFI
Type		SBU	2-Cell upset	3-Cell upset	4-Cell upset	>4-cell upset	/
#Number	90 MeV	102	27	11	1	2	7
	70 MeV	88	18	8	3	0	6

Table 4
Observed events in the second irradiation test.

Energy/MeV	SEFI
90	6
70	4

Table 5
The SEFI details the second irradiation test.

Energy (MeV)	SEFI	Number	Recovered
90	Hang	5	Y
	Output garbled	1	Y
70	Hang	4	Y

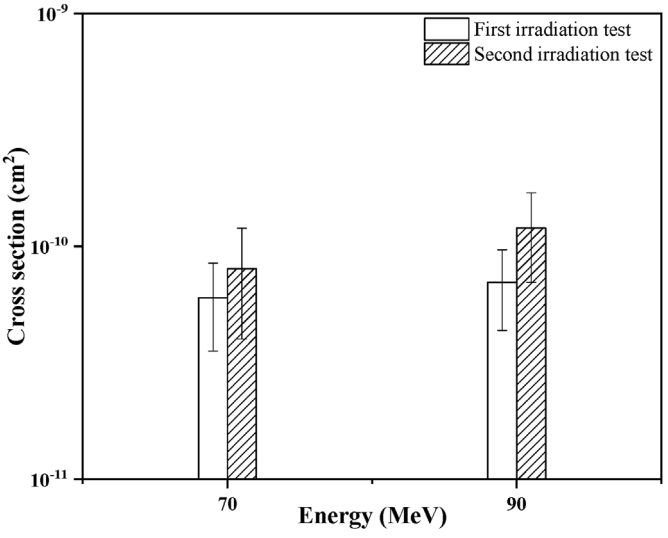

Fig. 4. The SEFI cross section in proton irradiation.

Table 6
Different flux irradiation results at 70 MeV proton.

Flux/10^{8}p·cm^{-2}·s^{-1}	Fluence/10^{11}p·cm^{-2}	SEFI	Cross section/10^{-11}cm^2
0.2	0.5	4	(8 ± 4)
0.1	0.5	4	(8 ± 4)

the temporal redundancy was used firstly to report SEU rather than using the spatial redundancy directly. This operation improves efficiency in upset detection. Since the DDR is outside of the chip with a longer read routine. In order to examine the improvement as a whole, we compared two cases' cycles. In the first case, 32 KB OCM was read three times in three cycles to determine whether a SEU occurs, and the time cycle is 23.88 ms. While it is 33.30 ms using the spatial TMR directly in the second case. It indicates the time cycle can be shortened by 28.3%. As the memory capacity increases, it can be speculated that this difference is more prominent. Another consideration of introducing temporal redundancy is to detect and process SET in OCM effectively, avoiding SET possible propagation from OCM to other blocks in a certain.

For a sole processor system, if the processor needs to perform the error detection and recovery operations, the ongoing applications will be affected or halted. And for the symmetric lockstep way, requires matching dual-core states. For instance, in [31], the dual-core processor in Xilinx Zynq-7000 SoC is executed as the symmetric lockstep way to immune SEE, but it requires to waits for 100 ms until dual-cores match their states, if they are not in the equal states. However, they can be avoided in the AMP pattern. For the AMP layer, the dedicated slave ARM core makes the master processor run the ongoing applications without being disturbed and don't need to match them. Moreover, for the 32 KB OCM, if a single processor examines an SEU, the cycle is about 15.6 ms, while for the AMP pattern, the period is about 8.3 ms. The time is shortened by 46.7%. Although we just examined the OCM block, this multi-layer design is also applicable to other shared resources. Even though the current design examined the 32 KB OCM, after verification in the manuscript, it can be applied in any capacity memory SEE hardening.

In this work, the SEE hardening performance is examined for the AMP cooperating with TMR and watchdog compared with the unhardened one using proton irradiation. In the future, more SEE hardening measures relying on the dual-core can be designed and more radiation tests will be performed to compare with this design.

5. Conclusion

A dual-core system-on-chip can run in an AMP pattern. A multi-layer design based on the AMP pattern cooperating with redundancy and watchdog monitor was applied to mitigate SEE in the 28 nm SoC. Two proton irradiation tests were performed to examine the performance of the mitigation design. The test results demonstrate that the multi-layer design can mitigate SEU in the 28 nm SoC effectively. In the first irradiation test without

employing mitigation, both SEU and SEFI events were observed. While during the second irradiation test, only SEFI events were detected due to adopting the multi-layer design. The multi-layer design can significantly shorten the cycle 46.7%, and can also be used to mitigate SEE on other components in 28 nm SoC.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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