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Implementation of a High Performance XOR-XNOR Circuit

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ABSTRACT

The parity function can be implemented with XOR (exclusive-OR) and XNOR (exclusive NOR) circuit. In this paper we propose a high performance XOR-XNOR circuit. The proposed circuitreduced the internal load capacitance on critical path and implemented with 8 transistors. The circuit produces a perfect output signals for all input combinations. Compared with the previous circuits, the proposed circuit presents the improved characteristics in average propagation delay time, power dissipation, power-delay product (PDP), and energy-delay-product (EDP). The proposed circuits are implemented with standard CMOS 0.18um technology. Computer simulations using SPICE show that the proposed circuit realizes the expected logic functions and achieves a reasonable performance.

Keywords

Parity Function, XOR-XNOR, High-Performance Circuit, Low-Power Circuit, Energy-Efficient Circuit, PDP, EDP

Ⅰ. Introduction

In Boolean algebra, the parity is a function in which the output depends on the number of 1s in the input. Parity function circuits have applications in many areas such as arithmetic, error detection and correction, communications and linear systems. Among these are adders, parity generators and checkers, encrypting and coding schemes for error control and synchronization circuits, sequence generators for process identification, system testing, signal acquisition, signal ranging and synchronization, and fault - tolerant circuit designs [1-4]. The circuits that use XOR and XNOR gates have several advantages over circuits which use other kind of gates such as NAND or NOR gates. Some advantages are their improved testability and reduced number of transistors. However, XOR and XNOR circuits require a large layout area for their realization on system-on-chip (SOC). Especially, XOR-XNOR circuit which generates the dual rail signals XOR and XNOR is the essential circuit for high performance arithmetic circuits [5-8]. The average propagation delay time, power dissipation, and power-delay-product (PDP), and energy-delay-product (EDP) are the essential metrics for the high performance parity function circuit. Many researches for parity function circuit have been performed. The various improved implementations of the parity function circuit have been presented in recent years [9-11]. This paper proposes a novel high performance parity function circuit reducing the internal load capacitance on the critical path.

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II. Previous works

2.1 Previous work 1

The XOR-XNOR circuit proposed by S. Kumar and M. Kumar is shown in Fig. 1 [9]. This circuit provides good driving capability as it uses static CMOS inverter and can operate at low supply voltages. In this circuit when inputs AB=00, the output (XOR) is a low logic signal (logic 0) because transistors P1, P2, and N3 are turned on and a low logic signal is passed to the output (XOR). When inputs AB=01, the output (XOR) is a high logic signal (logic 1) because transistor P1, N2, and N3 transistors are turned on while transistors P2, P3 and N1 are turned off and a high logic signal is passed to the output (XOR). In another case when inputs AB=10, the output (XOR) is a high logic signal because transistor P2, P3 and N1 are turned on and a high logic signal is passed to the output (XOR). In last case when inputs AB=11, the output (XOR) is a low logic signal because transistor P3, N1, and N2 are turned on and a low logic signal is passed to the output (XOR). Another output (XNOR) is obtained from the inverter consisting of transistors P4 and N4.

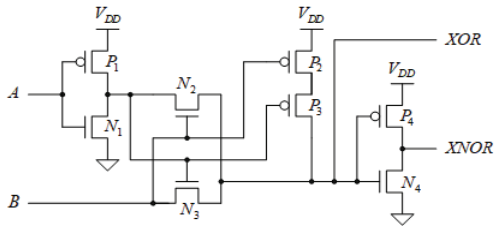

Fig. 1 Circuit diagram of previous work 1

2.2 Previous work 2

The XOR-XNOR circuit proposed by M. Kumar and J. Nath is shown in Fig. 2 [10]. In this XOR-XNOR circuit, the inverter consisting of transistors P1 and N1 generates the complement of input A. The output of this inverter controls the second inverter consisting of transistors P2 and N2. This second inverter nearly generates the XNOR function of A and B with a problem of voltage degradation for the input combinations AB=10 and 11. To avoid the problem two level restoring pass transistors P3 and N3 are used.

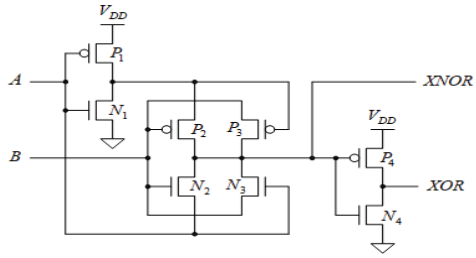

Fig. 2 Circuit diagram of previous work 2

In Fig. 2 when inputs AB=00, the transistors P1 and P2 are turned on and output (XNOR) is a high logic signal. When inputs AB=10, transistors P2, P3, N1, and N3 are turned on and a low logic signal is passed to the output (XNOR). Again for inputs AB=01, transistors P1 and N2 are turned on and the output (XNOR) shows a low logic signal. Finally, when inputs AB=11, transistors P3, N1, N2, and N3 are turned on and the output (XNOR) is a high logic signal.

2.3 Previous work 3

The XOR-XNOR circuit proposed by J. Kim is shown in Fig. 3 [11]. In this XOR-XNOR circuit, the first stage output signal in the case of inputs AB=00, 01, and 10 will be complete while inputs AB=11, transistors N1 and N2 are turned on and pass the “poor high” logic signal to the first stage output end. That is, if inputs AB=11, the first stage output end will display a voltage, VDD-V_T, a little lower than “high” but double path driving capability exists, due to both transistors N1 and N2’s being on. Hence, though the output is not complete, the driving current will increase. The inverter consisting of transistors P3 and N3 generates the complement of the first stage output, XOR.

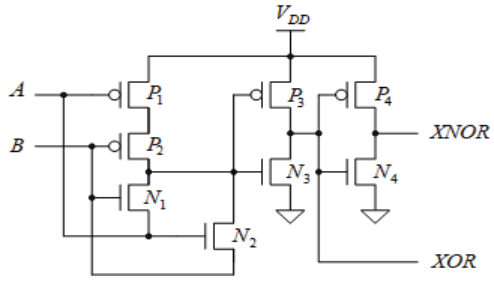

Fig. 3 Circuit diagram of previous work 3

The output of this inverter drives the second inverter consisting of transistors P4 and N4. This second inverter generates XNOR. This circuit has a driving output, and the signal level at both XOR and XNOR output end is perfect in all input combinations.

III. Proposed circuits

To achieve a high performance XOR-XNOR circuit, the proposed circuit has reduced the propagation delay time and the power disssipation by minimizing the internal load capacitance on the critical path. The proposed XOR-XNOR circuit is shown in Fig. 4. In the proposed circuit, the inverter consisting of transistors P1 and N1 generates the complement of input A. The output of this inverter controls the second inverter consisting of transistors P2 and N2. This second inverter nearly generates the XOR function of A and B with a problem of voltage degradation for the input combinations AB=00 and 01. To avoid the problem two level restoring pass transistors P3 and N3 are used. In this circuit when inputs AB=00, the inverter of input stage produces high logic signal. Transistors P2, P3, and N3 are turned on and transistor N2 is turned off. Therefore, the output (XOR) shows perfect low logic signal by transistor N3 and the output (XNOR) shows perfect high signal by the inverter of output stage. When inputs AB=01, the inverter of input stage produces high logic signal. Transistors P3, N2, and N3 are turned on and transistor P2 is turned off. Therefore, the output (XOR) shows perfect a high logic signal by transistor P3. and the output (XNOR) shows perfect low signal by the inverter of output stage. Again for inputs AB=10, the inverter of input stage produces a low logic signal. Transistor P2 is turned on and transistors P3, N2, and N3 are turned off. Therefore, the output (XOR) shows perfect high logic signal by transistor P2 and the output (XNOR) shows perfect low signal by the inverter of output stage. Finally, inputs AB=11, the inverter of input stage produces a low logic signal. Transistor N2 is turned on and transistors P2, P3, and N3 are turned off. Therefore, the output (XOR) shows perfect low logic signal by transistor N2 and the output (XNOR) shows perfect high signal by the inverter of output stage.

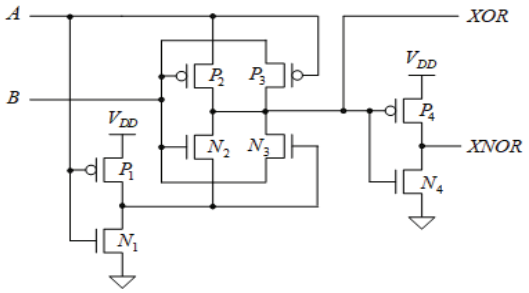

Fig. 4 Circuit diagram of proposed work

In the proposed circuit, total internal load capacitance on the critical path is equal to $2C_{gp}+3C_{gn}$. For example, with $C_{gp} \simeq 2C_{gn}$, in the proposed circuit, the overall internal load capacitance is approximately $7C_{gn}$.

To achieve a high performance XOR-XNOR circuit, the load capacitance of the input nodes, the internal nodes, and the output nodes are all related to the average propagation delay time and the power dissipation. Table 2 shows the comparison of

the internal load capacitance on the critical path for the various XOR-XNOR circuits.

From Table 1 we can confirm that the proposed XOR-XNOR circuit has the smallest internal load capacitance on the critical path. Therefore, the proposed XOR-XNOR circuit has a high performance characteristics because the proposed circuit has fast average propagation delay time, low power dissipation, and low PDP.

Table 1. Comparison table for the internal load capacitance on the critical path

	The internal load capacitance
Previous work 1 [9]	$3C_{gp}+2C_{gn} \simeq 8C_{gn}$
Previous work 2 [10]	$3C_{gp}+2C_{gn} \simeq 8C_{gn}$
Previous work 3 [11]	$3C_{gp}+3C_{gn} \simeq 9C_{gn}$
Proposed circuit	$2C_{gp}+3C_{gn} \simeq 7C_{gn}$

Ⅳ. Simulation results

The validity and effectiveness of the proposed circuit is verified through the SPICE under 0.18 um standard CMOS technology with the supply voltage 1.8V. For the simulation, 0.5pF capacitance is connected at the outputs respectively.

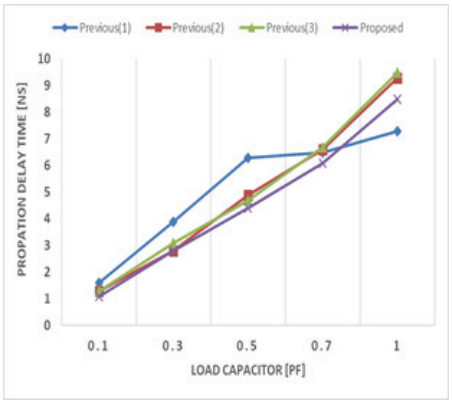

Fig. 5 Comparison of the average propagation delay time with load capacitance variation

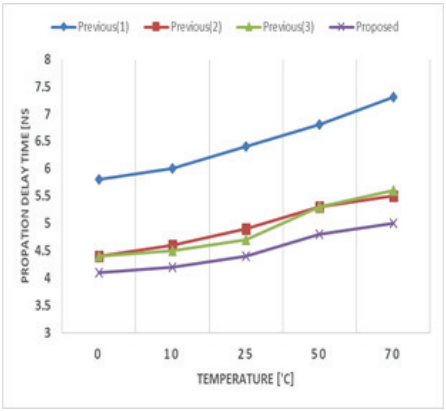

Fig. 6 Comparison of the average propagation delay time with temperature variation

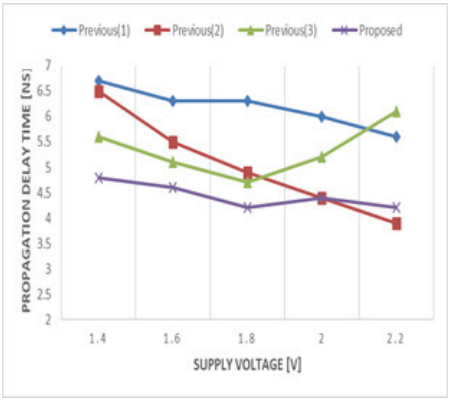

Fig. 7 Comparison of the average propagation delay time with supply voltage variation

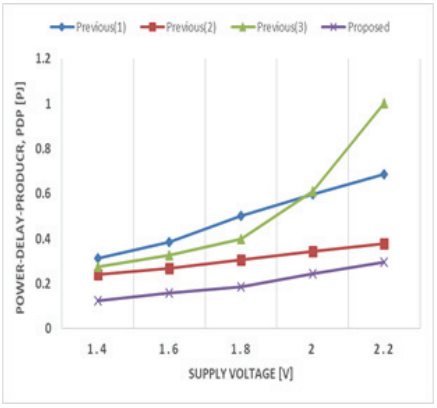

Fig. 8 Comparison of PDP with supply voltage variation

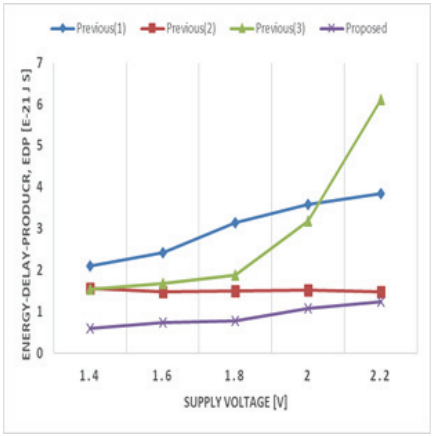

Fig. 9 Comparison of EDP of with supply voltage variation

Table 2. Simulation results

	t_P [ns]	p_D [uW]	PDP [pJ]	EDP [E-21Js]
Previous work 1 [7]	6.3	79.4	0.500	3.150
Previous work 2 [8]	4.9	62.8	0.306	1.499
Previous work 3 [9]	4.7	84.7	0.398	1.971
Proposed circuit	4.4	44.0	0.194	0.954

The simulation results show that the proposed circuit is functioning correctly for all input combinations. Table 2 shows the simulation results of electrical characteristics for the parity function circuits. The average propagation delay time t_P is an average value of t_{PLH} and t_{PHL}. Power dissipation p_D is an average power consumption through 500ns. PDP is the product of p_D and t_P. EDP is the product of PDP and t_P. Among the previous circuits, the previous work 3 has the lowest average propagation delay time. Also, the previous work 2 has the lowest power dissipation, PDP, and EDP. Compared with the superior circuit among the previous circuits, the proposed circuit reduced the average propagation delay time by 6.4%, the power dissipation by 29.7%, PDP by 36.6%, and EDP by 43.0%, respectively. From Table 2, it is obvious that the proposed circuit is the most competitive circuit among the previous circuits.

The comparisons of the average propagation delay time of the XOR-XNOR circuits with load capacitance variation (0.1pF to 1pF) and commercial operating temperature variation (0°C to 75°C) are shown in Fig. 5 and 6, respectively. From Fig. 5, we know that the proposed circuit has the lowest average propagation delay time. below 0.75pF load, whereas the previous work 1 has the lowest average propagation delay time above 0.75pF. Also, from Fig. 6, we know that the proposed circuit has the lowest average propagation delay time in the temperature variation. When the supply voltage changes from 1.4V to 2.2V (assume 0.5pF load capacitance and to 25°C temperature), the comparisons of the average propagation delay time, PDP, and EDP are shown in Fig. 7, 8 and 9, respectively. From Fig. 7, we know that the proposed circuit has the lowest average propagation delay time below 2V supply voltage, whereas the previous work 2 has the lowest average propagation delay time above 2V supply voltage. From Fig. 7, 8 and 9, we know that the proposed circuit has the lowest PDP and EDP in the supply voltage varying from 1.4V to 2.2V. However, above 2.4V supply voltage, the previous work 2 has the lowest average propagation delay time.

Ⅴ. Conclusion

This paper proposes a high performance XOR-XNOR circuit. To achieve the high performance circuit, we reduced the internal load capacitance on the critical path. According to the simulation results, the proposed parity function

circuit realize the perfect logic functions and achieve a high performance characteristics. Future work will include the improvement of the driving capability in a large load and the stability in high supply voltage

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