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A Wideband Inductorless LNA for Inter-band and Intra-band Carrier Aggregation in LTE-Advanced and 5G

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Abstract

This paper presents a wideband low noise amplifier (LNA) that is suitable for LTE-Advanced and 5G communication standards employing carrier aggregation (CA). The proposed LNA encompasses a common input stage and a dual output second stage with a buffer at each distinct output. This architecture is targeted to operate in both intra-band (contiguous and non-contiguous) and inter-band CA. In the proposed design, the input and second stages employ a g_m enhancement with resistive feedback technique to achieve self-biasing, enhanced gain, wide bandwidth as well as reduced noise figure of the proposed LNA. An up/down power controller controls the single input single out (SISO) and single input multiple outputs (SIMO) modes of operation for inter-band and intra-band operations. The proposed LNA is designed with a 45nm CMOS technology. For SISO mode of operation, the LNA operates from 0.52GHz to 4.29GHz with a maximum power gain of 17.77dB, 2.88dB minimum noise figure and input (output) matching performance better than -10dB. For SIMO mode of operation, the proposed LNA operates from 0.52GHz to 4.44GHz with a maximum voltage gain of 18.30dB, a minimum noise figure of 2.82dB with equally good matching performance. An IIP_3 value of -6.7dBm is achieved in both SISO and SIMO operations. with a maximum current of 42mA consumed (LNA+ buffer in SIMO operation) from a 1.2V supply.

Key words : carrier aggregation, single input single out (SISO), single input multiple outputs (SIMO), LTE-Advanced, inter-band, intra-band, contiguous, non-contiguous

Ⅰ. Introduction

Mobile network operators need more capacity and faster speed to meet the insatiable demand for mobile data while ensuring a good user experience, especially for streaming video and other data-intensive applications. Achieving these goals with the limited and fragmented spectrum across multiple bands becomes a huge task to mobile-network operators. CA is the solution that is widely investigated in addressing these challenges. CA raises the bandwidth and capacity of communication systems by combining two or more bands (inter-band CA) or several channels within a single band (intra-band CA, contiguous and non-contiguous) [1]. Intra-band CA is largely used to increase capacity rather than a wider band due to the sharing of propagation characteristics and commonality of frequencies, while inter-band CA is employed for wide bandwidth [2]. An inter-band CA will have the same bandwidth as a conventional wideband LNA.

In this paper, the design of a SISO and a SIMO low noise amplifier is presented for 8

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component carrier CA scenarios when the proposed LNA is embedded within the harmonic reconfigurable receiver [3] as shown in Fig. 1. In Section II, the CA receiver architecture is presented, focusing on the LNA requirements. Section III discusses the design of the proposed LNA with respect to its input matching, gain, bandwidth and noise analysis, and output reflection. The implementation and layout related issues are outlined in Section IV. Section V presents the simulation results in its gain, noise figure, S_{11}, and S_{22} followed by the conclusion in Section VI.

II. RF Front-End Architecture for CA Operation

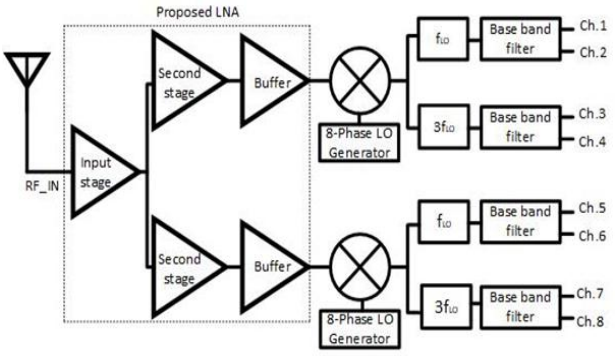

Fig. 1. Block diagram of the proposed RF front-end supporting 8-carrier aggregation.

A number of receiver architectures were reported to support carrier aggregation at the architectural level and the circuit level. In [1], several LNA topologies were investigated with trade-offs in their performances in terms of the impedance matching, low noise, and high linearity. The results presented are promising but it operates with a narrow bandwidth. Intra-band CA architecture [4] provides contiguous and non-contiguous operation with limited bandwidth and does not support inter-band operations. Harmonic reconfiguration [3] technique using a single LNA output with an 8-phase mixer for CA is proposed for inter-band and intra-band operations. 16 LNAs were also used in [5] to achieve the targeted design objectives but to the detriment of chip size and cost of design. Fig. 1 shows the architecture of the proposed front-end receiver. The LNA as the core part of the RF receiver front-end consists of a common input common-source inverter-based resistive feedback amplifier, two identical common-source inverter-based resistive feedback amplifiers as the second stage, and a source-follower as a buffer at each distinct output.

III. Design of the Proposed LNA

The shunt feedback topology is preferable for wide bandwidth and good linearity due to the feedback property [6, 7]. This section provides an in-depth analysis of the shunt feedback topology that is used for the proposed LNA architecture from the perspectives of input matching, gain, and noise.

Common gate and common source with resistive shunt-feedback amplifiers provide wideband input matching and flat gain [8]. The resistive input impedance is obtained from the ratio of the feedback resistance and the voltage gain of the common source amplifier [7, 8]. Therefore, to obtain 50 ohms input matching, feedback resistor needs to be only a few hundred ohms and this worsens the noise performance of the amplifier. Additionally, there is a strong dependence of gain on the amplifying devices (transistors); the amplifier with resistive feedback requires a substantial amount of current to generate a large transconductance (gm). This undoubtedly results in higher overall power consumption, providing a tradeoff between higher as well as low noise figure performances.

The input impedance is calculated from the small-signal model [9] shown in Fig. 3 as obtained from the simplified schematic diagram of the proposed LNA in Fig. 2 above. The small-signal model excludes the second and buffer stages as it has been proven below to have a negligible influence on the LNA input impedance performance.

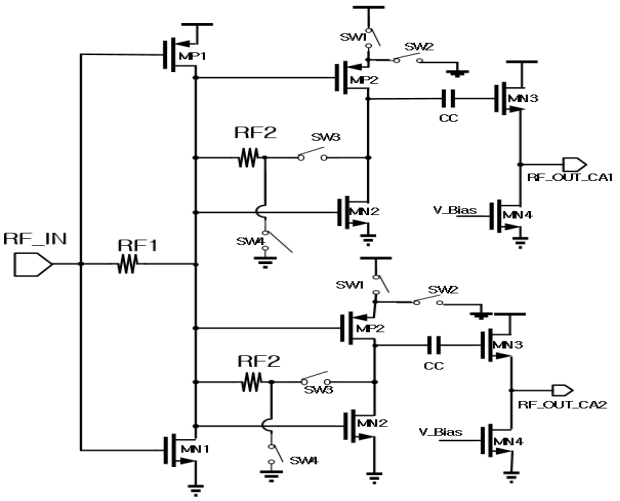

Fig. 2. Simplified schematic diagram of the proposed LNA, biasing not shown.

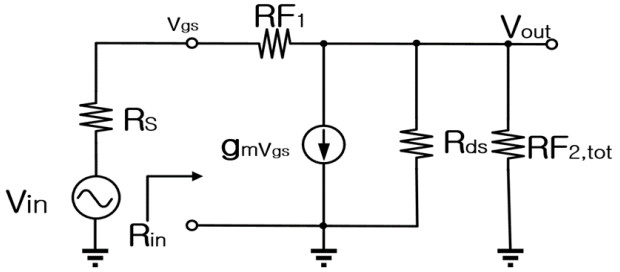

Fig. 3. Small signal model for input impedance analysis.

$$R_{in} = \frac{RF_1}{1-(\frac{gF_1 - g_m}{gF_1 + g_{ds} + gF_{2,tot}})} \quad (1)$$

Where g_m = g_mMN_1 + $gmMP_1$ is the small-signal transconductance, R_{ds} =$1/g_{ds}$ =($r_{on1}//r_{op1}$,) MN_1//($r_{on1}//r_{op1}$), MP_1 is the output resistance of MN_1 and MP_1, and $R_{F2,\ tot}$ = $R_{F2}/2$. With the following assumptions : R_{ds} >> R_{F2} and R_{F1} >> $1/g_m$, equation (1) can be simplified as follows:

$$R_{in} = \frac{RF_1}{1+g_m RF_2(\frac{RF_1}{2RF_1 + RF_2})} \quad (2)$$

The coefficient (two) of R_{F1} in the denominator of the terms within the brackets of equation (2) further decouples R_{F1} and g_m from the input impedance matching, bandwidth, and gain performances. The output resistance of the first stage was selected as low as possible by increasing the g_m of the first stage, resulting in a much undesired higher power consumption but necessary to achieving S_{11} better than -10dB with both SISO and SIMO operations. The proposed design is targeted to operate with a relatively wide bandwidth. In resistive feedback LNA topology, the feedback resistor limits the bandwidth performance. Feedback resistor RF_1 must therefore be chosen low enough in order not to degrade the bandwidth whiles maintaining S_{11} below -10dB. Optimum value of RF_1 in this design Table1.

The low-frequency gains for the first and second stages are derived from the small signal model in Fig. 4 [9] as:

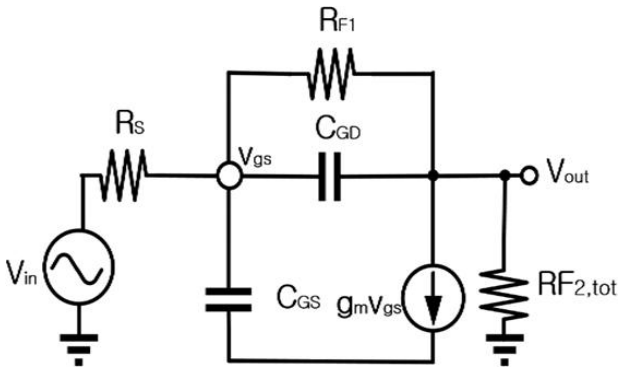

Fig. 4. Small signal model for gain analysis.

$$A_{v1} = \frac{v_{out1}}{v_{\in}} \frac{g_S(g_{F-}g_{m1})}{gF_1(g_{S+}gF_{2,tot} + g_{m1}) + g_S gF_{2,tot}}, \quad (3)$$
$$= \frac{RF_{2,tot}(1-g_{m1}RF_1)}{RF_1 + R_S + RF_{2,tot} + g_{m1}R_S RF_{2,tot}}.$$

Equation (3) can be simplified as:

$$A_{v1} \cong -(\frac{RF_1}{R_S})(\frac{1}{1+\frac{1}{1+g_{m1}RF_1}}) \quad (4)$$

The second stage gain is also given in equation (5) below.

$$A_{v2} \cong -(\frac{RF_2}{RF_1})(\frac{1}{1+\frac{1}{1+g_{m2}RF_1}}) \quad (5)$$

The source follower buffer gain was also derived in equation (6) below as:

$$A_{v3} \cong \frac{\frac{1}{g_{m4}} // r_{04} // r_{o3}}{\frac{1}{g_{m4}} // r_{04} // r_{o3} + \frac{1}{g_{m3}}} \quad (6)$$

Then, the overall gain of the open loop amplifier becomes:

$$A_v = \frac{v_{out}}{v_{in}} = A_{v1} A_{v2} A_{v3} \quad (7)$$

The major noise sources in this circuit are the feedback resistors, MOSFET transistors, and the bias resistors. The output referred noise of transistors MN_1 and MP_1 are given as:

$$\overline{v^2}_{n_{MN1}} = 4KT\gamma g_{m,MN1}\left(\frac{RF_1 + R_S}{g_{mMN1,MP1} R_S RF_2}\right)^2,$$
$$\overline{v^2}_{n_{MP1}} = 4KT\gamma g_{m,MP1}\left(\frac{RF_1 + R_S}{g_{mMN1,MP1} R_S RF_2}\right)^2 \quad (8)$$

The feedback resistors output noises are also given below:

$$\overline{v^2}_{n,RF1} = 4KTRF_1.$$
$$\overline{v^2}_{n,RF2} = 4KTRF_2\left(\frac{RF_1 + R_S}{g_{mMN1,MP1} R_S RF_2}\right)^2 \quad (9)$$

The noise factor of the input stage is approximated as:

$$F_1 \cong 1 + \frac{R_S}{RF_1} + \gamma\frac{1}{g_m R_S}\left(1 + \frac{R_S}{RF_1}\right)^2 + \frac{1}{{g_m}^2 RF_{2,tot} R_S}\left(1 + \frac{R_S}{RF_1}\right)^2 \cong 1 + \frac{R_S}{RF_1} + \gamma\frac{1}{g_m R_S} \quad (10)$$

Similarly, F_2 (noise factor of the second stage) can also be simplified as:

$$F_2 \cong 1 + \frac{R_S}{RF_2} + \gamma\frac{1}{g_m R_{out1}} \quad (11)$$

Where R_{out1} is the output impedance of the first stage with the assumption that $R_{out1}=R_S$.

From the Friis equation [10], the total noise factor of the input and second stages is given by equation (12). The noise of the buffer stage is ignored with the assumption that A_{v1} and A_{v2} are significantly high.

$$F = F_1 + \frac{F_2 - 1}{A_{v1}} \cong 1 + \frac{R_S}{RF_1} + \gamma\frac{1}{g_m R_s} \quad (12)$$

Thus, the noise of the first stage controls the system's total noise figure. From equation (12), R_S, RF_1 and γ are fixed parameters and cannot be manipulated for noise figure improvement. To improve on the noise performance, the transconductance (g_m) of the first stage must be increased but at the cost of increase in power consumption.

IV. Implementation and Layout Issues

The proposed wideband g_m enhanced resistive feedback LNA was designed in TSMC 45nm CMOS technology. Fig. 5 shows the final design with two inverters and two source follower buffers. Switches S_{W1} and S_{W3} are implemented with PMOS transistors, hence we needed an inverter circuit to invert the up/down power control from the convention ON/OFF (one/zero) input to turn ON/OFF S_{W1}. Switches S_{W2} and S_{W4} were also implemented with NMOS. Switch S_{W1} is used to control the supply voltage, which turns off the second stage transistor (MP_2). For CA1/CA2 SISO operation, CA2/CA1 input is low, turning off S_{W1} at CA2/CA1 path, resulting in RF_out_CA2 zero. S_{W2} channels any undesired signals the source of MP_2 to ground when S_{W1} is off in SISO operation. In addition, S_{W3} is used to control the feedback signal to the output of the first stage during SISO operation with S_{W4} acting as a signal path to ground when S_{W3} is off. The widths of the switching devices S_{W2}, S_{W3} and S_{W4} were sized to the minimum to reduce the source and drain capacitances (C_{GS} and C_{GD}) at the output nodes as well as their coverage area in the layout. However, S_{W1} has a large width to supply a high source voltage to MP_2 for a higher gain.

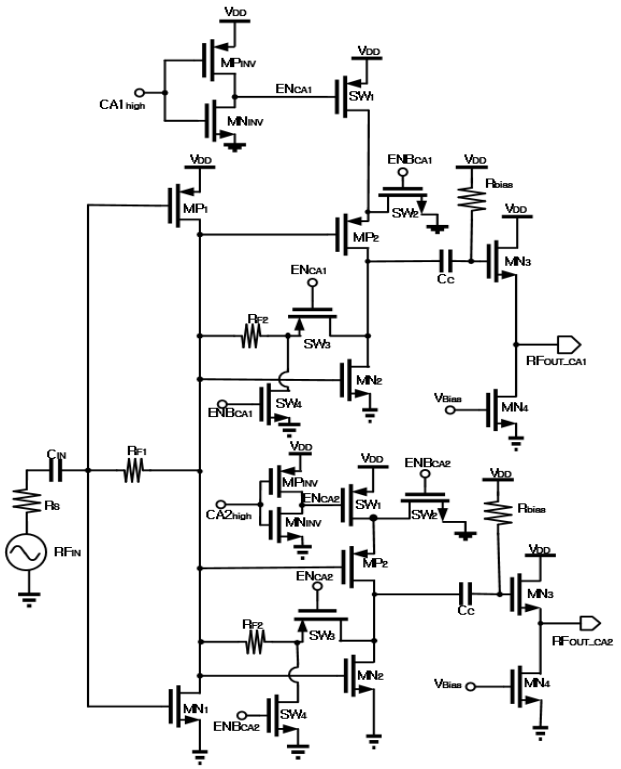

Fig. 5. Schematic diagram of the proposed LNA.

The feedback resistor at the input stage (R_{F1}) is critical for the amplifier's input impedance matching as shown in equation (2). To obtain S_{11} below -10 dB across the desired bandwidth, the value of (R_{F1}) must be a few hundred ohms. On the other hand, a high (R_{F1}) value is required to achieve a high gain and low noise figure as in equations (4) and (12). Due to the constant (two) in equation (2), R_{F1} can be further increased to twice its value but is equally limited by the bandwidth requirement. The gain can also be improved by increasing the transconductance (g_{m1}) but at a cost of higher current consumption. In this design, high gain, as well as wide bandwidth operations, are required. Thus, g_{m1} is increased to achieve a high gain and wide bandwidth at the cost of higher current consumption. Similarly, the second stage transistors are also sized to further increase the overall gain of the amplifier. The input matching is less dependent on the feedback resistor (R_{F2}) and can be increased to enhance the overall gain. Additionally, the second stage can output up to 4 distinct output paths without compromising the input matching but with only a 1dB reduction in gain for each additional output path. That is a 14dB gain for a 4 output signal paths. To reduce bandwidth degradation, we chose a minimum possible AC coupling capacitance (Cc) as shown in Table 1.

Table 1. Device dimension.

Component	Parameter
MN_1, MP_1	(1.5um/40nm)x64, (1.5um/40nm)x120
MN_2, MP_2	(1.5um/40nm)x40, (1.5um/40nm)x80
MN_3, MN_4	(1.5um/40nm)x11, (1um/40nm)x3
MP_{SW1}, MN_{SW2}	(1.5um/40nm)x70, (1.2um/40nm)x1
MP_{SW3}, MN_{SW4}	(1um/40nm)x3, (1.2um/40nm)x1
MP_{INV}, MN_{INV}	(600nm/40nm)x1, (600nm/40nm)x1
R_{F1}, R_{F2} r_{on1}, r_{op1},	214 ohms, 30 ohms 30 ohms, 69 ohms
R_{bias}, Cc	1k ohms, 155 fF

We minimized the parasitic resistance and capacitance by employing multi-metal [11] technique while laying out our design. The metal interconnections at the inputs and outputs of the first and second stages introduced a substantial amount of parasitic resistance and capacitance, which degrade the LNA performance. Thanks to the absence of an inductor, the final measured layout size was 0.047 mm^2 (LNA only) and is shown in Fig. 6. Although the chip occupies a relatively small area, the presence of the two inverter blocks also increased the total area. If S_{W1} were implemented with an NMOS device, the area would have reduced further. We also minimized the parasitic resistance of the drain and source of S_{W1}, by using a higher metal layer in order to supply sufficient voltage to the amplifying devices.

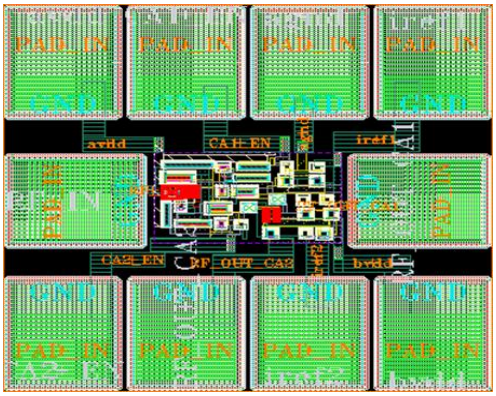

Fig. 6. The layout of the proposed LNA.

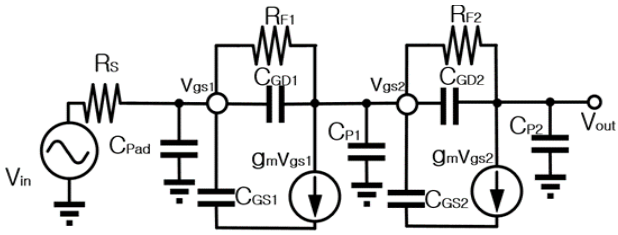

Fig. 7. Parasitic effects due to the layout.

V. Simulation Results

Figs. 8-12 show the S_{21}, S_{11}, NF, S_{22}, and IIP_3 parameter performance of the proposed LNA comparing the schematic and the layout designs. The schematic simulation results shown are the worst-case scenario analysis. The parasitic effects from the layout (shown in Fig. 7) are included in the schematic analysis to align the center frequency of the schematic with that of the layout. The simulation results show the performance of the CA LNA in both SISO and SIMO operations with good impedance matching, high gain, low noise figure, and good linearity. The S_{11} and S_{22} parameters were below -10 dB and -15 dB from 0.52 GHz-to-4.44 GHz as evidently shown in Fig. 9 and Fig. 11. Additionally, the -3 dB bandwidth also spans from 0.52 GHz-to-4.29 GHz and 0.52 GHz-to-4.44 GHz for SISO and SIMO operations. A 0.15 GHz variation in bandwidth between SISO and SIMO due to the effect of the switch transistors. The gains and noise figures of both the SISO and SIMO were 17.77 dB and 18.30 dB, 2.88 dB and 2.82 dB

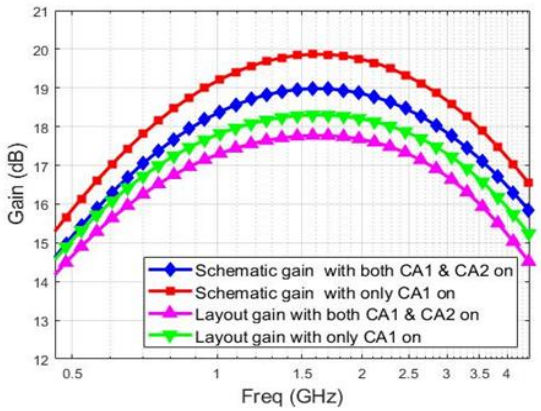

Fig. 8. Simulation results: power gain(S_{21}).

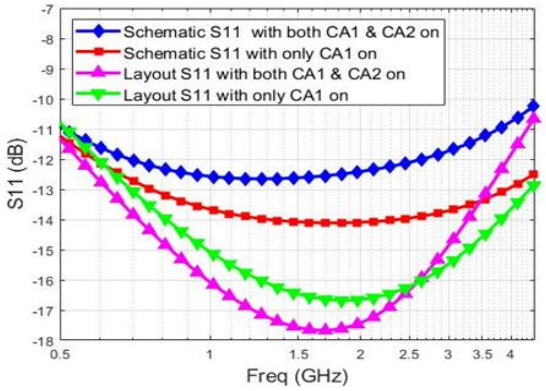

Fig. 9. Simulation results: input impedance matching(S_{11}).

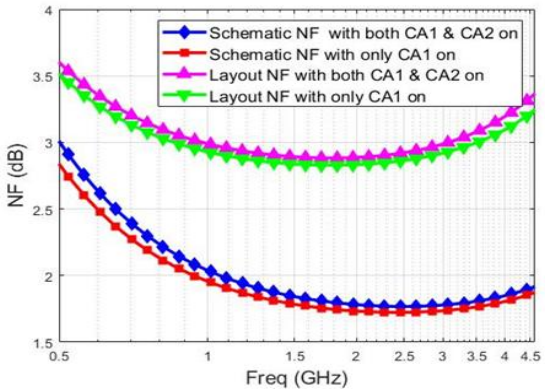

Fig. 10. Simulation results: noise figure(NF)

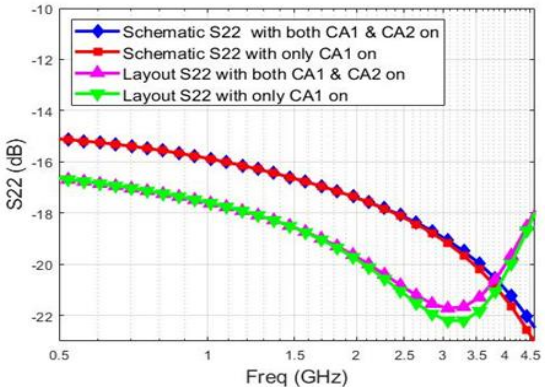

Fig. 11. Simulation results: output impedance matching(S_{22})

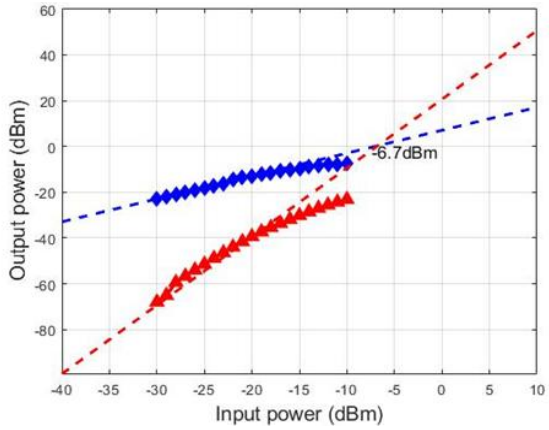

Fig. 12. Simulation result : third-order input intercept point (IIP_3)

respectively. The 0.53dB gain variation comes from the effect of the layout metal layers resistances at the input stage as well as resistor R_{F2}. The simulated IIP_3 showed no significant variation for the different mode of operation and was achieved as -6.7 dBm. The reported results of the layout and schematic designs showed a close relationship as indicated in the various plots.

Ⅵ. Conclusion

This paper proposed a new wideband LNA architecture for CA receiver in LTE-Advanced and 5G. The simulation results compare the schematic versus layout performance and a very good correlation and performance were achieved. A maximum gain of 17.77 dB and 18.30 dB were obtained for SISO and SIMO was 2.88 dB and 2.82 dB respectively and are well below 3 dB. An IIP_3 of -6.7 dBm for SIMO was achieved and varies slightly from SISO by -1 dBm. A very wide band of operation, covering 0.52 GHz to 4.44 GHz was achieved for CA intra-band and inter-band operations for SISO and SIMO operations. The minimum noise figures for SISO and SIMO was 2.88 dB and 2.82 dB respectively and are well below 3 dB. An IIP_3 of -6.7 dBm for SIMO was achieved and varies slightly from SISO by -1 dBm. A very wide band of operation, covering 0.52 GHz to 4.44 GHz was achieved for CA intra-band and inter-band operations. The LNA is capable of achieving up to 8 component carriers hence the receiver can cover the entire LTE-Advanced operational band of 100MHz while operating in a SIMO mode.

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