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A Low-Loss On-Chip Transformer Using an Auxiliary Primary Part (APP) for CMOS Power Amplifier Applications

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Abstract

We propose a low-loss on-chip transformer using an auxiliary primary part (APP) for an output matching network for fully integrated CMOS power amplifiers. The APP is designed using a fifth metal layer while the primary and secondary parts are designed using a sixth metal layer with a width smaller than that of the primary and secondary parts of the transformer to minimize the substrate loss and the parasitic capacitance between the primary and secondary parts. By adapting the APP in the on-chip transformer, we obtain an improved maximum available gain value without the need for any additional chip area. The feasibility of the proposed APP structure is successfully verified.

Key words : CMOS, Efficiency, Magnetic coupling, Matching network, Power amplifier, Transformer

Ⅰ. Introduction

Recently, on-chip transformers for RFIC applications have found many uses owing to their compact size and low cost [1], [2]. In particular, a distributed active transformer (DAT) is considered to have the potential to lend improvements to the performance of a CMOS power amplifier. Since the introduction of the DAT by Dr. I. Aoki [3], many studies about watt-level CMOS power amplifiers have been published. However, the output transformer of a CMOS power amplifier is still regarded as the component which can seriously degrade the overall efficiency of this type of power amplifier. Thus, there have been vigorous attempts to improve the efficiency of on-chip transformers.

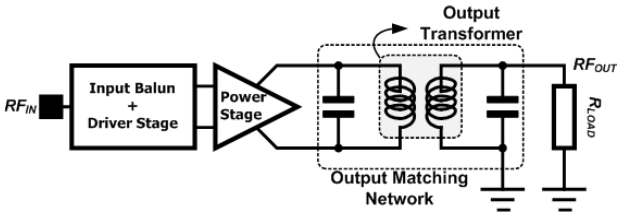

Fig. 1. Simple block diagram of a typical CMOS power amplifier using transformers as an output balun.

Fig. 1 shows a simple block diagram of a typical CMOS power amplifier using an output transformer. In general, given that the power amplifier is designed using a differential structure, an output balun is essential [4]. The output transformer, which acts as the output balun, also

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acts as an output matching network. Accordingly, the loss induced by the output transformer directly degrades the overall efficiency of the CMOS power amplifier [5]-[7]. Research with the goal of minimizing this loss is required to improve the efficiency of the power amplifier.

In this study, we propose a new structure for an on-chip transformer which minimizes its loss through the use of an auxiliary primary part. Using the proposed auxiliary primary part, the loss of the on-chip transformer is reduced without the requirement of a larger area.

II. Structure of a Typical On-Chip Transformer

In general, a transformer is composed of a top metal layer of the given CMOS technology to minimize the loss induced by the magnetic coupling between the transformer and the lossy silicon substrate. In this study, we used the 018-nm RFCMOS process, which provides six metal layers. Accordingly, the top metal layer is the sixth metal layer.

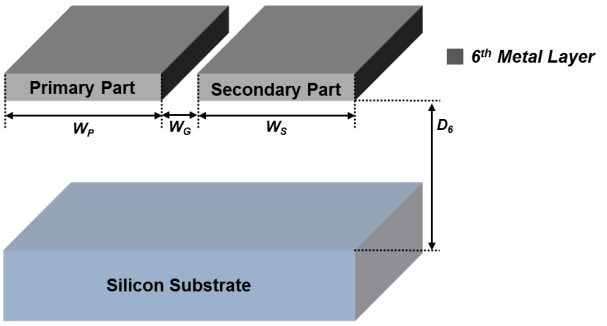

Fig. 2. Typical structure of an on-chip transformer.

Fig. 2 shows the structure of a typical on-chip transformer for the CMOS power amplifier shown in Fig. 1. In general, an edge-side coupled transformer uses the top metal layer, which is the thickest of all of the metal layers used for the primary and secondary parts, as shown in Fig. 1. Given that the top metal layer has lowest resistance and that it is located the greatest distance away from the lossy silicon substrate out of all metal layers, the use of an edge-side coupled transformer can minimize the loss induced by the resistance and undesired magnetic coupling between the transformer and the substrate. However, the magnetic coupling between the primary and the secondary parts is limited at the edges of these parts and hence degrades the coupling factor, k.

III. The Proposed Auxiliary Primary Part of the On-Chip Transformer

Fig. 3 shows the structure of the proposed on-chip transformer using an auxiliary primary part. In Fig. 3, for the sake of simplicity, the silicon substrate is omitted. In the proposed on-chip transformer, the designed auxiliary primary part is attached to the primary part using the fifth metal layer. The auxiliary primary part and the primary part are connected through via-holes. As shown in Fig. 3, given that the interaction between the primary and secondary parts is enhanced by virtue of the added auxiliary primary part, the coupling factor, k, is improved compared to that of an edge-side coupled transformer.

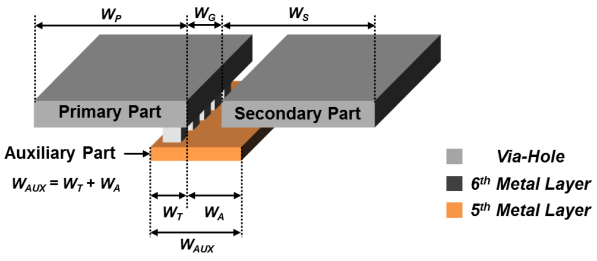

Fig. 3. Proposed on-chip transformer using the auxiliary primary part.

Additionally, most RF currents of primary and secondary parts are concentrated at the edges, near each other. Thus, the auxiliary primary part proposed here can improve the magnetic coupling between the primary and the secondary parts.

IV. Results

To prove the feasibility of the proposed transformer structure, we conducted a 2.5D electromagnetic (EM) simulation. In this study, we fixed W_P and W_S at 50 μm; this value is one of the most commonly used widths of an integrated output transformer for a CMOS power amplifier with watt-level output power. The length of the primary and secondary parts of the transformer is fixed at 1.0 mm for a general 1.9-GHz CMOS power amplifier [1], [3]. W_G and D_6 in Figs. 2 and 3 are 3 μm and approximately 8 μm, respectively.

Fig. 4 provides the EM simulation results of a typical and of the proposed transformer according to the operating frequency with various values of W_A ranging from 2 to 10 μm. As shown in Fig. 4, the simulated maximum available gain (MAG) of the proposed structure is higher than that of the typical structure.

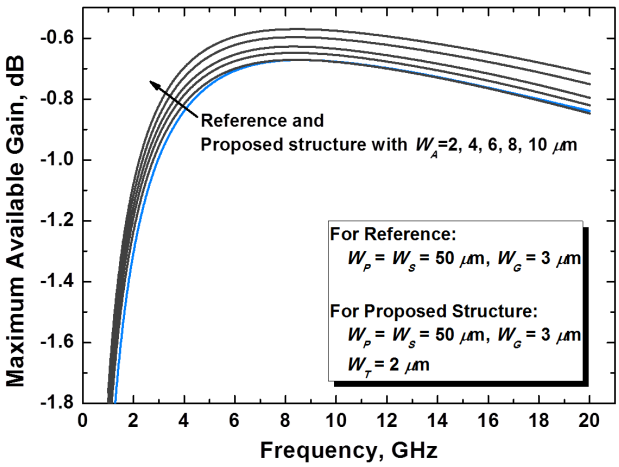

Fig. 4. Maximum available gains of the typical and proposed transformers according to the operating frequency (length of primary and secondary part: 1.0 mm).

As shown in Fig. 5, we checked the MAG of the typical and proposed structure at an operating frequency of 1.9 GHz. As shown in Fig. 5, the MAG of the proposed structure gradually increases according to W_A. However, an excessive W_A will introduce excessive parasitic capacitance between the primary and secondary parts of the transformer. This parasitic capacitance can degrade the bandwidth of the CMOS power amplifier. Accordingly, the value of W_A should be determined in consideration of the required bandwidth and efficiency of the given CMOS power amplifier. As shown in Figs. 3 and 5, the MAG of the proposed transformer is improved without the need for any additional chip area.

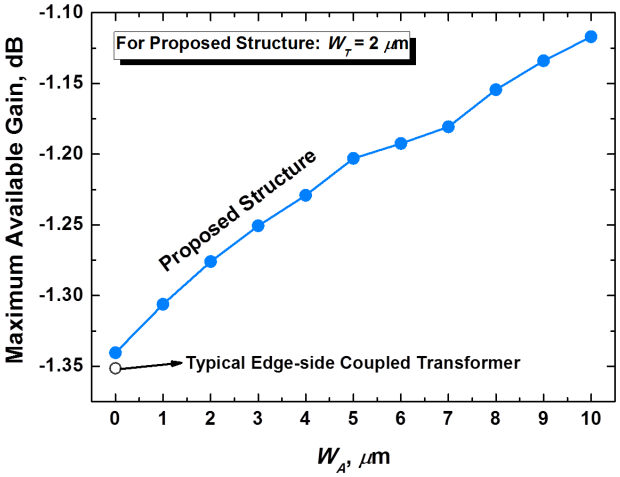

Fig. 5. Maximum available gains of the typical and proposed transformers according to WA (length of the primary and secondary part: 1.0 mm).

V. Conclusion

In this study, we proposed a low-loss on-chip transformer using an auxiliary primary part (APP) for RF CMOS power amplifier applications. The APP elevates the magnetic coupling between the primary and secondary parts of the transformer and hence improves the maximum available gain (MAG) compared to that of a typical edge-side coupled transformer. The required chip area for the proposed transformer is identical to that of a typical transformer. Although we investigated the MAG of the transformer for the output balun of a 1.9 GHz CMOS power amplifier in this study, the design concept of this study can easily be adapted to other circuit applications where a transformer is required.

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