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Analysis of Gate-Oxide Breakdown in CMOS Combinational Logics

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Abstract

As CMOS technology scales down, reliability is becoming an important concern for VLSI designers. This paper analyzes gate-oxide breakdowns (i.e., the time-dependent dielectric-breakdown (TDDB) aging effect) as a reliability issue for combinational circuits with 45-nm technology. This paper shows simulation results for the noise margin, delay, and power using a single inverter-chain circuit, as well as the International Symposium on Circuits and Systems (ISCAS)'85 benchmark circuits. The delay and power variations in the presence of TDDB are also discussed in the paper. Finally, we propose a novel method to compensate for the logic failure due to dielectric breakdowns: We used a higher supply voltage and a negative ground voltage for the circuit. The proposed method was verified using the ISCAS'85 benchmark circuits.

Keywords: TDDB, gate-oxide breakdown, aging effect

1. INTRODUCTION

As CMOS technology scales down, the time-dependent dielectric breakdown (TDDB), also called a gate-oxide breakdown, is considered to be one of the most important causes of temporal degradation in CMOS devices [1].

When the insulating properties of the silicon dioxide in the CMOS gate wear out, a conducting path is formed through the oxide to the substrate. Because of this conducting path, it is no longer possible to control the current flow between the drain and source by controlling the gate voltage.

As the technology scales down, the gate-oxide thickness of CMOS devices scales as well. Nowadays, oxide thicknesses of less than 2 nm are common in state-of-the-art technologies [2,3]. Moreover, the saturating trend for supply-voltage scaling creates a large electric field in the gate oxide, which forms tunneling currents. The lifetime of a particular gate is determined by the total amount of charge that is carried through the gate oxide by the tunneling current. Therefore, current nano-size devices are more prone to oxide breakdown than larger technologies.

Oxide breakdowns can be categorized into hard breakdowns (HBD) and soft breakdowns (SBD). An HBD is considered to be a catastrophic failure of the device and, hence, the entire circuit. Compared to an HBD, the conductance of an SBD is limited and strongly non-linear [4]. Therefore, it is important to analyze the TDDB impact on the performance of digital circuits in deeply scaled technology and compensate for the TDDB impact using circuit-design techniques.

In this paper, the TDDB impact on a digital circuit is analyzed for a 45-nm–technology node using an inverter chain, a ring oscillator, and the International Symposium on Circuits and Systems (ISCAS)'85 benchmark circuits. In this paper, we demonstrate the speed and power variations due to the presence of TDDB and different TDDB levels. Moreover, we propose a novel TDDB compensation method to correct system failures due to HBDs.

2. GATE-OXIDE BREAKDOWN

Intrinsic gate-oxide failures are caused when the material wears out, due to the long-term damage induced by currents flowing through the oxide. A measure of the intrinsic oxide breakdown is referred to as the TDDB, i.e., the time for a gate oxide to manifest breakdown when subjected to voltage and temperature stresses.

The TDDB can be expressed as the gate-oxide breakdown

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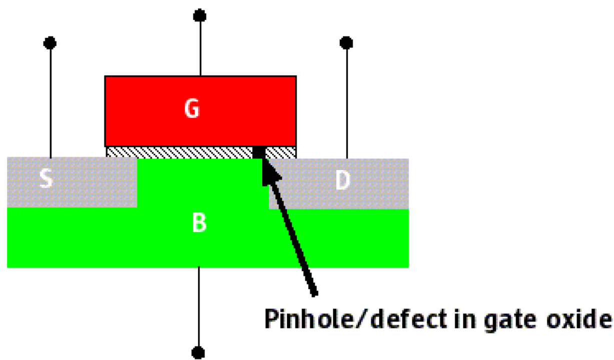

Fig. 1. TDDB effect, cross-section view

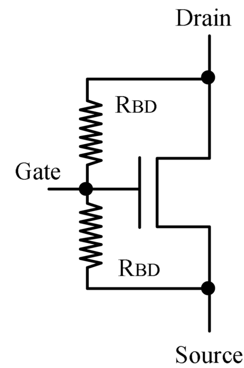

Fig. 2. TDDB model for NMOS

failure rate or the failure in time (FIT). The lower the TDDB is, the higher the failure rate or FIT is. At current MOSFET operating voltages, the most widely accepted degradation model is the "trap creation" process, which is attributed to hydrogen released from the anode. Hydrogenous species (either protons or atomic hydrogen) are freed from the silicon layers by energetic electrons and then drift and diffuse through the oxide, reacting with the lattice to produce traps and other defects.

A breakdown occurs when a series of connected traps develops across the gate oxide, forming a conducting path from the gate to the substrate, or the gate to the source and drain, as shown in Fig. 1. The precise point at which the breakdown occurs is statistically distributed. As a result, only statistical averages can be predicted. For this reason, a large gate-oxide area must typically be used to detect the breakdown.

A gate-oxide breakdown manifests itself as an increase in gate current, while retaining its insulating properties; this happens when the I-V curve becomes linear, i.e., manifests resistor-like behavior. For thinner gate oxides (<= 30e-10, an SBD is the most likely event.

In this paper, we use the TDDB device model proposed in [5,6]. As shown in Fig. 2, the gate-to-channel tunneling current is modeled using breakdown resistors (R_{BD}) from the gate to the drain and source. The R_{BD} values range from GΩ (no TDDB) to a few hundred KΩ (HBD). This time-dependent gate-to-source/drain resistance model was experimentally verified in [7,8]. The simulations performed in this paper only consider n-channel MOSFET (NMOS) devices suffering from a TDDB. In terms of the time to oxide breakdown, p-channel MOSFET (PMOS) devices are an order of magnitude higher than NMOS devices, according to [9,10].

Other papers have also used a single resistor path to model TDDB, e.g., [2]. To analyze the TDDB effect using these two models, we used an inverter chain that consists of three inverters, where the middle inverter suffers from a TDDB.

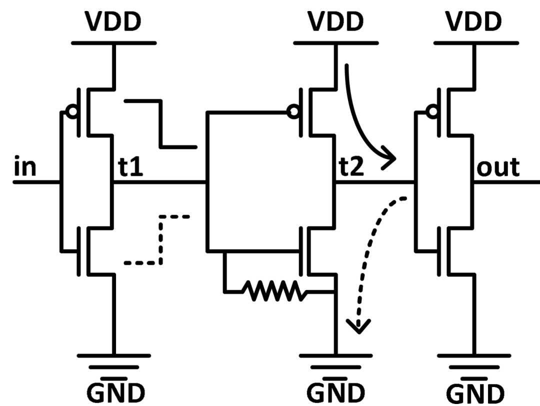

Fig. 3. Single-path model

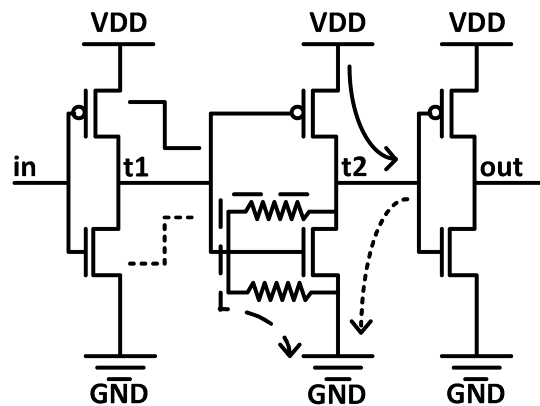

Fig. 4. Dual-path model

When node t1 is asserted to a logical '1', the NMOS of the second inverter is turned on. Node t2 is pulled down to ground by the NMOS with one resistor, as shown in Fig. 3, or two resistors, as shown in Fig. 4. The dual-path TDDB model has a faster discharging time than the single-path TDDB model. Therefore, its average delay can be reduced, compared to the single-path TDDB model and the no-TDDB case.

The simulation results for Fig. 3 and Fig. 4 show that the delay using the dual-path model is reduced to 13% compared to that of the single-path model. Compared to the no-TDDB case, the delay using the dual-path model is reduced to 13.3%. The breakdown case in Fig. 4 was analyzed using the HSPICE circuit simulator with 45-nm PTM technology and V_{dd} = 1.0 V.

3. GATE-OXIDE BREAKDOWN ON DIGITAL CIRCUITS FOR DEEPLY SCALED TECHNOLOGY

3.1 Noise Margin

In terms of an inverter's voltage-transfer characteristics, the oxide breakdown in an NMOS transistor results in an upward shift of the voltage-outward-low (V_{OL}) value, as illustrated in Fig. 5. There is no downward shift of the voltage-outward-high (V_{OH}) value because we assumed that only NMOS transistors have the oxide-breakdown effect.

In Fig. 5, when the TDDB occurs on the NMOS transistors, the noise margin (especially NM_L) is decreased. However, for NM_H, it is almost the same as the no-TDDB case. The NM_H is reduced slightly, due to the increase of the voltage-inward-high (V_{IH}) value. Therefore, with the presence of TDDB, the noise margin is reduced and will be further reduced if the TDDB worsens.

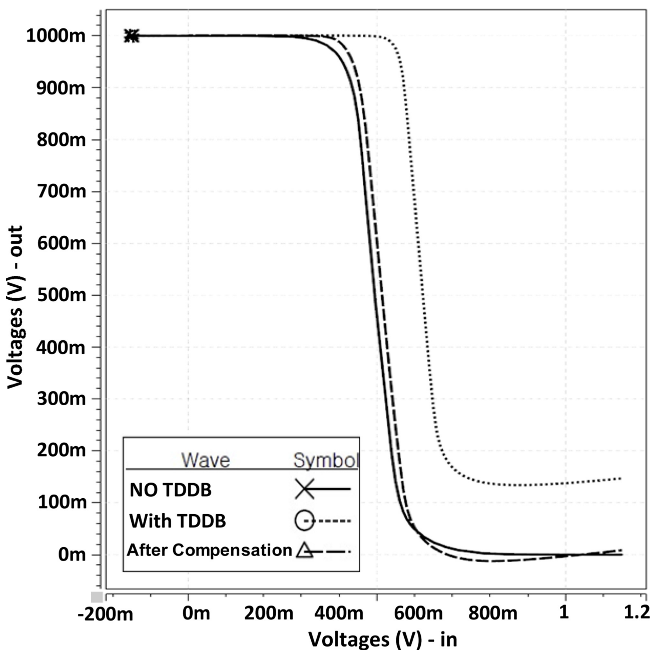

Fig. 5. Noise-margin analysis

3.2 Power Consumption and Speed Variation

To demonstrate the power variation and speed variation with the presence of a TDDB, we simulated an inverter chain with 101 inverters, and inserted TDDB resistors at random locations with random resistor values (from 100 KΩ to 300 KΩ).

Table 1 shows that, as the percentage of TDDB gates in the inverter chain increases, the total power consumption increases and the total delay decreases.

Table 1. Simulation Results for Inverter Chain with TDDB

Percentage of TDDB gates (%)	Total power (W)	Total delay (s)
0	5.75E-06	9.02E-10
10	8.36E-05	8.88E-10
20	1.21E-04	8.80E-10
30	1.98E-04	8.76E-10
40	2.57E-04	8.72E-10
50	3.30E-04	8.59E-10
60	3.48E-04	8.58E-10
70	4.41E-04	8.50E-10
80	5.05E-04	8.36E-10
90	5.21E-04	8.29E-10
100	6.12E-04	8.21E-10

3.3 Reverse Body Biasing

As shown in Fig. 6 and Fig. 7, the reverse body-biasing (-.04 V and -1V) for NMOS devices reduces the power consumption and increases the delay in the presence of TDDB gates.

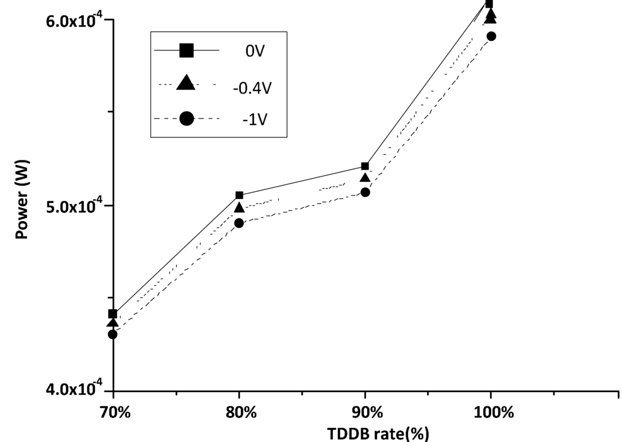

Fig. 6. Power vs. reverse-body biasing

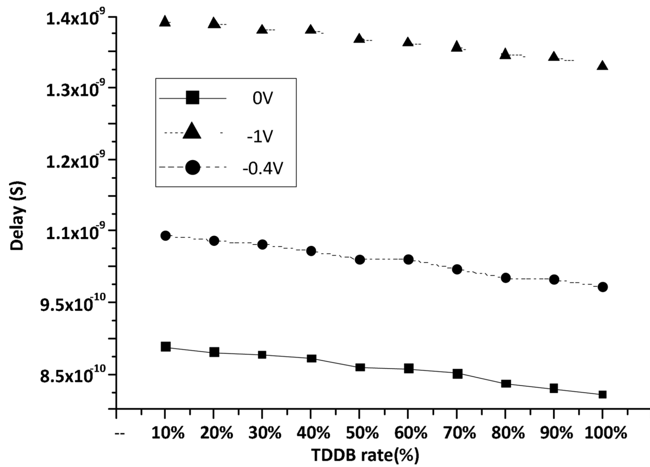

Fig. 7. Delay vs. reverse body biasing

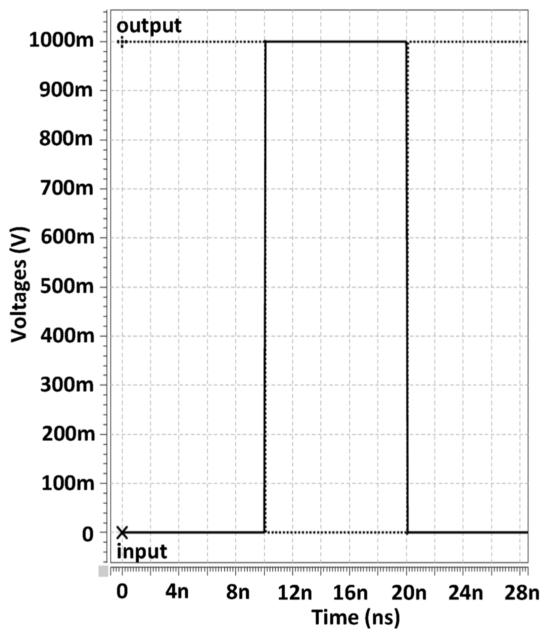

Fig. 8. Input and output waveform before HBD

3.4 Logic Failure Due to Hard Breakdown

A severe TDDB condition is considered to be a hard breakdown, which results in a system failure. We simulated an inverter chain with five inverters. Fig. 8 and Fig. 9 compare the inverter chain behavior before and after the HBD. As shown in Fig. 9, the HBD prevents the output from toggling; however, the output voltage shrinks due to the break-down path from the NMOS gate to the drain.

4. COMPENSATION METHOD FOR GATE-OXIDE BREAKDOWN

When the logic suffers from severe TDDB, e.g., an HBD, it can

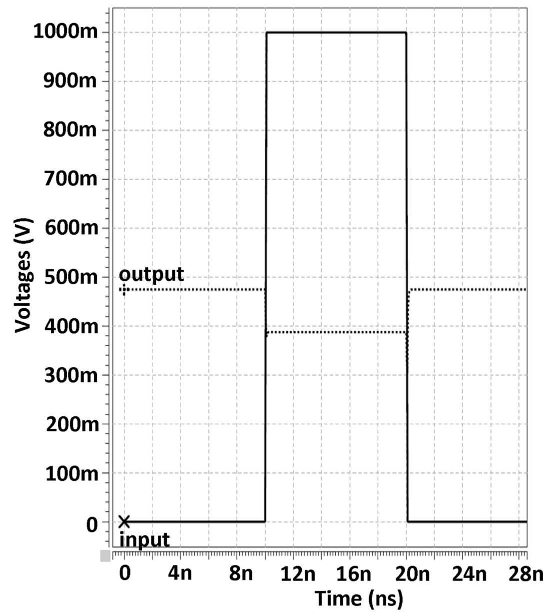

Fig. 9. Input and output waveform after HBD

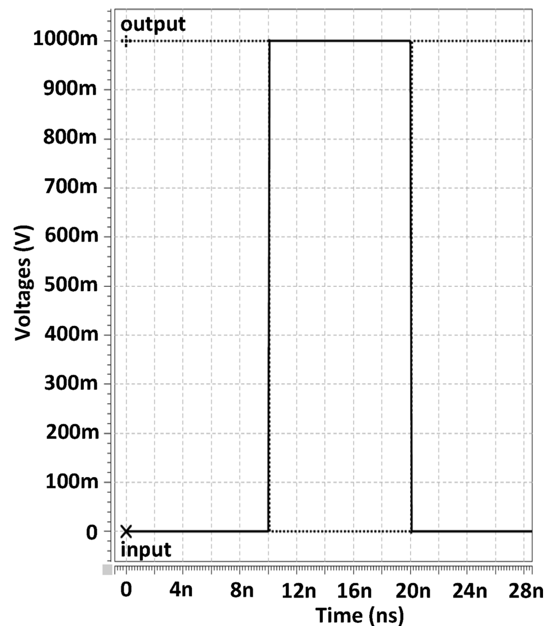

Fig. 10. Input and output waveform before HBD

cause system or logic failures. We tried to compensate the logic and system with a higher supply voltage and a negative ground voltage. First of all, we used an inverter chain with no TDDB stress, and the logic worked correctly, as shown in Fig. 10.

As shown in Fig. 11, the HBD prevents toggling at the output. The output voltage is decreased, compared to Fig. 10, due to the breakdown path from the gate to the drain in the NMOS. Therefore, the logic function can no longer be operated as an inverter chain.

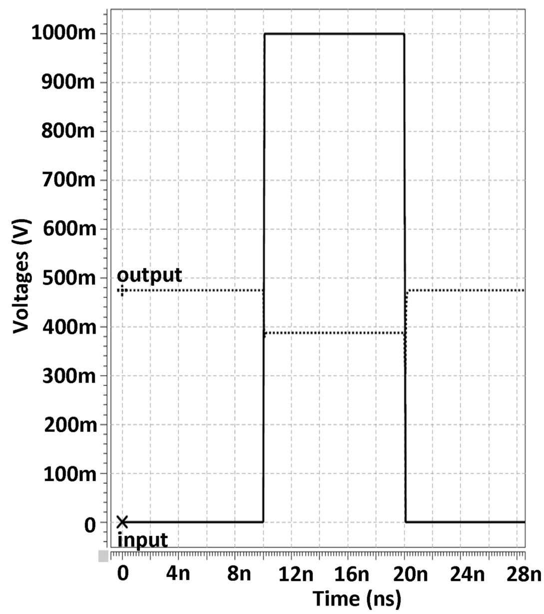

Fig. 11. Input and output waveform after HBD

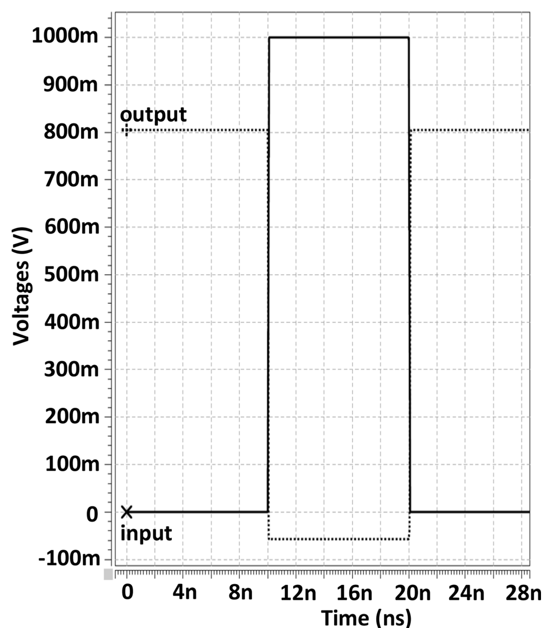

Fig. 12. Input and output waveform after compensation

After we apply a higher supply voltage (1.20 V) and a negative ground voltage (-0.20 V), we can obtain the waveform shown in Fig. 12. It works properly; however, the total power increases by 72.43% and the average delay increases by 48.36%.

For the ISCAS-circuit compensation, we tried to compensate only for a system-failure situation. As a higher supply voltage and a negative ground were asserted, the ISCAS testbench circuits consumed more power. However, our purpose was only for the system to work correctly (i.e., we ignored the power overhead.)

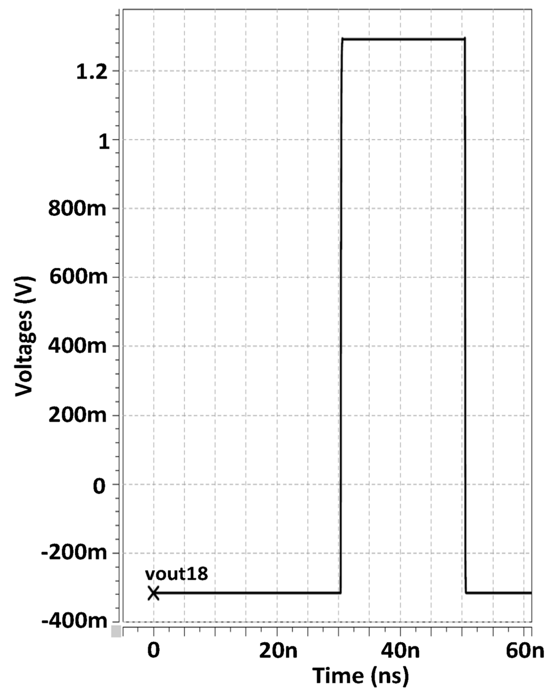

Fig. 13. c3540 circuit Output waveform after compensation

When we increase the supply voltage to 1.35 V and decrease the ground voltage to -0.35 V, the correct waveform, shown in Fig. 13, is generated.

5. CONCLUSIONS

In this paper, we simulated and analyzed the time-dependent dielectric-breakdown (TDDB) aging effect for a combinational circuit and ISCAS'85 benchmark circuits with 45-nm technology. This paper showed the simulation results for noise margin, delay, and power using a single inverter-chain circuit, as well as the ISCAS'85 benchmark circuits. In addition, we proposed a novel method to compensate for the logic failure due to dielectric breakdowns. We used a higher supply voltage and a negative ground voltage. The proposed method was verified using the ISCAS'85 benchmark circuits.

REFERENCES

[1] J.H. Stathis, "Physical and predictive models of ultra thin oxide reliability in CMOS devices and circuits," in *Proc. Intl. Reliability Physics Symposium*, pp. 132-149, 2001.

[2] M. Choudhury, V. Chandra, K. Mohanram, R. Aitken, "Analytical model for TDDB-based performance degra-

dation in combinational logic," in Design, Automation & Test in Europe Conference & Exhibition (DATE), pp. 423-428, 2010.

[3] T. Nigam, A. Kerber, P. Peumans, "Accurate model for time-dependent dielectric breakdown of high-k metal gate stacks," in *Proc. Intl. Reliability Physics Symposium*, pp. 523-530, 2009.

[4] B. Kaczer, R. Degraeve, "Gate oxide breakdown in FET devices and circuits: From nanoscale physics to system-level reliability," in *Microelectronics Reliability*, vol. 47, pp. 559-566, May 2007.

[5] J. Fang, S.S. Sapatnekar, "Scalable methods for the analysis and optimization of gate oxide breakdown," in *Quality Electronic Design* (ISQED), pp. 638-645, 2010.

[6] H. Wang, M. Miranda, F. Catthoor, D. Wim, "Impact of random soft oxide breakdown on SRAM energy/delay drift," *IEEE Trans. Device and Mater. Rel*., Vol. 7, No. 4, pp. 581-591, December 2007.

[7] T. Wee Chen, Y. M. Kim, K. Kim, Y. Kameda, M. Mizuno, S. Mitra, "Experimental study of gate-oxide early life failures," in *Proc. Intl. Reliability Physics Symposium*, pp. 650-658, 2009.

[8] S.S. Lombardo, J.H. Stathis, B.P. Linder, K.L. Pey, F. Palumbo, C.H. Tung, "Dielectric breakdown mechanisms in gate oxides," *Journal of Applied Physics*, Vol. 98, No. 12, pp. 1-36, 2005.

[9] B. Kacze, R. Degraeve, M. Rasras, K. V. de Mieroop, P. J. Roussel, G. Groeseneken, "Impact of MOSFET gate oxide breakdown on digital circuit operation and reliability," *IEEE Trans. Electron Devices*, Vol. 49, pp. 500-506, 2002.

[10] R. Rodriguez, R.V. Joshi, J.H. Stathis, C.T. Chuang, "Oxide breakdown model and its impact on SRAM cell functionality," in *Simulation of Semiconductor Processes and Devices*, pp. 283-286, 2003.