Electrical Loss Reduction in Crystalline Silicon Photovoltaic Module Assembly: A Review

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ABSTRACT: The output power of a crystalline silicon (c-Si) photovoltaic (PV) module is not directly the sum of the powers of its unit cells. There are several losses and gain mechanisms that reduce the total output power when solar cells are encapsulated into solar modules. Theses factors are getting high attention as the high cell efficiency achievement become more complex and expensive. More research works are involved to minimize the "cell-to-module" (CTM) loss. Our paper is aimed to focus on electrical losses due to interconnection and mismatch loss at PV modules. Research study shows that among all reasons of PV module failure 40.7% fails at interconnection. The mismatch loss in modern PV modules is very low (nearly 0.1%) but still lacks in the approach that determines all the contributing factors in mismatch loss. This review paper is related to study of interconnection loss technologies and key factors contributing to mismatch loss during module fabrication. Also, the improved interconnection technologies, understanding the approaches to mitigate the mismatch loss factors are precisely described here. This research study will give the approach of mitigating the loss and enable improvement in reliability of PV modules.

Key words: Photovoltaics, Solar cells, Solar modules, Interconnections, Mismatch, CTM

Nomenclature

V_{OC} : open circuit voltage

I_{SC} : short circuit current

FF: Fill Factor

P_{max} : Maximum Power

Subscript

c-Si : crystalline silicon

PV : photovoltaic

CTM : cell-to-module

CTMV : cell-to-module variance

CTE : coefficient of thermal expansion

T&S : Tabbing and Stringing

R_{ts} : Tabbing and Stringing Resistance

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1. Introduction

PV modules are in huge demand among worldwide green energy resources as they are now used to supply electrical power and considered as good replacement of fossil fuel. The modules are fabricated by interconnecting number of solar cells in series through few steps. This processing leads to different loss and gain mechanisms.

Due to this, the total output power of a module of series connected solar cells is less than the sum of the power of all solar cells. It is known as cell to module loss. Fig. 1 shows the factors that contributing in the final module efficiency reduction. Several past research works have grouped those factors into three parts: Geometrical Factors, Optical Factors and Electrical Factors[1-4]. The focus of this paper is to study the sources of electrical losses and how they can be optimized. From Fig. 1 we can observe that electrical loss accounts for 0.75% of overall reduction in cell to module efficiency. One of the key challenges to reduce electrical loss is to optimize untimely failure of solar cell interconnection. Interconnection is building the series connection between cells. It governs the electrical property of
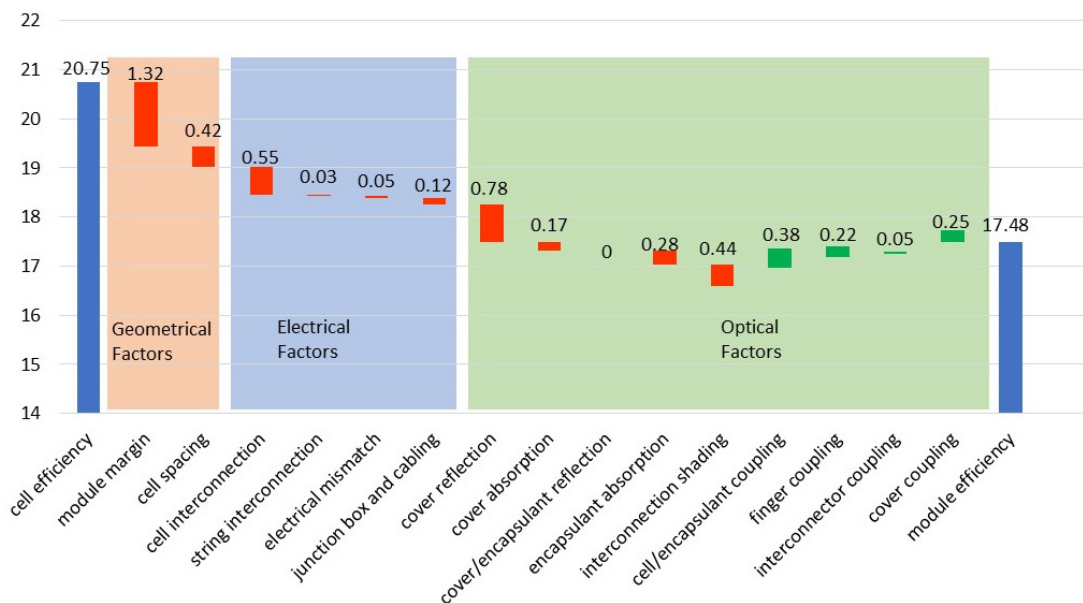
Fig. 1. CTM Loss Factors

the module. Report says among all reasons of module failure ~40.7% PV modules fail due to interconnection[5]. The interconnections allow the electrical, thermal and mechanical contact between solar cell and electrodes. Temperature cycling during module's field operation causes the degradation of soldering joints resulting in interconnection failure. Current challenge in PV module manufacturing is identifying the reliability of PV interconnections and approaching new soldering technologies. Another important factor to optimize electrical loss is reducing mismatch loss. Due to manufacturing variance and variation in operation condition, the individual cells operation faces a deviation from their individual maximum power capacity. It causes a small loss in output power and is known as "mismatch-loss". Many research attempts are made to investigate the sources of mismatch loss which reduced its contribution in CTM loss to 0.05%. According to the reports of International Technology Roadmap for Photovoltaics, 0.0% mismatch loss is achievable in upcoming years[6]. Also, junction box and cabling are key reasons of electrical loss which contributes 0.1% in overall CTM loss[7]. This article reviews different sources of electrical loss factors and new approaches to improve them. Also, new interconnection and soldering technologies, identification of reliable PV modules, examining the sources of mismatch loss discussed precisely. Aim of this review paper is to find appropriate technologies to enhance CTM ratio.
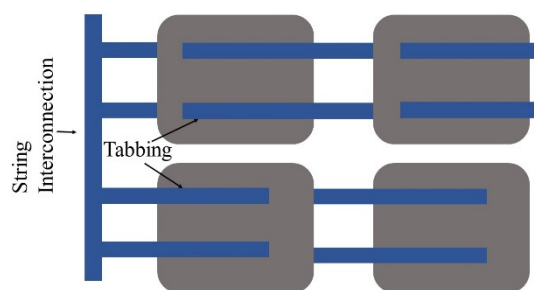

Fig. 2. Cell Interconnection and String Interconnection

2. Types of Electrical Losses in PV module

2.1 Interconnection Loss and Calculation approach

A single solar cell consists an array of gridlines of width < 0.4mm. Current in the solar cell is collected by busbars which is also metallization directly on the solar cell. Finer gridlines and low resistant busbars enable high I_{SC} and FF[8]. A set of c-Si solar cells are connected in series to from a string by cell interconnect ribbon during module fabrication[9]. Multiple strings are associated with 'string interconnect'. This is located nearly to the module edge and sometimes may be covered with module frame or cover layers[10]. Fig. 2 shows a schematic diagram of cell interconnect and string interconnect. The challenges of interconnection process of c-Si cells in PV modules includes thermo-mechanical stress, series resistance and shadowing loss[11,12]. Interconnection by soldering process is difficult and a high temperature process which occurs at about 250°C[13]. The Infra-red reflow soldering involves high thermo-mechanical
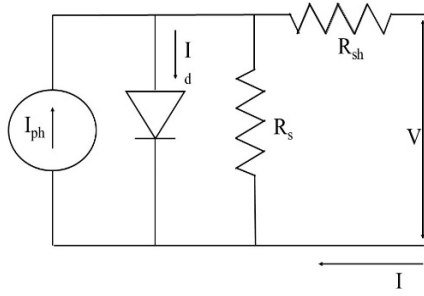
Fig. 3. One Diode Model of Solar Cell

Fig. 4. Cell Interconnection and Current Flow between them

strain to the solder joints which may cause fatigue related damages. It is one of the key challenges of interconnection technology. Series resistance loss is another major challenge in interconnection technology. Metallization for contact formation and tabbing accounts for these losses. Calculating the conversion losses due to T&S is not simple and straight-forward. Here we have discussed some approaches based on previous research. This suggests one diode model of a solar cell, as shown in Fig. 3, is a method which can be used to measure the conversion loss due to T&S[14]. The relation between cell current (I) and voltage (V) satisfies the following equation[15]:

$$I = I_{ph} - I_0 \left[\exp\{(V+IR_S)/nV_T\} - 1 \right] = -(V+IR_S)/R_{Sh} \qquad (1)$$

Where, I_{ph}: photo-generated current

$\quad\quad R_S$: series resistance

$\quad\quad R_{Sh}$: shunt resistance

$\quad\quad I_0$: saturation current of the diode

$\quad\quad n$: Ideality Factor

the effect of R_S on maximum power (P_{max}) of the cell can be quantified by using Eq. (1) and the CTM conversion loss due to T&S can be determined from the expression derived from above equation. Also, in Eq. (1) the total series resistance of a cell array consists of the bare cell resistance (R_{so}) and resistance due to T&S (R_{st}). Another approach is considered where a typical metallic ribbon makes contact all along the busbar lengths and behaves like a distributed resistance. In this configuration current is collected along the length of the busbars uniformly and flows through the fingers to the nearest busbars. After busbar collecting the current, full cell current is stored at the ribbon end. An accumulative equivalent of distributed resistance observed by the cell can be given by Eq. (2)[16].

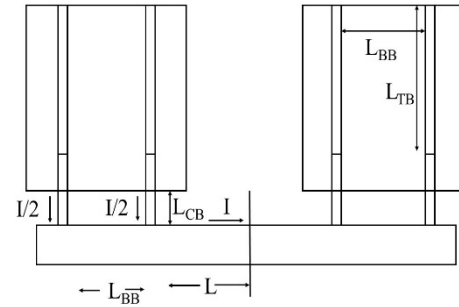$$R_{ts} = \frac{1}{3}\rho_{rib}\left(\frac{L_{rib}}{W_{rib}t_{rib}}\right) \qquad (2)$$

Where, ρ_{rib}: resistivity of the metallic ribbon

$\quad\quad L_{rib}, W_{rib}, t_{rib}$: length, width and thickness of the ribbon respectively

If there is a gap between the cells in an array, we can directly use the combined resistance. The cell-to-cell gap series resistance for a cell with two busbars can be given by following expression,

$$\frac{1}{2}\rho_{rib}\left(\frac{L_{CTC}}{W_{rib}t_{rib}}\right)$$

and for a 3 busbars cell:

$$\frac{1}{3}\rho_{rib}\left(\frac{L_{CTC}}{W_{rib}t_{rib}}\right)$$

Where, L_{CTC}: length of cell-to-cell gap

In the above expression the resistance due to busbars and the contact resistance is neglected. When the tabbed strings are connected in series by busing, an additional series resistance is introduced by busbars. Fig. 4 shows the schematic diagram of two strings connected in series and the current flow between them. For that configuration, the total resistance due to tabbing-stringing-busing is given by Eq. (3)[17].

$$R_{tsb} = \frac{1}{3}\rho_{rib}\left[\frac{L_{TB}}{W_{rib}t_{rib}}\right] + \rho_{rib}\left[\frac{L_{CB}}{W_{rib}t_{rib}}\right] + \frac{1}{2}\rho_{rib}\left[\frac{L_{BB}}{W_{rib}t_{rib}}\right] \qquad (3)$$

In the above equation, $\rho_{rib}, W_{rib}, t_{rib}$ is the resistivity, width and thickness of the ribbon respectively. W_{Brib}, t_{Brib} are the width and thickness of bussing ribbon respectively. L_{TB} is the length of the soldered ribbon. L_{CB} is the distance between cell edge and bussing ribbon and L_{BB} is the length between two extreme busbars of a single cell. When the bare cell parameters − V_{OC},

I_{SC}, V_m, I_m are measured, they can be used to measure the parameters of one diode equivalent circuit. Once the one-diode equivalent circuit parameters are known, the theoretical estimation of series resistance due to tabbing-stringing-bussing is possible by using Eqs. (2) and (3). In addition, the bare cell resistance is a dominating factor in lower efficiency cells which makes the conversion loss at T&S lower. On the other hand, the loss is higher for high efficiency cells.

Another substantial challenge of interconnection technology is shadowing losses. A wider cell requires a thicker interconnection ribbon for conducting larger currents. Reports[18] suggests that shadowing losses increases proportionally with the increase in the width of the interconnection ribbon. the ribbon strip thickness is restricted by the stress accumulated at the solder joint. The differences in the coefficient of thermal expansion between silicon wafer and interconnection ribbon material is the reason of this stress[19]. Additionally, the bending of the interconnection ribbons at the edge of the wafer causes further stress. This affects the reliability of the whole module assembly[20-24]. In the later section we will discuss about the approaches to reduce the interconnection losses.

2.2 Electrical Mismatch Losses and the calculation approach

Mismatch loss is the difference between the maximum power of a PV module and the total sum of maximum powers of individual cells connected in module. When the cells are encapsulated into module a broader group of changes occur which results in mismatch loss. Optimization in module manufacturing strategies requires proper understanding of mismatch loss. This section reviews the mismatch loss related to electrical interconnection. The loss mechanism which impact the mismatch loss will give an idea to module manufacturers.

2.2.1 Theoretical mismatch loss for interconnection

When the cells are interconnected in series to develop a module, the mismatch loss is proportional to the variance of maximum power current (I_{mp})[25,26], given by following equation:

$$\text{Series Loss}(\%) \propto \sigma_{I_{mp}}^2 \qquad (4)$$

$\sigma_{I_{mp}}$ is the standard deviation of the maximum power current. The typical value of this standard deviation is in the range of 0.5% - 0.6% which accounts for 0.02% - 0.04% loss. But the Eq (4) will be valid only when the interconnected devices will

operate in forward bias, otherwise stated the I_{mp} of each connected cells will be less than the average value of I_{SC} of the all cells. If the cells have faults or shading occurs Eq. (4) is not applicable[27-32]. Similarly, when the cells are connected parallelly, the mismatch loss becomes proportional to the variance of the maximum power point voltage (V_{mp}). The equation is a s follows

$$\text{Parallel Loss}(\%) \propto \sigma_{V_{mp}}^2 \qquad (5)$$

σ_{Vmp} is the standard deviation of the maximum power point voltage[33]. Eq. (5) is free from reverse bias fault risk and applicable for a wider range of standard deviation values of V_{mp}.

2.2.2 Mismatch Loss due to cell−to−cell variance

The variance in the cell's performance leads to mismatch loss and is known as "module level" mismatch loss. Previously this loss had a huge impact on module development[33,34] but in modern photovoltaic technologies the effect is so small and is virtually unmeasurable[35,36] because modern cell performances show less variance when fabricated in mass production. After the fabrication of the photovoltaic cells they are uniformly sorted based on their current or power. The main purpose of the cell sorting is to reduce the cell-to-cell variance. When enough cells are sorted to make a module[37] they are combined to form a "cell packet". Average electrical performance of the cell consisted the cell packet determines the electrical performance of the module developed from those cells. Though it can not be determined perfectly because some variances are introduced during module fabrication process. This is known as Cell to Module Variance (CTMV).

2.2.3 Mismatch loss due to module−to−module variance

Variance in module performance attributes to mismatch loss when they are interconnected in an array. This is known as "array level" mismatch loss. If they are interconnected in a typical series strings Eq. (4) will be applied and for parallel interconnection Eq. (5) can express the loss. To optimize this loss the modules are also sorted according to their I_{mp} and V_{mp}. Research study says that the module sorting to reduce mismatch loss is not a zero-cost process and it may affect the overall cost in large scale production[38-41].

2.2.4 Loss due to cell−to−module variance

Previously we have discussed the interconnection and

encapsulation of cells into modules introduces CTMV[42]. This can provide valuable information about module production quality. The variance due to CTMV is assumed to be the difference between the final module variance and the variance of cell packet average. The relation is shown in Eq. (6)[43]

$$\sigma_{\text{CTM}}^2 = \sigma_{\text{Mod}}^2 - \sigma_{\text{cpAv}}^2 \tag{6}$$

for a perfect module i.e. 0 CTM loss it should be $\sigma_{\text{Mod}}^2 = \sigma_{\text{cpAv}}^2$. The σ_{CTM} is important to calculate the variances of I_{mp} and V_{mp}. If Vmp is changed the additional series resistance is changed as well as σ_{CTM}. Changes in Imp is related to the optical effects during encapsulation process.

2.3 Mismatch Loss Calculation Approach

From past research works three attempts have been identified to compute the mismatch loss at the final stage of module development[44-46]. One of them is significantly important as the only approach that measures the mismatch loss at the ultimate module level via direct experimentation. Though this technique is not enough to accurately calculate the loss for modern manufacturing techniques, and it is not a general method for all module manufacturing strategies. The second method is a mathematical model built for CTM effects which includes mismatch. The third approach is using the expected difference values between module I-V curve and suns-V_{OC} curve to obtain the mismatch loss. Though these two approaches are designed in such a manner that they cannot deal with non-standard condition. So, they cannot detect relatively small mismatch accurately. Later in recent years another approach has been made to overcome the drawbacks of the above methods. Here a hypothetical module of 72 component cells has been considered[47]. The I-V curves of production cells are summarized to form the I-V curve of the hypothetical model and calculate the maximum power and maximum current from the curve. The hypothetical curve is assumed to have no additional series resistance due to interconnections or changes in cell current due top encapsulation[48]. The mismatch loss is obtained by calculating the difference between the sum of maximum powers of 72 different cells and the maximum power of the hypothetical model. The calculation of mismatch loss is as following equation:

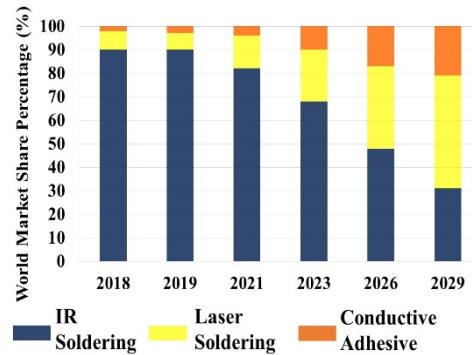$$L = \frac{\sum_{i=1}^{72} p_i - P_{\text{max}}}{\sum_{i=1}^{72} p_i} \tag{7}$$

Fig. 5. Recent and expected market share of different cell interconnection technologies

Where, p_i = maximum power of ith cell

P_{max} = maximum power of the hypothetical module

This approach is the most direct approach of mismatch loss estimation which is validate for modern technologies based on power-current relationship.

2.4 Junction Box Failure

Junction Box protects the cell strings connection to the external terminal. Generally, the box contains the bypass diodes that protects the cell from hot spot or shadowing[49]. But the improper design or incorrectly disclosed junction boxes causes corrosion to the junction box connections due to the moisture entered. This causes wiring failure that results in internal arcing and arcing can initiate fire[50]. Also, back-sheet delamination near junction box causes an unconstrained stress which further introduces a mechanical stress on the components and break them[51].

3. Challenges in optimizing Electrical Loss in PV module

3.1 Interconnection Technology reliability challenge

Previous reports claim that degradation in interconnection occurs as the PV modules are subjected to regular thermal cycles during their in-field operation[52] and introduces additional series resistance[53]. Interconnections in solar cells are primarily done by two techniques. One is soldering technology, and another is using electrically conductive adhesive[54]. In the following sections we will discuss about the reliability of these two technologies on the system performance and degradation during operation. Fig. 5 shows the current market share and future progress of different cell interconnection technologies.

3.1.1 Solder Interconnection Technology

A crucial part of module fabrication is joint interconnections by soldering technology. The solder establishes a connection between ribbon and electrode. The current flows from silicon wafer to ribbon through this connection. The materials like solder, bus-bar, ribbon and silicon wafer are bonded together at the joint. The differences in the coefficient of thermal expansion of those materials are the reasons of thermo-mechanical reliability problems. Soldering technology is a high temperature process. During the process the shearing force on silicon wafer is introduced due to the differences in coefficient of thermal expansions of the bonding materials. This results in fatigue damage in the module as well as grid finger interruption at the edges of bus-bar[55]. Furthermore, the local weather is a key factor that affects the PV module temperature. This influences the degradation of solder interconnection. Lifetime prediction analysis reports claim that same type of c-Si PV modules installed in various locations show different lifetimes[56]. The daily temperature cycle and moisture is involved in metal degradation, cracked grain boundary, additional series resistance and heating[57]. To avoid the conventional soldering problems, researchers developed laser soldering technology for various PV module designs. This technology is highly reliable as it introduces reduced mechanical and thermal stress in solder joints. An experimental investigation report[58,59] suggests that a conventional soldering method induces a peel force ranged between 1-3 N while for laser soldering technology the force is nearly equal to zero. Hence this technology causes less damage in solar cell interconnection. It can be concluded that in near future laser soldering technology can produce reliable and cost-effective interconnection technology.

3.1.2 Electrically Conductive Adhesive Technology

The high temperature soldering technology actuate stress and the on-field operation brings deformation in solar cell. These results in cell distortion, rupturing, cracking and overall module failure. To avoid the above problems the use of electrically conductive adhesive for cell interconnection technology has been adapted. The adhesive, made of silver loaded epoxy resins, are used as alternative bonding to interconnect solar cells[60-62]. since the process is the low temperature it implants low residual stress on joint resulting in less module failure. Also, mechanical properties of the bonded materials at joint subjects to optimal changes due to the use of conductive adhesive and the electrical conductivity at the joint increases. Still this process is associated with some key reliability challenges. During on field operation oxidation of adhesive materials results in degradation. Additionally, adhesive-metal bonding suffers from de-bonding which results in crack, corrosion and system failure.

3.2 Challenges in Mismatch Loss Estimation in field

The mismatch loss for a given set of module categories in the field is influenced by manufacturing and design related factors. For a particular field installation, the modules are sorted according to their power rating with tolerance and current. In addition to that solar irradiation and temperature uniformity also affects the mismatch factors. Previously research works were done on the mismatch loss due to separate type of modules in a large fielded array, the mismatch loss related to the difference between theoretical and actual measured power of module, considering mismatch loss as a function of installation condition and their tolerance power. But there are still some factors which is yet to be considered. One of them is the variation in the condition experienced by individual module operating in the field an array. Also, the precision of the power measuring instrument in a field condition is ignored. The attempt of on-spot calculation of actual mismatch loss of an operating system was not considered yet[63,64]. Power optimizers used to eliminate mismatch loss arguably have no other design features in the array system to reduce mismatch loss. So, when the result is generalized in standard field the loss may be over extended. If the solar panels are chosen according to their power rating and no other sorting, this also do not have an accurate measurement of mismatch loss – it can either be improved or declined[65]. The daily sky conditions also have key influence on the mismatch loss. If the average calculation of mismatch loss is done on clear sky day and cloudy day the value will not be same for the two. Due to no shading loss issues on clear sky day. Another important factor is inverter that converts solar energy into electrical energy[66]. A single central inverter is used to invert energy at every string and simultaneously eliminate parallel mismatch loss, but if the modules are not sorted accordingly the inverters used at group of string make an optimal deference. The three most important factors that needs to be focused to reduce mismatch loss are invariable illumination, uniform temperature and relation between performance under simulated light condition and performance on field condition[67]. Also, the manufacturing and field designs are similarly important in low mismatch loss.

4. Discussions and Future Opportunities

Numerous c-Si PV module designs developed before to minimize electrical losses and several challenges are discussed earlier but no single technique was succeeded to overcome all the challenges. Therefore, more research works needed for cell design and manufacturing. Research work to optimize CTM electrical loss is focused on optimizing series resistance, shadowing and recombination loss, mismatch loss module degradation and induced thermo-mechanical stress. Series resistance mainly arises due to through emitter and base solar cell, contact between metal and silicon and the resistance due to top and rear metal contact. Further research is needed to reduce metal contact resistivity which can also improve the energy conversion efficiency. Interconnection ribbon on the c-Si wafer surface induces shadowing loss. This increases with the increase in interconnection width. To avoid this problem the technology of interconnection at the back of cell is introduced however the technology is complex and expensive. Thus, further development in reducing shadowing loss is required. Thermo-mechanical stress due to the difference between CTE of bonding materials at interconnection causes module degradation and system failure. The parameters of module manufacturing design such as busbar, ribbon, back-sheet dimensions needed to be set accordingly to improve the PV module reliability. Additionally, more improvement is required for conductive electric adhesive required for interconnection to make the PV module more durable and reliable. Mismatch loss reduction approach loss in PV module has developed many theoretical equations and cell sorting methods but that do not involve all the key factors responsible for them mainly the single field conditions. Also, cell sorting increases module variance and further cost is associated with this. The cell sorting for high volume manufacturing does not have a fixed cost and sometimes may be too expensive which further increases the module price. Further cost increases with the system developed for designing and installing modules of different power ratings. Still the manufacturing technology requires cell sorting based on cell color for maintaining product standard and thermal breakdown characteristics for ensuring safety. This concludes further research opportunity for developing more improved cell sorting algorithms that will reduce mismatch loss as well as develop cost effective module systems.

5. Conclusion

In this review paper we presented the different loss mechanisms due to interconnection, mismatch and junction box failure during cell-to-module fabrication. The new technological and theoretical approaches to optimize the loss was also discussed. The proper electrical interconnection technology and novel module design can reduce CTM loss up to 0.0%. It was shown that basic pre-dominant interconnection technology induces thermo-mechanical stress in the cell and joints, increases series resistance and shadowing losses. This paper identified that laser soldering technology and conductive adhesive soldering can overcome those problems and can produce a highly reliable module. Though the adhesive-metal bonding initiates some substantial crack resulting into corrosion induced system failure. It seems major research work in tooling and manufacturing facilities still requires optimizing CTM loss further. Also, we assessed that installation-related issues have significant role in mismatch loss. Better understanding and accurate in-situ loss estimation can minimize the mismatch loss further and cost optimization needs the attention. This paper reviewed all the potential factors occurring mismatch loss and identified some calculation approaches. Further research scopes in cost reduction and loss mitigation strategy was also described.

Acknowledgments

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