A Novel Design of an RF-DC Converter for a Low–Input Power Receiver

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Abstract

Microwave wireless power transmission (MWPT) is a promising technique for low and medium power applications such as wireless charging for sensor network or for biomedical chips in case with long ranges or in dispersive media such. A key factor of the MWPT technique is its efficiency, which includes the wireless power transmission efficiency and the radio frequency (RF) to direct current (DC) voltage efficiency of RF–DC converter (which transforms RF energy to DC supply voltage). The main problem in designing an RF–DC converter is the nonlinear characteristic of Schottky diodes; this characteristic causes low efficiency, higher harmonics frequency and a change in the input impedance value when the RF input power changes. In this paper, rather than using harmonic termination techniques of class E or class F power amplifiers, which are usually used to improve the efficiency of RF-DC converters, we propose a new method called "optimal input impedance" to enhance the performance of our design. The results of simulations and measurements are presented in this paper along with a discussion of our design concerning its practical applications.

Key Words: Microwave Wireless Power Transfer, RF–DC Converter, RF–DC Efficiency, Rectifier, Schottky Diodes.

I. INTRODUCTION

In 1969, an experiment that used a 2.45-GHz continuous wave microwave beam to power a small helicopter was carried out by Professor William C. Brown [1]. In his experiment, the helicopter flew as high as 18.28 m and was supplied with 270 W DC of power from rectennas. Currently, due to the evolution of the semiconductor, microwave power transmission (MPT) has many practical applications if high amount of power is not needed (compared with other requirements). The biomedical industry is a major example; Yakovlev et al. [2] used MPT to transfer energy to implantable biomedical devices, which had receiver chips that consumed close to 2 mW for wireless powering and data transfer. MPT has also been used for energy har-

vesting in radio frequency identification (RFID) tags at 900 MHz by Zoscher et al. [3]. Furthermore, the literature showed us the various designs' key factor which is the radio frequency to direct current (RF–DC) conversion efficiency of the rectifier (or RF–DC converter) being between 55% and 72.5%.

The efficiency of the RF–DC converter is mainly dependent on the diode inside the circuit. That diode not only generates harmonic frequency but also causes the change of the input impedance when the input RF power increases or decreases (as shown in Fig. 1). Chaudhary et al. [4] put forward an idea for a harmonic termination matching technique that improved efficiency moderately at a 140-mW RF input power level. However, because they chose input impedance (which is based on the diode datasheet), choosing input impedance caused a problem,
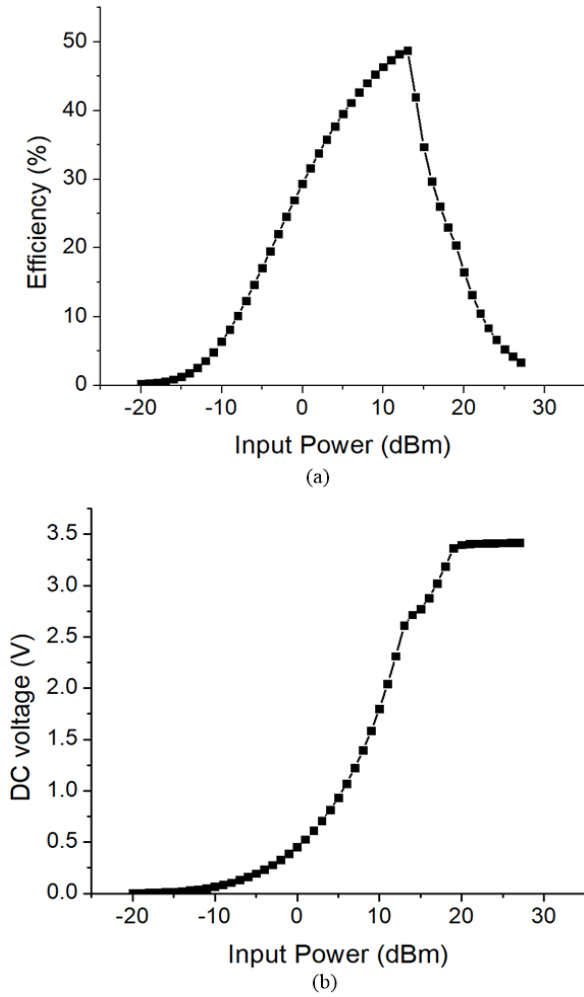
Fig. 1. (a) RF–DC efficiency and (b) DC voltage vs. RF input power level.

which was the mismatch at a low input power. It also resulted in low efficiency (between 0 dBm to 12 dBm), which is usually used for charging biomedical devices.

To overcome rectifier's problems concerning the low input RF power level, we used an optimal input impedance solution combined with the harmonic termination network, as explained below:

- First, the optimal input impedance was found by using the relation between the input power level and the maximum efficiency with an optimal load resistance.

- Second, the harmonic termination (such as in design of class E or class F power amplifiers) is applied to match the optimal input impedance to the receiver antenna impedance. In this paper, we assumed that the receiver antenna impedance was 50 Ω.

II. PRINCIPAL DESIGN OF THE RF–DC CONVERTER

First is the source of the nonlinear property of the diode which was analyzed by Guo et al. [5], who found that, from the

nonlinear junction resistance R_j and the nonlinear parasitic junction capacitance C_j, the nonlinear junction resistance and capacitance could be expressed by the following equations:

$$R_j = \frac{8.33 \times 10^{-5} nT}{I_s + I_b} \tag{1}$$

$$C_j = C_{j0} \left(1 - \frac{V_0}{V_{bi}}\right)^{-M} \tag{2}$$

where n is the ideality factor, T is temperature in Kelvin degree (K) and I_s and I_b are the saturation current and the externally applied bias current, respectively. C_{j0} is the diode zero-bias junction capacitance. V_0, V_{bi} and M are the diode reverse bias voltage, the diode built-in potential voltage and the diode grading coefficient, respectively. From the Eqs. (1) and (2), we can clearly see that the non-linear effect of the Schottky diode relate with the temperature T and the diode reverse bias voltage V_0. While the temperature makes a negligible difference to the change in the resistance of input impedance, the diode reverse voltage can causes an abundant change at the reactance of the input impedance of the circuit. This is because of the relation between the diode reverse bias voltage and the diode voltage V_d as show below:

$$V_0 = \frac{1}{2\pi} \int_{-\pi}^{\pi} V_d d\theta \tag{3}$$

where:

$$V_d = \begin{cases} -V_{bi} + I_{In} R_S \sin(\theta), & -\pi < \theta < 0 \\ V_{In}, & 0 < \theta < \pi \end{cases} \tag{4}$$

where V_d is the diode voltage, R_S is the parasitic series resistance of the diode, and θ is the waveform voltage angle. V_{In} and I_{In} are the voltage and the current of the input signal, respectively.

Second is the harmonic components of the diode that were reported by Chaudhary et al. [4], these harmonic frequency components not only cause DC power dispersion at the output of a diode but they also cause the signal distortion of the fundamental frequency at the input of the rectifier. To overcome this problem, we tried to use the harmonic termination matching network to match the optimum input impedance and terminate the harmonic frequency. In this paper, we choose the optimum impedance is $82.2 - 70.6j$ at an input power of 12 dBm (as shown in Fig. 2).

In Fig. 2, when the input power of the rectifier increases, it causes a change in the circuit's input impedance. Therefore, the RF to DC efficiency and the output DC power of the circuit are affected by that adjustment of input impedance.

The schematic of our design is shown in Fig. 3. In this design, we use the HSMS 2852 Schottky diode which works well at a low RF input power (compared with other diodes) because of
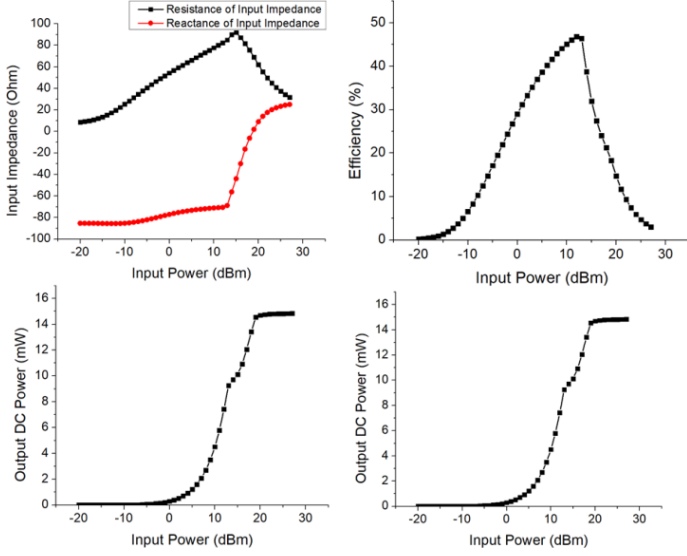
Fig. 2. The optimum impedance vs. output DC power and RF–DC efficiency.
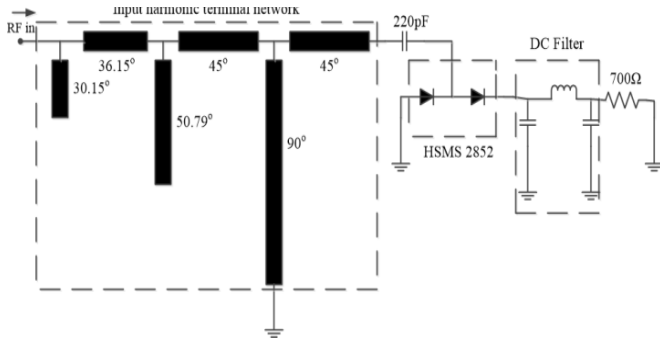

Fig. 3. Schematic of the RF–DC converter circuit.

the efficiency loss and the built-in potential voltage relation.

$$Diode\ loss = \frac{V_{bi}}{V_{DC} + V_{bi}} \qquad (5)$$

where V_{bi} is the built-in potential voltage of the diode, V_{DC} is the DC voltage of the rectifier, and 'diode loss' is the efficiency loss of the diodes.

In the case of the HSMS 2852 [6], the V_{bi} is quite low just 0.35 V while V_{bi} of the other diodes are around 0.5 V.

However, the DC output voltage of HSMS 2852 is lower than the other diodes due to this diode's break down voltage. In general, the DC voltage at the output of a diode is lower than the diode reverse bias voltage and break down voltage V_{br} that mean $V_{DC} < V_0 \le V_{br.}$

III. Results of the Simulation and Experiment

The key part of our design is the input harmonic terminal network (as was illustrated in the previous section). Its electromagnetic (EM) model is shown in Fig. 4 and its EM simulation results are shown in Fig. 5.
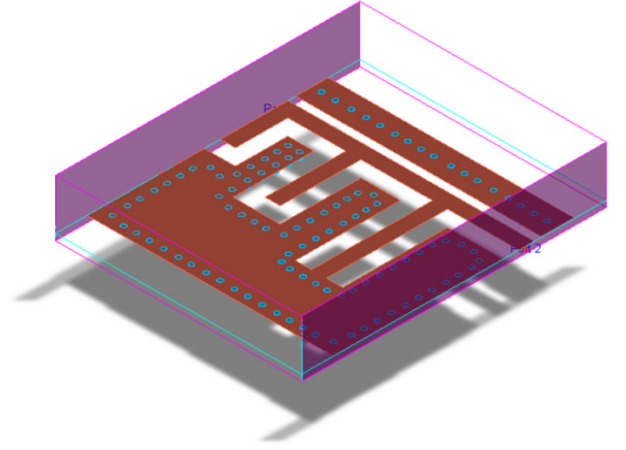

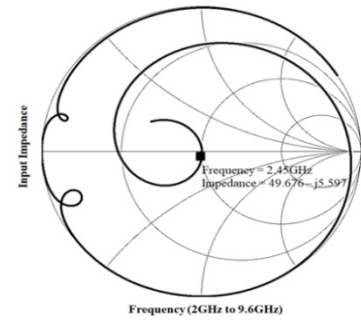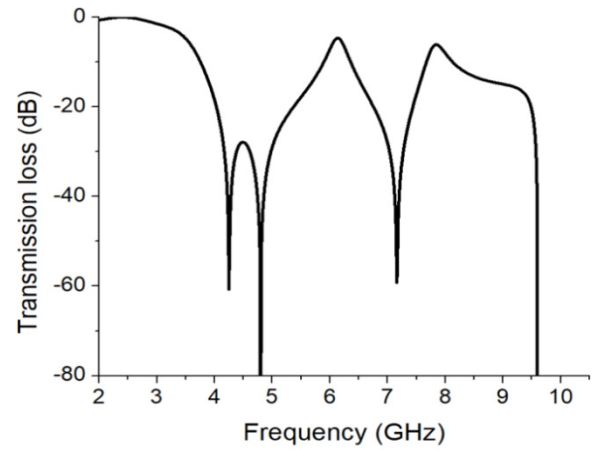Fig. 4. EM model of the harmonic terminal network.

Fig. 5. Simulation results of the harmonic terminal combined with the matching network.

In Fig. 5, we can see the two main functions of the harmonic terminal combined with the matching network technique. First, there is harmonic suppression at the second harmonic frequency, which is achieved using a half wavelength (90°) short-circuit resonator; the harmonic suppression of the third harmonic frequency is achieved by using open stub harmonic trap (30.15°). Second, this technique is also used to match the impedance of the Schottky diode to the antenna's impedance, which is 50 Ω by using a 45° transmission line and a 36.15° transmission line and a 50.79° open stub. The simulation results of the efficiency and DC voltage of our rectifier are shown in Fig. 6. The RF–DC conversion efficiency of our circuit increased 21% compared
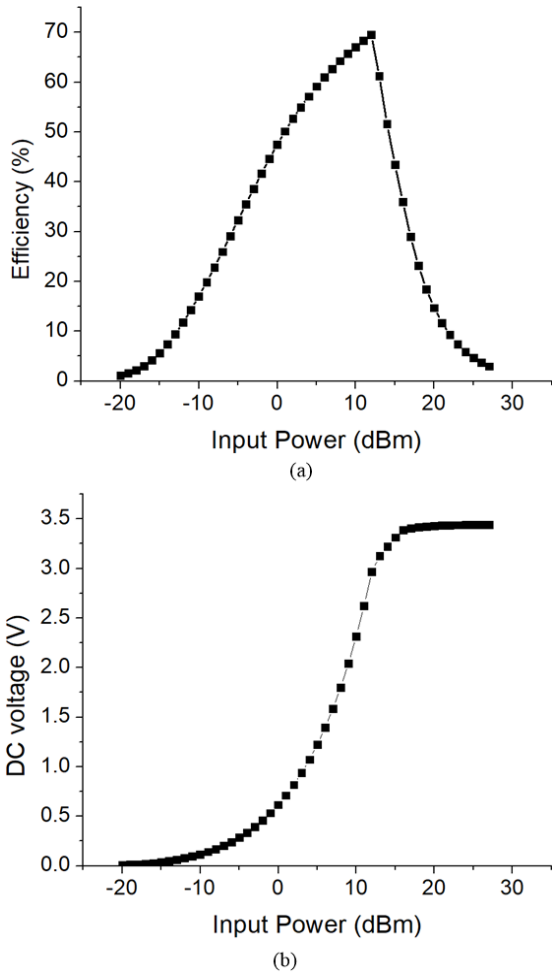
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Fig. 6. (a) The efficiency and (b) DC voltage of the rectifier after using the harmonic terminal combined with the matching network.

Fig. 7. (a) The efficiency and (b) DC voltage of the rectifier after using the general harmonic rejection filters.

to the design without the harmonic terminal (as shown in Fig. 2). There is a 15% improvement in RF to DC efficiency when compared with the general harmonic rejection filters used by Chandravanshi et al. [7]. The harmonic rejection filters was also used in this paper's design at 2nd and 3rd harmonic frequencies and the rectifier's efficiency shown in Fig. 7. The fabrication of this paper's circuit is shown in Fig. 8.

Choosing an optimal load resistor that improves the overall RF–DC conversion efficiency of a circuit is also one of the main parts of our design process. In this paper, the resistor tuning range was chosen to be from 600 Ω to 1.1 kΩ and increased by increments of 50 Ω. Finally, the optimum load resistor was found (as shown in the circuit schematic in Fig. 3).

The size of our circuit was 5 cm × 4 cm; we used the Taconic TLC32–C1 substrate with a height of 0.78 mm. The measurement setup and measurement results are illustrated in Fig. 9. Finally, Figs. 10 and 11 present a comparison between the measurement results and the simulation results for DC voltage and efficiency.

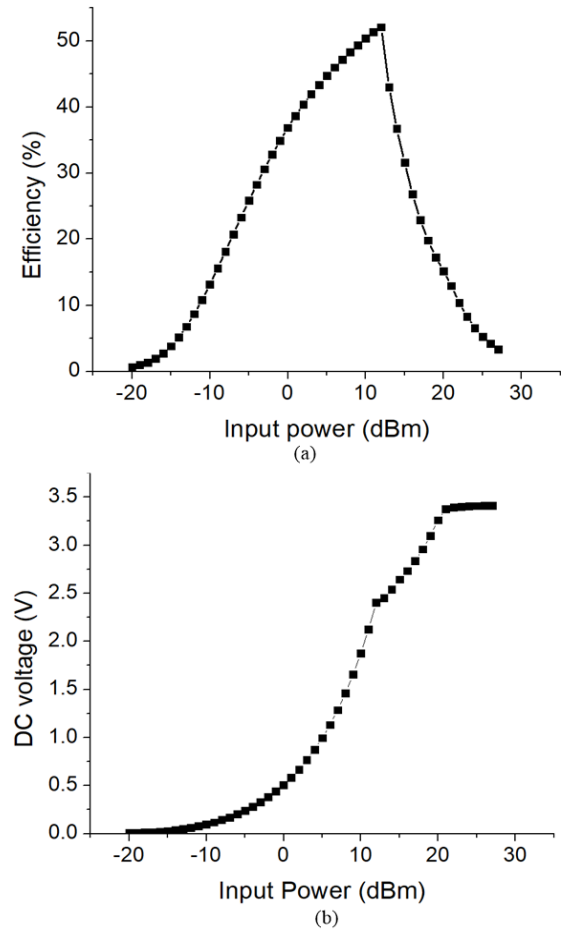In Fig. 9, our rectifier is connected to the signal generator that generates an RF signal power, which is between 8 dBm and 12 dBm. Volt–Ohm–Millimeter (VOM) was used to measure the final DC voltage of our design, to easily capture measurement results and check the life time of the HSMS 2852 diode. We attached the VOM probe to the power line of our design. The DC voltage measurement result was 0.043 lower than the simulation result. This may due to the loss of the substrate or a VOM error. The RF to DC efficiency of a circuit can be calculated by using the following equation.

$$\eta = \frac{P_{DC}}{P_{IN}} \times 100\% = \frac{V_{DC}^2}{R_L} \Big/ P_{in} \times 100\%$$

(6)

where R_L is the optimum load resistance of the circuit, η is the RF to DC efficiency of the circuit and P_{in} is the input power of the RF signal.

For low input power applications, the efficiency of the circuit is quite sensitive to changes of in DC voltage. If the change in voltage is 0.043, it can cause a change of RF to DC efficiency by to 2.84%. The experiment also showed the difference between theory and practice by employing the HSMS 2852 diode to design the rectifier. In theory, that diode cannot work for an input signal power higher than 8 dBm [6]. However, we found
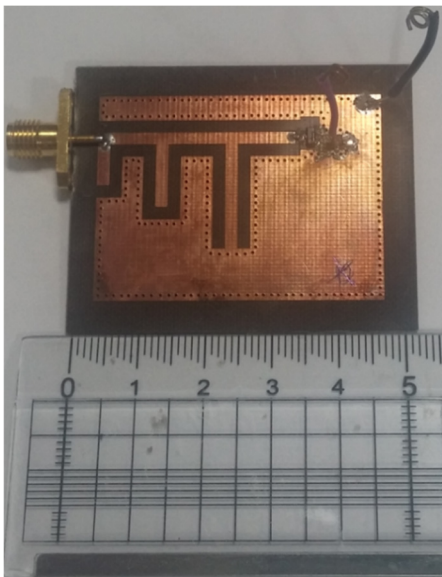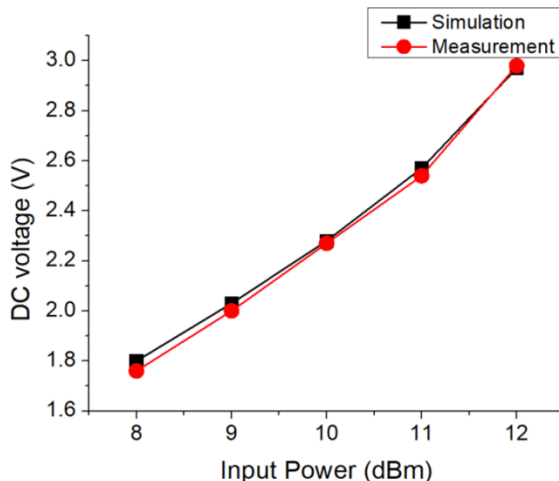
Fig. 8. Fabrication of RF–DC converter.

(a)

(b)

Fig. 9. (a) Measurement set up for the rectifier. (b) The DC voltage measurement result at the input RF power is 8 dBm.

that it can work for an input signal power up to 12 dBm, though the lifetime of the diode is short (around 1 minute).

Fig. 10. Simulation and measurement results of DC voltage of RF–DC converter.
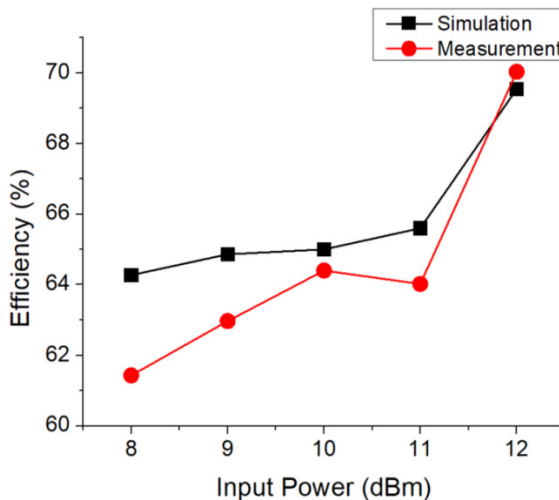
Fig. 11. RF to DC efficiency result of 2.45 GHz rectifier.

IV. CONCLUSION

The harmonic terminal combined with the matching network technique that improves DC voltage and the efficiency of RF rectifier was proposed. By finding the optimal input impedance and employing the harmonic terminal network, the RF to DC efficiency was improved up to 21%. Although there is an error between the simulation result and the measurement result, it is still acceptable (with the maximum error in RF to DC efficiency around 2.84%). In the future, we will try to integrate our design into an antenna to turn it into a rectenna that works for low power wireless applications.

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