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Effect of Subthreshold Slope on the Voltage Gain of Enhancement Mode Thin Film Transistors Fabricated Using Amorphous SiInZnO

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High-performance full swing logic inverters were fabricated using amorphous 1 wt% Si doped indium-zinc-oxide (a-SIZO) thin films with different channel layer thicknesses. In the inverter configuration, the threshold voltage was adjusted by varying the thickness of the channel layer. The depletion mode (D-mode) device used a TFT with a channel layer thickness of 60 nm as it exhibited the most negative threshold voltage (-1.67 V). Inverters using enhancement mode (E-mode) devices were fabricated using TFTs with channel layer thicknesses of 20 or 40 nm with excellent subthreshold slope (S.S). Both the inverters exhibited high voltage gain values of 30.74 and 28.56, respectively at V_{DD} = 15 V. It was confirmed that the voltage gain can be improved by increasing the S.S value.

Keywords : Amorphous oxide semiconductor, Logic inverter, SiInZnO, Thin film transistor

1. INTRODUCTION

Thin film transistors (TFTs) have attracted increasing attention for next-generation integrated circuits owing to the need for high-density integration. Next-generation integrated circuits require transparent and flexible TFTs with simple fabrication processes, which are limitations faced by existing traditional Si-based transistors. Amorphous oxide semiconductors have been used as channel layers of TFTs as they exhibit various advantages, such as transparency in the visible light range because of their wide bandgap (> 3.2 eV) and good electrical characteristics at low processing temperatures [1-4]. In this regard, Choi et al. reported that amorphous silicon-indium-zinc-oxide (a-SIZO) thin films can be processed at temperatures below 150°C [5]. It has also been confirmed that these thin films can be deposited on flexible substrates. The inverters used in systems-on-panel are based on complementary metal oxide semiconductor (CMOS) circuits. However, the existing Si-based CMOS cannot be applied to the next-generation integrated circuits. The use of p-type, organic TFTs or single walled carbon nanotube TFTs is also limited because of the complicated fabrication processes involved [6,7]. In addition, it is difficult to achieve p-type characteristics in oxide semiconductors. This is because, the valence band maximum of the oxide semiconductor is composed of O 2p orbitals [8]. In order to overcome these problems, inverters fabricated using only n-type TFTs have been studied in recent years. The n-type inverter can be fabricated easily and variously by adjusting the threshold voltage (V_{th}), for example, by changing the channel layer material, channel layer thickness, and passivation layer [9-11]. However, studies aimed at improving the voltage gain of n-type inverters are still insufficient.

In this study, high-quality transistors were fabricated using a-SIZO thin films. Using the same channel material, TFTs with different channel layer thicknesses were fabricated. Subsequently, an inverter with high voltage gain was fabricated by adjusting only the thickness of the channel layer. In addition, we analyzed the influences of enhancement mode (E-mode) TFT mobility and subthreshold slope (S.S) value on the voltage gain.

2. EXPERIMENTS

The a-SIZO TFTs were fabricated on heavily doped p-type silicon

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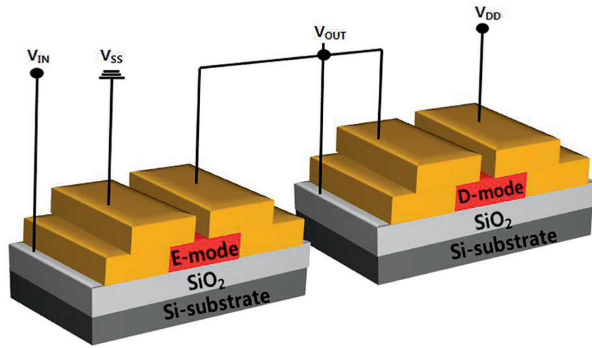

Fig. 1. Schematic of the n-type inverter circuit.

wafers (resistivity 0.001~0.002 ohm/cm), which comprises a 200 nm-thick SiO_2 layer following a typical ultrasonic cleaning process. A powder mixture of 99.99% pure SiO_2, In_2O_3, and ZnO was used as a SIZO (SiO_2: In_2O_3: ZnO = 1:3:1 wt%) target. The process parameters used for magnetron sputtering were: working power of 30 W, working pressure of 2 mTorr, and pure Ar atmosphere of 30 sccm at room temperature. The channel layers were prepared at thicknesses of approximately 20, 40, and 60 nm. For the TFTs, the width/length was fixed as 250 μm/50 μm. After the deposition, the film was annealed for 2 h at 150℃. Subsequently, different electrodes were deposited, followed by conventional photolithography and lift-off processes. Ti (10 nm) and Al (40 nm) layers as source/ drain electrodes were deposited by e-beam and thermal evaporation, respectively. Finally, the inverter was connected with depletion-mode load as shown in Fig. 1. The electrical characteristics and the inverter characteristics were measured using a semiconductor parameter analyzer (EL 423, ELECS Co.).

3. RESULTS AND DISCUSSION

Figure 2 shows the X-ray diffraction (XRD) spectra of the Si substrate and the a-SIZO thin film on the Si substrate. The XRD spectrum of the a-SIZO thin film was similar to that of the Si substrate and no other additional peaks were observed. This confirms that the a-SIZO thin film was amorphous. The TFTs were fabricated using the a-SIZO thin films prepared at different channel layer thicknesses. The transfer characteristics of the a-SIZO thin films are shown in Fig. 3, and the electrical characteristics are summarized in Table 1. The field

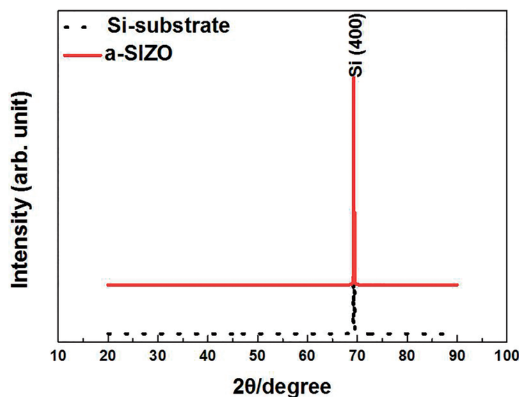

Fig. 2. XRD spectra of the Si wafer and the a-SIZO thin film deposited on the Si wafer.

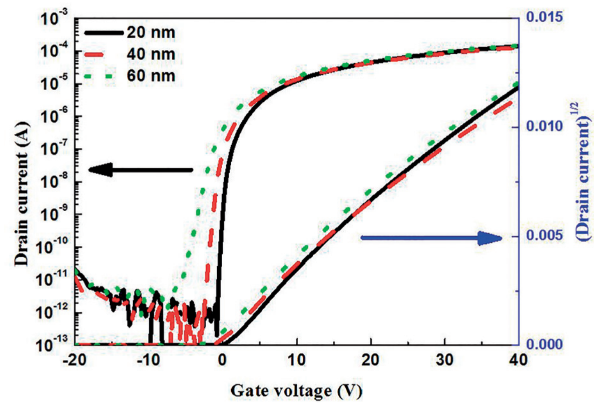

Fig. 3. Transfer characteristics of the a-SIZO thin films prepared with different channel layer thicknesses.

Table 1. TFT characteristics of the a-SIZO thin films prepared with different channel layer thicknesses.

Channel thickness	20 nm (E-mode 1)	40 nm (E-mode 2)	60 nm (D-mode)
V_{th}	0.73	-0.47	-1.67
On/Off current ratio	7.03 x 10^8	3.69 x 10^8	1.50 x 10^8
Mobility	12.41	13.10	13.99
S.S	0.23	0.36	0.94

effect mobility (μ_{FE}) can be calculated using equation (1) [12].

$$\mu FE = \frac{Lg_m}{WC_{OX}V_{DS}}, \quad (1)$$

where V_{DS} is the drain voltage, g_m is the transconductance, C_{ox} is the capacitance of the gate insulator, and W and L are the channel width and length, respectively. As the channel layer thickness was increased, the μ_{FE} increased from 12.41 to 13.99 cm^2/Vs. It has been reported that the carrier concentration increases and the electrical characteristics improve with increase in the channel layer thickness [10]. Furthermore, it can be seen that the V_{th} shifts in the negative direction from 0.73 to -1.67 V with increase in the channel layer thickness. However, the value of S.S decreased. This may be attributed to an increase in the amount of oxygen vacancies in the channel, which act as electron traps, with an increase in the channel layer thickness. Therefore, it is possible to control the electrical characteristics of the TFTs such as V_{th} by varying the channel layer thickness. We fabricated two types of inverters to investigate the effect of the S.S value on the voltage gain of the inverter. Both the inverters used the TFTs with the channel layer thickness of 60 nm (which exhibited the most negative V_{th}) as depletion mode (D-mode) devices. The inverter fabricated using the 20 nm-TFT in E-mode is referred to as Inverter 1, and that using 40 nm-TFT in E-mode is referred to as Inverter 2. Figure 4 shows the voltage transfer characteristics and the calculated values of the voltage gain of the inverters at different values of V_{DD}. The values of the voltage gain are summarized in Table 2. Both the inverters exhibited high voltage gain values of 30.74 and 28.56 at V_{DD} = 15 V. However, it can be seen that the voltage gain of Inverter 1 is higher than that of Inverter 2. Even though the electrical characteristics such as μ_{FE} of the E-mode of Inverter 2 were better than those of Inverter 1, the voltage gain showed the opposite trend. From these results, it can be confirmed that the voltage gain of the inverter is strongly dependent on the S.S value of the E-mode TFT. Similar results have been reported in the literature. For example, Han et al. reported that

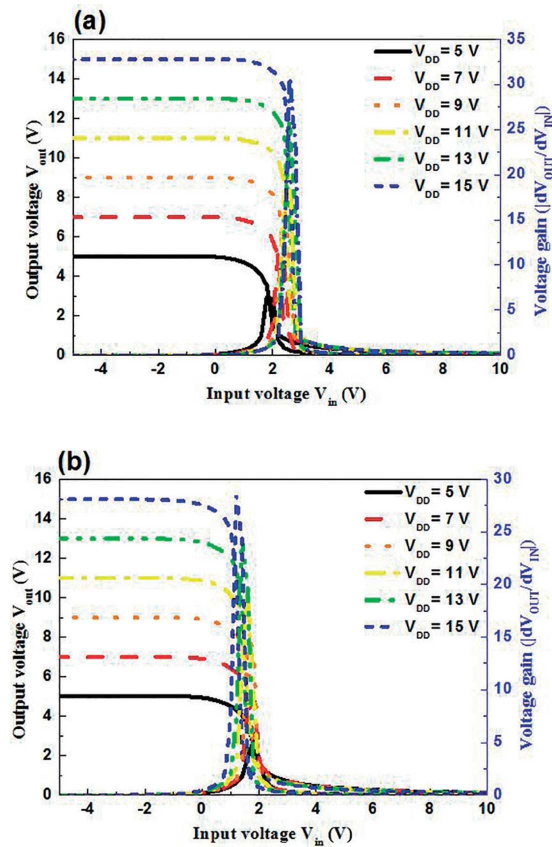

Fig. 4. Voltage transfer characteristics and calculated voltage gain values of (a) inverter 1 and (b) inverter 2 at different values of V_{DD}.

Table 2. Maximum values of the voltage gain at different values of V_{DD}.

V_{DD}	5 V	7 V	9 V	11 V	13 V	15 V
Inverter 1 voltage gain	6.42	11.6	16.47	19.95	25.96	30.74
Inverter 2 voltage gain	5.06	9.91	14.75	19.66	24.44	28.56

the voltage gain of an inverter strongly depends on the S.S value of the E-mode [13]. The electrical characteristics of the 20 nm-TFT were worse than those of the 40 nm-TFT; however, the former exhibited a higher S.S value than the latter. Therefore, a high value of voltage gain could be obtained when the inverter was fabricated using the 20 nm-TFT.

4. CONCLUSIONS

In summary, we fabricated different inverters by varying the channel layer thickness of a-SIZO TFT and investigated the effect of S.S values on the voltage gain. The inverters fabricated using channel layer thicknesses of 20 and 40 nm exhibited high voltage gain values of 30.74 and 28.56, respectively at V_{DD} = 15 V. Although the mobility of the 40 nm-TFT was higher than that of the 20 nm-TFT, the voltage gain of the inverter fabricated using 20 nm-TFT was higher than that of the inverter fabricated using 40 nm-TFT. This is attributed to the higher S.S value of the former than the latter. It is interesting to note that the voltage gain strongly depended on the S.S value when compared to the other electrical characteristics. Therefore, the value of S.S should be considered during the fabrication of an n-type inverter.

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