TRANSACTIONS ON ELECTRICAL AND ELECTRONIC MATERIALS
Vol. 18, No. 4, pp. 185-189, August 25, 2017

Regular Paper

pISSN: 1229-7607 eISSN: 2092-7592
DOI: https://doi.org/10.4313/TEEM.2017.18.4.185
OAK Central: http://central.oak.go.kr

CMOS Integrated Multiple-Stage Frequency Divider with Ring Oscillator for Low Power PLL

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Received March 31, 2017; Revised June 2, 2017; Accepted June 5, 2017

This paper proposes a low power frequency divider for an integrated CMOS phase-locked loop (PLL). An injection-locked frequency divider (ILFD) was designed, along with a current-mode logic (CML) frequency divider in order to obtain a broad-band and high-frequency operation. A ring oscillator was designed to operate at 1.2 GHz, and the ILFD was used to divide the frequency of its input signal by two. The structure of the ILFD is similar to that of the ring oscillator in order to ensure the frequency alignment between the oscillator and the ILFD. The CML frequency divider was used as the second stage of the divider. The proposed frequency divider was applied in a conventional PLL design, using a 0.18 μm CMOS process. Simulation shows that the proposed divide-by-two ILFD and the divide-by-eight CML frequency dividers operated as expected for an input frequency of 1.2 GHz, with a power consumption of 30 mW.

Keywords : Frequency divider, ILFD, CML, Ring oscillator, CMOS

1. INTRODUCTION

PLL is used in various communication systems such as clock generation circuit and frequency synthesizers. The frequency divider [1-4] is one of the most important components in PLL system. Conventional analog PLL [5,6] typically consists of phase detector, charge-pump, filter, VCO, and frequency divider. The VCO and the frequency divider are important to determine the operating frequency range and power consumption of the PLL.

Recently, several frequency dividers such as injection-locked (IL), current-mode logic (CML), and super-dynamic divider were introduced for their advantages such as their high-frequency operation. Such considerations are also critical design parameters for VCO.

In this work, ring oscillator is used as a VCO. Compared to ring oscillator, LC cross-coupled oscillator performs better in terms of high-frequency operation and power consumption. However, the fabrication of an integrated inductor inside LC cross-coupled oscillator results in unpredictable parasitic capacitance and resistance between its metal lines.

CML frequency divider is widely used in a conventional PLL, but its power consumption increases significantly with the operating frequency. ILFD [7-9] has been reported to operate in high frequencies with low power consumption. However, it has a narrow locking range and suffers from a high-power consumption as the division ratio increases.

In this work, injection-locked and CML dividers are applied as the first and second stages of a divider chain, respectively, to obtain a low power consumption in the high-frequency range. The structure of ILFD is made similar to that of the VCO for a better frequency alignment. A ring oscillator is used as VCO for its high operating frequency. CML divider, which is applied for the second stage of the divider, consists of a differential pair and a latch circuit, which are the main component of a master-slave (M-S) flip-flop. Compared to other flip-flops, the M-S flip-flop has the advantage of having a high operating speed without causing logic errors because it utilizes both the positive and negative triggered latches.

We designed the frequency divider with a divide-by-two ILFD and a divide-by-eight CML divider using a 0.18-μm CMOS process. The divider was applied in a conventional analog PLL and measurements were made through CADENCE simulation.

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2. CIRCUIT DESIGN OF DIVIDER

Figure 1 shows the block diagram of the proposed PLL which has a 1.2 GHz VCO, a 0.6 GHz divide-by-two ILFD, and a three-stage CML frequency divider. The input of the ILFD is the fundamental signal f_{out} which is the output frequency of the VCO. The ILFD has a similar circuit structure to that of the VCO, which consists of a ring oscillator in order to ensure frequency alignment. In this work, the ILFD is designed to divide frequency by two, while CML frequency divider is used to divide frequency by eight by employing three stages of flip-flops.

PLL also consists of phase frequency detector (PFD) and charge pump (CP). The output of the CML divider is connected to the second frequency input port of the PFD. The frequency is 75 MHz and is the result of the LFD (1/2) and CML (1/8) frequency dividers dividing the VCO output frequency of 1.2 GHz.

VCO and ILFD are shown in Figs. 2(a) and (b), respectively. VCO has the structure of ring oscillator [10] whose simplicity makes it a popular choice in many integrated circuits such as microprocessors and memories. Three common source (CS) stages in the oscillator provide an oscillating frequency which depends on the load capacitors and resistors. In Fig. 2(a), the load resistors have been replaced with PMOS current sources which are controlled by the DC bias voltage, V_{bias}. The variation of Vbias can switch the PMOS transistors into the saturation or triode modes and provides different resistances and, thus, oscillating frequencies in the oscillator. The structure of ILFD is designed to be similar to that of VCO. If LC oscillator (which employs an inductor and a capacitor) is used in the VCO or the ILFD, a high oscillating frequency can be obtained with low power consumption. However, the fabrication of an inductor in an integrated circuit is more difficult to design and takes up a larger die-area than a ring oscillator. The input signals in ILFD are injected into the gates of NMOS transistors. In the locking state, the zero crossings of V_{out} and its inverse coincide with the peaks of the input signals. The differential operation provides a division ratio of 2. The turning frequency is determined by the equivalent load capacitor and resistor. The oscillating frequency of the VCO can be similarly obtained by the equivalent capacitance and resistance which result from the MOS oxide and the channel current. When the ILFD is locked with a proper signal injection, half of the input frequency can be obtained as an output. The locking state comes when the peaks of the input signals match to the zero crossings of V_{out} and its inverse.

Another high-frequency ILFD with the structure of LC oscillator, which includes an inductor and a capacitor, is proposed. The application of the injection signal and the locking mechanism are similar to those of the proposed ILFD which has a three-CS-stage ring oscillator. While ILFD based on LC oscillator can provide a high oscillating frequency by using an inductive energy component, the fabrication of inductor in an integrated circuit costs more and requires a difficult process. Furthermore, integrated small-size inductor usually causes unpredictable parasitic capacitance and resistance.

CML frequency divider [4] as shown in Fig. 3 is composed with two CML master-slave flip-flop. The master-slave flip-flop operates as the read and latch circuits. The read circuit is the n-MOS differential pair and the latch circuit is the cross-coupled MOSFETs in the block. The CML divider is designed to provide a 1/8 frequency division with a 3-stage chain. In order to increase the frequency bandwidth, an inductive peaking structure can be applied in CML frequency divider. The load resistors in frequency divider are replaced by DC bias in MOS gate, which can improve a current driving capability of current source.

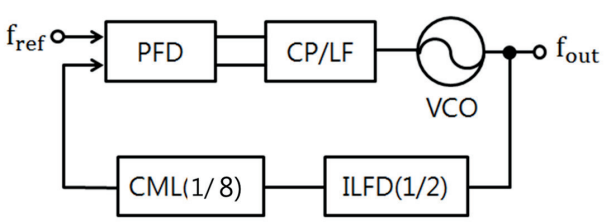

Fig. 1. Block diagram of PLL with ILFD and CML frequency divider.

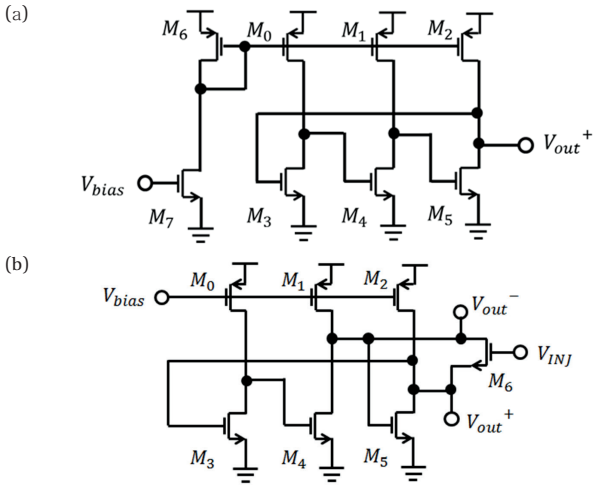

Fig. 2. Schematic of (a) VCO and (b) ILFD.

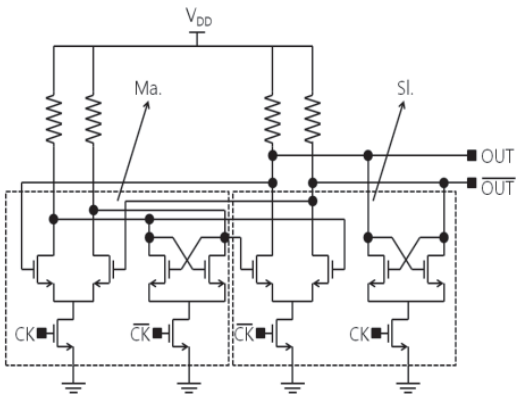

Fig. 3. Schematic of CML frequency divider.

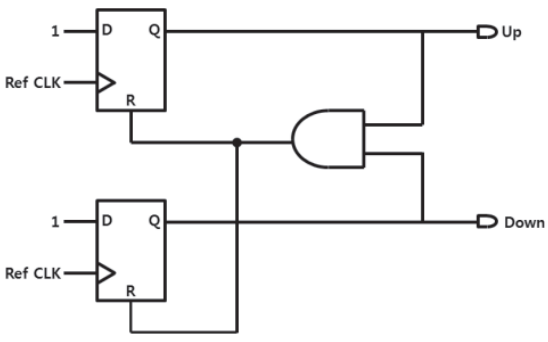

Fig. 4. Block diagram of the phase frequency detector (PFD).

Figure 4 is the block diagram of the phase frequency detector (PFD), where D flip-flops and AND logic gate are included. The output of frequency divider goes to FB CLK in PFD. When the two inputs of PFD are both in the high logic state, D flip-flops are initialized.

3. RESULTS

Figure 5 is the chip layout of the VCO, ILFD, and CML blocks, which are designed in 0.18 μm CMOS process. The area of the circuit is 0.1 mm^2.

The output waveforms of ring oscillator and ILFD are shown in Fig. 6. The simulation is carried out using CADENCE Spectre. Figure 6(a) shows the input and output waveforms of the ILFD. The 0.6 GHz output is obtained with an input frequency of 1.2 GHz. The CML frequency divider can operate in a wide bandwidth. However, its power consumption significantly increases with operating frequency. In contrast, the ILFD is useful when operating at high frequencies because of its relatively low power consumption, though it has a narrow locking range. Figure 6(b), which is obtained from the ring oscillator and the ILFD with a LC cross-coupled topology, shows locking time of approximate 400 ns and an output frequency of 1.2 GHz. In order to reduce power consumption, the locking time of PLL should be reduced. To obtain a fast-locking PLL, the loop bandwidth of PLL should be made as wide as possible. This, however, can increase phase noise and jitter. Several works [11-13] has proposed hybrid synthesizer, lock-aid circuit, and phase detection circuits to reduce the locking time.

Figure 7 shows a block diagram of the four stages of the divider and the corresponding output waveforms. The block diagram of the divider presented in Fig. 7(a) has a single-stage ILFD and a three stage CML divider. Figure 7(b) is the output waveforms for each of the 4-stages of the divider for an input frequency of 1.2 GHz. The simulation result is obtained from a post-layout simulation using a 0.18 μm CMOS process. The outputs of each divider show that the frequency of each input signal is divided by two. The final output Ⓔ shown in Fig. 7(b) has a period of approximate 13.3 ns, which corresponds to a frequency of 75 MHz. The power consumption of the ILFD is about 3.6 mW. Total power consumption of the frequency dividers is 30 mW.

In the final stage of the divider shown in Fig. 7(a), an output buffer is used to ensure that there is sufficient output voltage swing. This buffer can also provide a more stable output, though it results in higher power consumption and uses more die-area. Figures 8(a) and (b) shows the buffer circuit and the output waveforms of the final-stage of the CML divider with and without the buffer. The

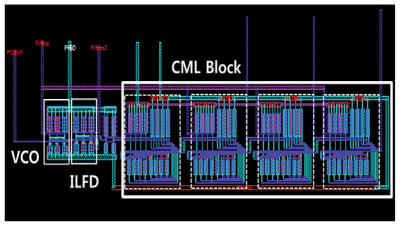

Fig. 5. Layout of VCO, ILFD, and CML dividers.

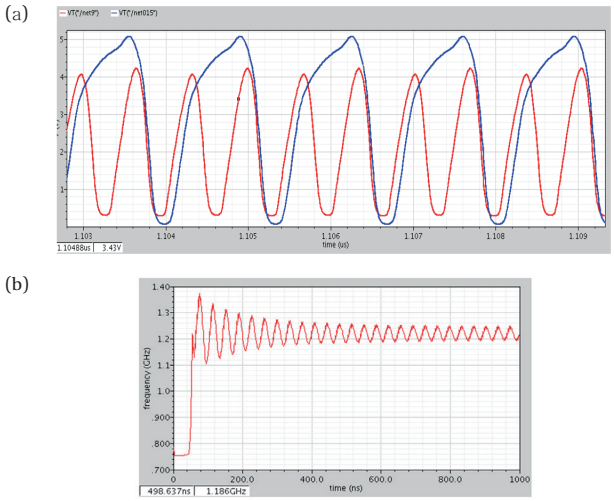

Fig. 6. (a) 0.6 GHz output waveform of ILFD with 1.2 GHz input frequency and (b) output waveform of VCO after locking.

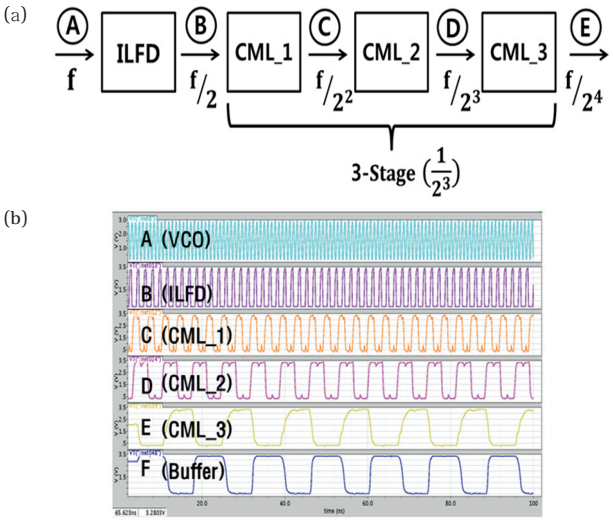

Fig. 7. (a) Block diagram of ILFD and CML frequency divider and (b) output signal of each stage of the dividers (A ~ F).

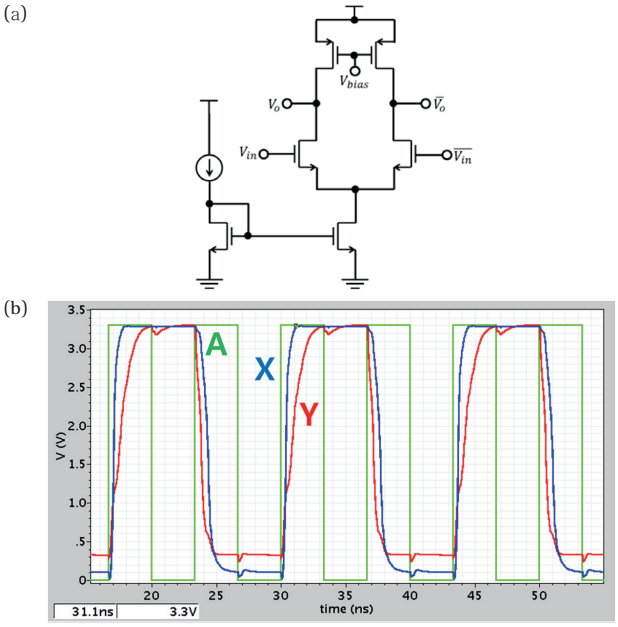

Fig. 8. (a) Circuit of buffer in the proposed divider and (b) output waveforms (X) with and (Y) without buffer.

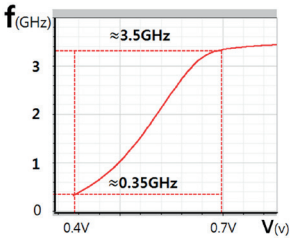

Fig. 9. Output frequency (f_{out}) of VCO versus control voltage.

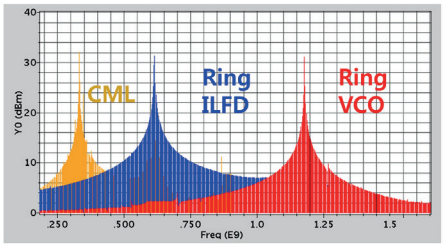

Fig. 10. Output frequency spectra of VCO and ILFD.

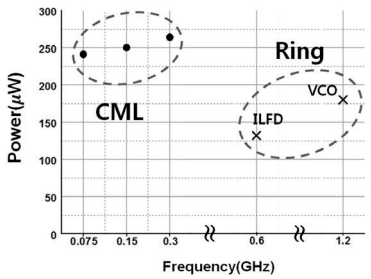

Fig. 11. Power consumption versus frequency in the divider chain with two different kinds of dividers.

buffer consists of a differential pair and a current mirror. Figure 8(b) indicates that the buffer provides a more stable waveform with a large swing. This result is obtained for an input signal of 20 GHz with the proposed divide-by-two CML divider.

VCO is an important element in PLL for its high-frequency operation. The main concern in VCO design is their high-frequency capability and achieving a wide locking range with low power consumption. The VCO used in this work has the topology of a ring oscillator. Figure 9 is a graph which shows the characteristic of the VCO output frequency versus the control voltage, Vc. The range region of linearity of f_{out} goes from 0.4 GHz to 3 GHz, and the desired output frequency of 1.2 GHz is obtained for a bias voltage of 0.5 V.

If VCO and ILFD are replaced by a circuit based on an LC cross-coupled oscillator, the operating frequency can be in the ranges of tens of GHz, but, power consumption may be significantly increased. Moreover, the accurate fabrication of an inductor of a specific value is difficult for an integrated circuit.

As shown in Fig. 2(a) (which is the schematic of the proposed VCO), the DC bias voltage in MOSFET M7 provides a variable conductance, which can be obtained from the device parameters, that can be used to adjust the operating frequency. Figure 9 shows the narrow region of linearity, which is about 0.2 V in the bias voltage. To increase the region of linearity of f_{out}, a capacitor array or a varactor can be placed between the stages of the inverter circuit.

The output frequency spectra of VCO and ILFD are shown in Fig. 10. Two high power peaks are obtained from the post-layout simulation. The simulation results of the VCO and the ILFD show high sensitivity peaks at the frequencies of 1.48 and 0.74 GHz. The result indicates that the divide-by-two operation performed by the ILFD is done accurately and that the VCO produces a high frequency of 1.49 GHz.

Figure 11 shows power consumption with variation of the 77operating frequency. At a frequency of 1.2 GHz, the VCO operates with a power consumption of 180 μW. The ILFD has a circuit structure similar to that of the VCO, which is a ring oscillator with a three-stage CMOS inverter, in order to ensure frequency alignment. In this work, the ILFD is designed to be a divide-by-two frequency divider. A single ILFD and three CML dividers dissipate a power of 130 and 760 μW, respectively, and the total power consumption is 890 μW. The CML frequency divider, which has more circuit elements in the master-slave flip-flop, has higher power consumption. The power consumption of the ILFD is supposed to increase linearly with the operating frequency because of the switching power consumption. The on-off switching operations in MOS transistors in the ILFD circuit are the major sources of power consumption. The locking range and bandwidth of the ILFD depend on parameters such as the injection current and the Q-factor of the ring oscillator. In the ILFD, there is a trade-off between power consumption and high-frequency locking. Advantage of the circuit proposed in this work is the significant reduction in power consumption, compared to that of an LC cross-coupled oscillator and an ILFD, which usually consumes power in the range of tens of mW. Moreover, die area can be reduced and the fabrication process can be significantly simplified because of the simple structure of the proposed circuit.

4. CONCLUSIONS

This paper proposes a high performance frequency divider for CMOS integrated PLL. VCO and ILFD with topology of ring oscillator are analyzed to obtain a low power frequency divider. A 1.2 GHz VCO is obtained by using a three-stage inverter circuit and a DC bias control. The proposed ILFD has a similar structure to that of ring oscillator, which is used as a VCO, while the CML divider as the 2nd stage divider applies a master-slave flip-flop, which is composed of a differential pair and a latch circuit. The ILFD and a three-stages CML divider are used to divide an input frequency of 1.2 GHz by two and eight, respectively. Our simulation analysis using a 0.18-μm CMOS process shows that the proposed divider operates accurately and is able to provide a signal with a 75 MHz frequency, which is required for the input of the PDF in PLL. At the supply voltage of 1.2 V, the power consumptions of ILFD and entire divider are approximately 3.6 mW and 30 mW, respectively.

ACKNOWLEDGEMENT

This work was supported by the intramural research grant of Chungbuk National University in 2015.

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