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New Configuration of a PLDRO with an Interconnected Dual PLL Structure for K-Band Application

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Abstract

A phase-locked dielectric resonator oscillator (PLDRO) is an essential component of millimeter-wave communication, in which phase noise is critical for satisfactory performance. The general structure of a PLDRO typically includes a dual loop of digital phase-locked loop (PLL) and analog PLL. A dual-loop PLDRO structure is generally used. The digital PLL generates an internal voltage controlled crystal oscillator (VCXO) frequency locked to an external reference frequency, and the analog PLL loop generates a DRO frequency locked to an internal VCXO frequency. A dual loop is used to ease the phase-locked frequency by using an internal VCXO. However, some of the output frequencies in each PLL structure worsen the phase noise because of the *N* divider ratio increase in the digital phase-locked loop integrated circuit. This study examines the design aspects of an interconnected PLL structure. In the proposed structure, the voltage tuning; which uses a varactor diode for the phase tracking of VCXO to match with the external reference) port of the VCXO in the digital PLL is controlled by one output port of the frequency divider in the analog PLL. We compare the proposed scheme with a typical PLDRO in terms of phase noise to show that the proposed structure has no performance degradation.

Key Words: Analog PLL, Digital PLL, Dual-Loop, Front-End, Phase-Locked PLL, PLDRO.

I. Introduction

In microwave communication systems that require high-capacity data transmission such as satellites' base station systems and electronic warfare (EW), the local oscillators at the transmitter/receiver terminals should maintain the characteristics of low phase noises and excellent spectral purity [1].

As the frequency resources of C, S, and Ku bands for such microwave communication systems have already been saturated, frequency resources should be developed in the K and Ka bands, which are quasi-millimeter wave bands (18–40 GHz) [2].

Digital modulation systems are used to transmit high-capacity data at high speeds using the K band. In particular, in the case of phase modulation systems, the oscillator characteristics of high-stability and low-phase noises are required because the frequency stability and phase noise characteristics have major effects on the beat error ratio characteristics [3]. In the fields of radars and electronic warfare, precise frequencies up to several MHz or several hundred kHz (e.g., 9.625xx GHz) are required for oscillators instead of integer multiples of the external reference frequency.

Satellite communication base stations and EW systems require the characteristics of the in-band phase noises of the local oscillators of microwave communication systems, which use the Ka-band or millimeter bands not to exceed –70 dBc/Hz at the offset frequency of 1 kHz and –90 dBc/Hz at the offset fre-

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quency of 100 kHz according to the center frequency specified by IESS-308. Therefore, phase-locked dielectric resonator oscillators (PLDROs) are widely used to satisfy the required standards [4].

In the case of existing PLDROs, the internal voltage controlled crystal oscillator (VCXO) frequency is phase-locked at the external reference frequency in the primary digital phase-locked loop (PLL) circuit, and the phase-locked VCXO frequency and the DRO output frequency are phase-locked and used in sequence in the secondary analog PLL circuit. In this case, if the internal VCXO frequency is not an integer multiple (e.g., 96 MHz) of the external reference frequency (10 MHz) but a complicated frequency (e.g., 96.25 MHz), the comparison frequency will become smaller when the phase is compared in the phase detector (PFD) of the integer phase-locked loop integrated circuit (PLLIC). Accordingly, the divider ratio of the PLLIC increases, thus resulting in bad phase noise characteristics.

To output precise frequencies, two loops (digital PLL and analog PLL) are used together for each change in frequency. In this case, the divider ratio of the PLLIC of the digital PLL circuit for primary phase comparison with the external reference frequency (10 MHz) increases and leads to bad phase noise characteristics in the in-band loop bandwidth of the analog PLL circuit (final output frequency) [5–7].

The proposed PLDRO is in a new structure in which no phase noise deterioration occurs in the analog loop filter band, and the output frequency can be freely adjusted. Recently, precision to several hundred kHz (e.g., 9.625xx GHz) has been required as the center frequency of local oscillators in accordance with the requirements of communication systems.

A design equation for the proposed PLL structure was derived and presented in this study.

The output frequency of the DRO was coupled and made to pass through the frequency divider and the phase was directly compared with that of the external reference frequency (10 MHz) in the PLLIC. Then, the error voltage that corresponds to the phase difference was made to pass through the loop filter to control the voltage tuning (VT) terminal of the VCXO. To verify theprposed PLDRO, a new PLL with 9.625 GHz band was designed. The final output frequency was multiplied by two to become 19.25 GHz, and the result was experimentally verified. Fig. 1 shows the block diagram of the proposed PLDRO structure.

II. Circuit Topology

The concept of the proposed PLDRO is configured as an interconnected dual-loop PLL structure, in which a digital PLL and an analog PLL are interconnected. The proposed PLDRO is designed so that the phase error voltage resulting from the

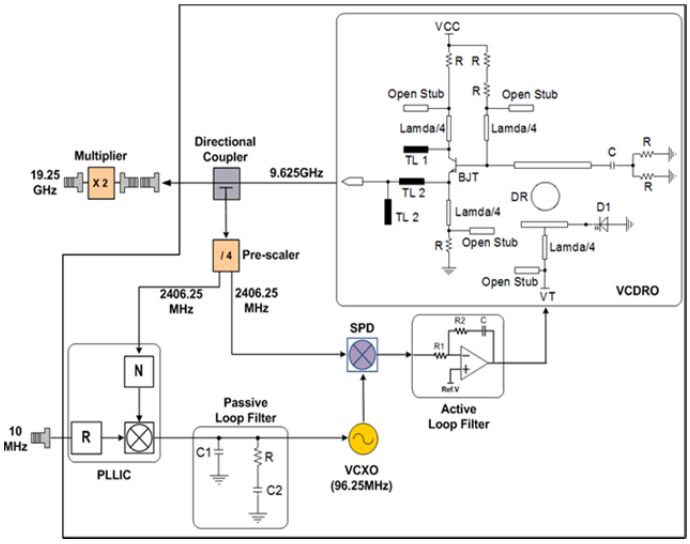

Fig. 1. Block diagram of the proposed total PLDRO.

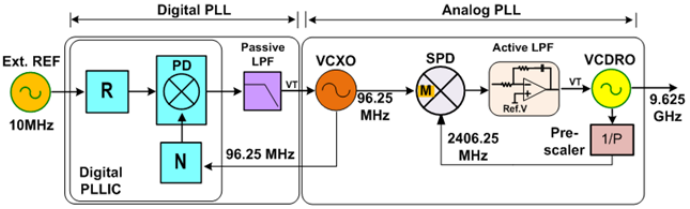

Fig. 2. Block diagram of the general PLDRO.

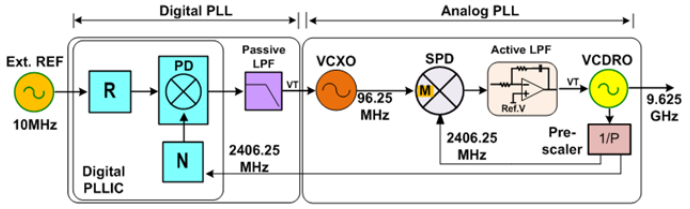

Fig. 3. Block diagram of the proposed PLDRO.

phase comparison between the reference frequency input and the output frequency of the VCDRO controls the VT terminal of the VCXO, which is not a subject of the direct comparison.

Fig. 2 shows the block diagram of the general PLDRO for the independent PLL loop flow. The increase in the *N* divider ratio is related to the complex frequency of the VCXO (96.25 MHz), as the phase should be compared with the external reference in the digital PLL configuration. Fig. 3 presents the block diagram of the proposed PLDRO for the PLL loop flow.

The phase of the output frequency of the VCDRO divided by four and that of the external reference frequency (10 MHz) are directly compared with the PFD to output the error voltage, which corresponds to the phase difference between the two signals. The error voltage controls the VT terminal of the VCXO, which is not a subject of direct phase comparison, through the secondary manual loop filter, which has the characteristics of low-pass filters. Thereafter, the controlled VCXO controls the

VCDRO, and the error voltage is obtained through the phase comparison with the harmonics multiplied 25 times in the sampling phase detector (SPD) through the analog loop filter.

Then, the output frequency of the VCDRO that corresponds to the phase error voltage is inputted into the phase detector of the PLLIC, and the above process is repeated until the VCXO comes under the in-phase condition. This way, as the phase is compared with the output frequency of the VCDRO instead of the integer multiple of the external reference frequency (10 MHz), only the VCXO, which is a subject of the PLL circuit, is followed, and the deterioration of phase noises resulting from the increase in the divider ratio does not occur within the analog PLL bandwidth. That is, by changing only the frequency of the VCXO, the output frequency of the PLDRO can be freely implemented to the precise frequencies of several hundred kHz.

As shown in Fig. 3, the output frequency is as follows:

$$f_{OUTPUT} = (PXM) f_{VCXO}, \tag{1}$$

where P is the divider ratio(4) of the pre-scaler, f_{VCXO} is the output frequency (96.25 MHz) of the internal VCXO, and M is the number of multiplication (25) of the SPD. The secondary passive loop filter of the digital PLL of the proposed PLDRO shown in Fig. 1 is presented in Fig. 4. The impedance transfer function is as follows:

$$Z(s) = \frac{1 + s\tau_2}{sc_t(1 + s\tau_1)}, \quad \tau_1 = \frac{RC_1C_2}{c_t}, \quad \tau_2 = RC_2 \tag{2}$$

$$C_t = \frac{K_\varphi K_{VCO}}{N\omega_C^2} \cdot \sqrt{\frac{(1 + \omega_C^2 \tau_2^2)}{(1 + \omega_C^2 \tau_1^2)}} \tag{3}$$

where K_ϕ is the phase detector gain (V/rad), K_{VCO} is the VCXO gain (Hz/V), ω_C is the loop bandwidth, and N is the divider ratio, which is a value obtained by dividing the VCXO frequency by the comparison frequency (PFD).

The secondary active loop filter of the analog PLL of the proposed PLDRO shown in Fig. 1 is presented in Fig. 5. The transfer function is as follows:

$$F(s) = \frac{\tau_2 s + 1}{\tau_1 s}, \quad \tau_1 = R_1 C, \quad \tau_2 = R_2 C \tag{4}$$

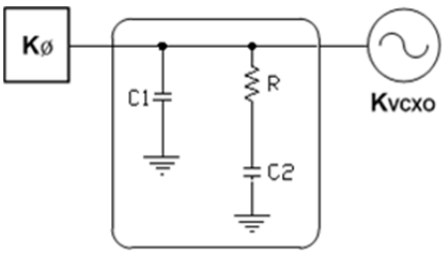

Fig. 4. Secondary passive loop filter of the digital PLL.

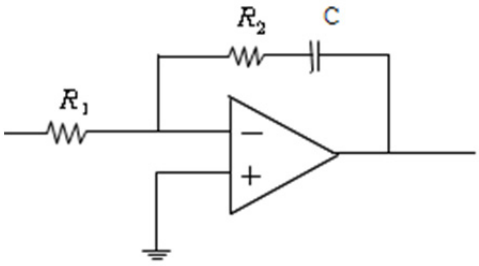

Fig. 5. Secondary active loop filter of the analog PLL.

III. Design and Simulation

The components that contribute to the noises inserted into the interconnected dual-loop PLLs of the proposed PLDRO structure are shown in Fig. 6. The noise term variables are as follows:

ϕ_{nR} : Reference VCXO phase noise

ϕ_{nM} : Reference divider or SRD phase noise

ϕ_{nO} : Total output phase noise

ϕ_{nN} : Pre-scaler divider phase noise

ϕ_{nDRO} : DRO phase noise

V_{nPD} : Phase detector phase noise

V_{nLPF} : Loop amplifier phase noise

The phase noise in the PLDRO final output is derived by Eq. (5):

$$\varphi_{nO} = \left\{\left[\left[\left(\frac{\varphi_{nR}}{M} + \varphi_{nM}\right) - \left(\frac{\varphi_{nO}}{N} + \varphi_{nN}\right)\right] \cdot K_{PD} + V_{nPD} + V_{nLPF}\right\} H(s)\} \cdot \frac{K_{DRO}}{s} \cdot \varphi_{nDRO}, \tag{5}$$

where

K_{DRO} is the VC-DRO modulation sensitivity(radians /second per volt)

K_{PD} is the PD or SPD output sensitivity (volts per radian)

$H(s)$ is the loop filter transfer function

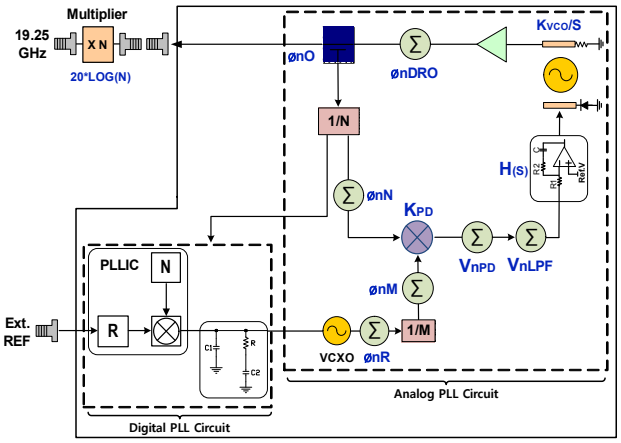

Fig. 6. Phase noise generator in the proposed PLDRO structure.

N is the DRO divider ratio
M is the reference divider ratio

Eq. (5) shows that the loop filter transfer function $H(s)$ is connected to individual noise sources in the analog PLL loop band except for the free-running phase noise of the DRO. In particular, the phase noise characteristics of the VCXO corresponding to the internal reference frequency in the analog PLL circuit directly affect the phase noises in the loop filter band. That is, if the phase noise characteristics of the VCXO are poor, the final output phase noise will be poor in the PLL loop band [8].

How the digital PLL circuit affects the phase noise of the VCXO, which is not a subject of direct phase comparison, is examined in Section III-1, and the phase noise of the final output (analog PLL circuit) is analyzed in Section III-2.

1. Analysis of the Phase Noise of the Digital PLL Circuit

The overall phase noise of the digital PLL is as follows (Table 1):

$$TotalPN = 10 * LOG(10^{\frac{VCXOsPN}{10}} + 10^{\frac{REFsPN}{10}} + 10^{\frac{PSsPN}{10}} + 10^{\frac{PDsPN}{10}}). \quad (6)$$

Eq. (6) obtains the final output phase noise of the digital PLL circuit. The characteristics of the individual components are as follows:

The phase noise of the VCXO output under No. 1 is the value after passing the high pass attenuation of the passive loop filter. The phase noise of the reference output under No. 2 is the value after an increase by the N divider ratio. This value is one (3850) set in the PLLIC but a value (9.625) obtained by dividing the VCXO frequency by the external reference frequency followed by passing the low pass attenuation by the passive loop filter. The phase noise of the pre-scaler output under No. 3 is a value after passing the low pass attenuation by the passive loop filter. The phase noise of the phase detector output under No. 4 can be calculated by Eq. (7), followed by passing through the low pass attenuation by the passive loop filter.

$$\text{Close-in phase noise} = PLLIC's\ noise\ floor - 10 * LOG(PFD) - 20 * LOG(N), \quad (7)$$

where PFD is the phase frequency detector, and N is the divider and pre-scaler ratio of the digital PLLIC.

The results of the calculation of the above equation using Excel are as shown in Table 1.

As the VCXO in the digital PLL circuit is not included in the closed loop PLL route regardless of the increase in the number of N the divider ratio, the pure phase noise characteristics of VCXO can be maintained outside the loop filter band without affecting the phase noise. The phase noise values in the digital PLL circuit calculated as such are –138.6 dBc/Hz and –148.9 dBc/Hz at 1 kHz and 10 kHz offset frequencies for 96.25 MHz, respectively.

2. Analysis of the Phase Noise in the Final Output (Analog PLL Circuit)

The overall phase noise of the analog PLL (Table 2) is as follows:

$$TotalPN = 10 * LOG(10^{\frac{DROsPN}{10}} + 10^{\frac{REFsPN}{10}} + 10^{\frac{PSsPN}{10}} + 10^{\frac{PDsPN}{10}}). \quad (8)$$

The phase noise of the final output is calculated by Eq. (8). The characteristics of the individual components are as follows:

The phase noise of the DRO output under no.1 is the value after passing the high pass attenuation by the active loop filter. The phase noise of the reference output under No. 2 is the phase noise of the VCXO, which is the value after an increase

Table 1. Phase noise calculation for the proposed PLDRO (digital PLL)

Digital PLL (VCXO)	BW (kHz)	PFD (MHz)	F_O (GHz)	N		
96.25 MHz PLVCXO	0.1	10	0.09625	9.625		
Frequency [Hz] @ OFFSET	10	100	1,000	1.0E+04	1.0E+05	1.0E+06
VCXO phase noise	-88	-115	-140	-149	-160	-160
Reference phase noise	-108	-140	-150	-155	-155	-155
Pre-scaler phase noise	-135	-140	-145	-148	-148	-148
PD phase noise	-125.3	-125.3	-125.3	-125.3	-125.3	-125.3
High Pass Attenuation (LF)	20.0	0.0	0.0	0.0	0.0	0.0
Low Pass Attenuation (LF)	0.0	0.0	20.0	40.0	60.0	80.0
Reference multiply	-88.3	-120.3	-130.3	-135.3	-135.3	-135.3
No.1 VCXO output	-108.0	-115.0	-140.0	-149.0	-160.0	-160.0
No.2 Reference output	-88.3	-120.3	-150.3	-175.3	-195.3	-215.3
No.3 Pre-scaler output	-135.0	-140.0	-165.0	-188.0	-208.0	-228.0
No.4 Phase detector output	-125.3	-125.3	-145.3	-165.3	-185.3	-205.3
Total phase noise	-88.3	-113.6	-138.6	-148.9	-160.0	-160.0

Table 2. Phase noise calculation for the proposed PLDRO (analog PLL)

Analog PLL (DRO)	BW (kHz)	PFD (MHz)	F_O (GHz)	N		
9.625 GHz PLDRO	100	100	9.625	96.25		
Frequency [Hz] @ OFFSET	10	100	1,000	1.0E+04	1.0E+05	1.0E+06
DRO phase noise	-30.0	-50.0	-90.0	-100.0	-120.0	-130.0
Reference phase noise	-88.3	-113.6	-138.6	-148.9	-160.0	-160.0
Pre-scaler phase noise	-125	-130	-140	-150	-150	-150
PD phase noise	-125.0	-125.0	-125.0	-125.0	-125.0	-125.0
High Pass Attenuation (LF)	140.0	100.0	60.0	20.0	0.0	0.0
Low Pass Attenuation (LF)	0.0	0.0	0.0	0.0	0.0	20.0
Reference multiply	-48.6	-73.9	-98.9	-109.2	-120.3	-120.3
No.1 DRO output	-170.0	-150.0	-150.0	-120.0	-120.0	-130.0
No.2 Reference output	-48.6	-73.9	-98.9	-109.2	-120.3	-140.3
No.3 Pre-scaler output	-125.0	-130.0	-140.0	-150.0	-150.0	-170.0
No.4 Phase detector output	-125.0	-125.0	-125.0	-125.0	-125.0	-145.0
Proposed PDRO's phase nose	-48.6	-73.9	-98.9	-108.8	-116.5	-129.5
19.25G PLDRO PN (X2)	-42.6	-67.9	-92.9	-102.7	-110.5	-123.5

by the N divider ratio—a product of the number of multiplication (25) of the SRD in the SPD and the divider ratio (4) of division by four, followed by the low pass attenuation by the active loop filter. The phase noise of the pre-scaler output under No. 3 is the phase noise characteristic of the divider (1/4), which is the value after passing the low pass attenuation by the active loop filter, used separately. The phase noise of the phase detector output under No. 4 is the phase noise characteristic of the SPD, which is a value after passing the low pass attenuation by the active loop filter. The results of the calculation of the above equation using Excel are shown in Table 2.

The final phase noise values of 9.625 GHz calculated as such are –98.9 dBc/Hz and –108.8 dBc/Hz at 1 kHz and 10 kHz offset frequencies for 9.625 GHz, respectively.

If 9.625 GHz is changed into the K band (19.25 GHz) using a doubler, the phase noise values will change as follows (deteriorated by 20*log(N)): –92.9 dBc/Hz and –102.7 dBc/Hz at 1 kHz and 10 kHz offset frequencies for 9.625 GHz, respectively. Fig. 7 shows the results of the analysis of the phase noise of the K-band (19.25 GHz) after the multiplication of the proposed PLDRO by two. The values satisfy both the Intelsat Earth Station Standard and the IESS-308 standard. The actual results of the measurement are presented in Section IV. As shown by the results indicated in blue, in the case of the general PLDRO, if the digital PLL and the analog PLL are independently implemented, the IESS-308 standard will not be observed in the 1 kHz offset frequency because of the increase in the N divider of the digital PLL circuit.

As indicated by the blue line in the general PLDRO in Fig. 7, the results of the calculation using Excel are presented in Tables 3 and 4.

The results shown in Table 5 are indicated to be worse than

Table 3. Phase noise calculation for the general PLDRO (digital PLL)

Digital PLL (VCXO)	BW (kHz)	PFD (MHz)	F_O (GHz)	N		
96.25 MHz PLVCXO	0.1	0.25	0.09625	385		
Frequency [Hz] @ OFFSET	10	100	1,000	1.0E+04	1.0E+05	1.0E+06
VCXO phase noise	-88	-115	-140	-149	-160	-160
Reference phase noise	-108	-140	-150	-155	-155	-155
Pre-scaler phase noise	-135	-140	-145	-148	-148	-148
PD phase noise	-109.3	-109.3	-109.3	-109.3	-109.3	-109.3
High Pass Attenuation (LF)	20.0	0.0	0.0	0.0	0.0	0.0
Low Pass Attenuation (LF)	0.0	0.0	20.0	40.0	60.0	80.0
Reference multiply	-56.3	-88.3	-98.3	-103.3	-103.3	-103.3
No.1 VCXO output	-108.0	-115.0	-140.0	-149.0	-160.0	-160.0
No.2 Reference output	-56.3	-88.3	-118.3	-143.3	-163.3	-183.3
No.3 Pre-scaler output	-135.0	-140.0	-165.0	-188.0	-208.0	-228.0
No.4 Phase detector output	-109.3	-109.3	-129.3	-149.3	-169.3	-189.3
Total phase noise	-56.3	-88.2	-117.9	-141.5	-158.0	-160.0

Table 4. Phase noise calculation for the general PLDRO (analog PLL)

Analog PLL (DRO)	BW (kHz)	PFD (MHz)	F_O (GHz)	N	PD(PN)	
9.625 GHz PLDRO	100	100	9.625	96.25	-125	
Frequency [Hz] @ OFFSET	10	100	1,000	1.0E+04	1.0E+05	1.0E+06
DRO phase noise	-30.0	-50.0	-90.0	-100.0	-120.0	-130.0
Reference phase noise	-56.3	-88.2	-117.9	-141.5	-158.0	-160.0
Pre-scaler phase noise	-125	-130	-140	-150	-150	-150
PD phase noise	-125.0	-125.0	-125.0	-125.0	-125.0	-125.0
High Pass Attenuation (LF)	140.0	100.0	60.0	20.0	0.0	0.0
Low Pass Attenuation (LF)	0.0	0.0	0.0	0.0	0.0	20.0
Reference multiply	-16.6	-48.6	-78.3	-101.8	-118.3	-120.3
No.1 DRO output	-170.0	-150.0	-150.0	-120.0	-120.0	-130.0
No.2 Reference output	-16.6	-48.6	-78.3	-101.8	-118.3	-140.3
No.3 Pre-scaler output	-125.0	-130.0	-140.0	-150.0	-150.0	-170.0
No.4 Phase detector output	-125.0	-125.0	-125.0	-125.0	-125.0	-145.0
General PDRO's phase nose	-16.6	-48.6	-78.3	-101.7	-115.5	-129.5
19.25G PLDRO PN(X2)	-10.6	-42.6	-72.2	-95.7	-109.5	-123.5

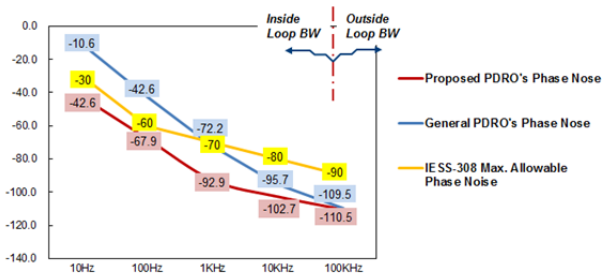

Fig. 7. Graph of the analysis of the phase noise of the proposed PLDRO (9.625 GHz X2 = 19.25 GHz).

Table 5. Summary of Tables 3 and 4

Offset freq.	10 Hz	100 Hz	1 kHz	10 kHz	100 kHz
Digital PLL	-56.3	-88.2	-117.9	-141.5	-158.0
Analog PLL	-16.6	-48.6	-78.3	-101.7	-115.5
After X2	-10.6	-42.6	-72.2	-95.7	-109.5

those of the proposed PLDRO.

IV. Fabrication and Measurement

A PLDRO of 9.625 GHz was implemented on the basis of the proposed PLDRO structure. The frequency is multiplied by two so that the final output frequency is 19.25 GHz. The final output frequency is applied to the local oscillator of the K-band microwave system. In this case, a crystal oscillator of 10 MHz is used for the external reference frequency to obtain the output frequency of 9.625 GHz from the VCDRO. The set values of the individual parameters of the PLLIC are R = 16, REF = 10, and N = 3,850.

The external reference frequency 10 MHz is directly entered into the PLLIC, and the output frequency 9.625 GHz of the VCDRO is divided by four into 2,406.25 MHz. Then, one of the divided frequencies is entered into the PLLIC and another one into the SPD. The phase detector in the PLLIC compares the phase with the VCDRO, and the relevant phase error voltage is connected with the VT terminal of the VCXO. The output frequency 96.25 MHz of the VCXO is multiplied by 25 in the SRD of the SPD to generate 2,406.25 MHz harmonic signals. The phase is compared with that of the output frequency 2,406.25 MHz divided by four of the VCDRO.

As shown in Fig. 8, the VCDRO is designed in the form of a series feedback. The 50-Ω line is connected to the input terminal of the active element to select the location of the DR. therefore, the resonance conditions are formed at the resonance frequency of the dielectric resonator to obtain excellent phase noise characteristics. The VCDRO is designed to oscillate at 9.625 GHz using the BJT element and the high-Q DR (dielectric

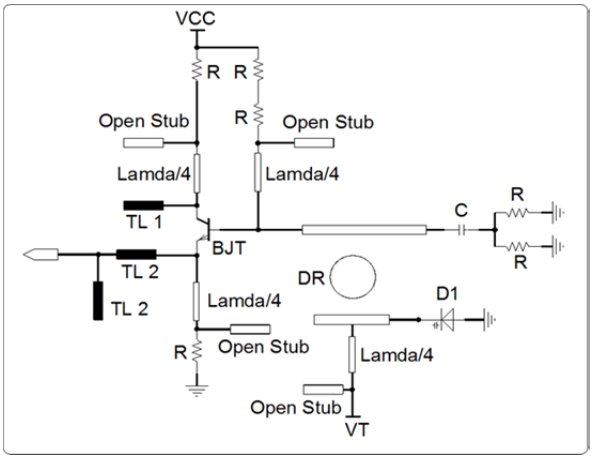

Fig. 8. Voltage-controlled DRO circuit.

resonator). The emitter TL2 of the BJT element is for making the transistor unstable and for output impedance matching. The collector TL1 of the BJT element determines the oscillation frequency and phase noise. The varactor diode (D1) is used to change the internal capacity value of the varactor diode using the phase error voltage output from the SPD through the active loop filter to tune the VT terminal (VT range, 0–12 V).

The analog PLL is implemented with secondary active filters and is designed to have a bandwidth of approximately 100 kHz to obtain optimum phase noise characteristics. To lock the phase, a Schmitt trigger comparator and an integrator are used as frequency acquisition and search circuits, respectively. The integer PLLIC and VCXO (96.25 MHz) with excellent phase noises are adopted for the digital PLL circuit. The doubler is multiplied using passive components, so that it can be operated in the K-band. A band pass filter is applied to remove spurious bands other than the operating frequency.

Fig. 9 shows the output power of PLDRO with +17.07 dBm at the 200 kHz span for 9.625 GHz before multiplication. Fig. 10 presents the output power of PLDRO with +14.43 dBm at the 5 GHz span for 19.25 GHz after multiplication.

The measurement results of the SSB phase noises (dBc/Hz)

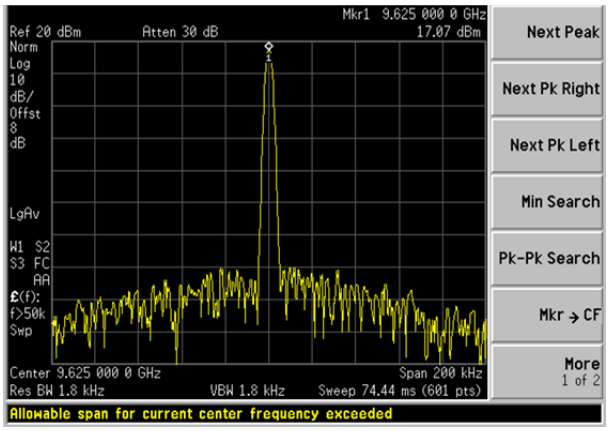

Fig. 9. Measurement results of the output power at the 9.625 GHz output frequency (before multiplication by two).

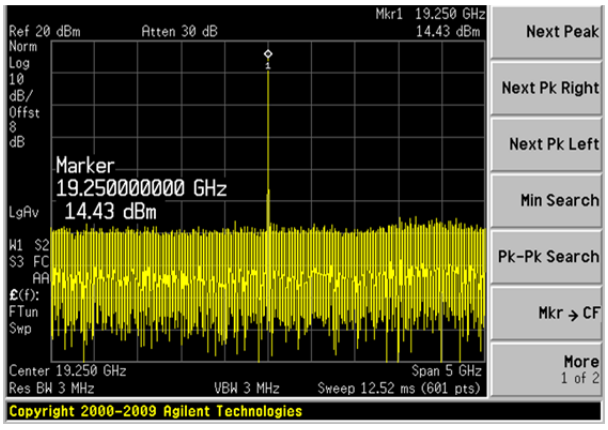

Fig. 10. Measurement results of the output power at the 19.25 GHz output frequency (after multiplication by two).

of the implemented PLDRO at the 9.625 GHz output frequency before multiplication by two and at the 19.25 GHz output frequency after multiplication by two are shown in Figs. 11 and 12, respectively.

The phase noises measured at a 19.25-GHz output frequency after multiplication by two are –96.5 dBc/Hz and –103.3 dBc/Hz at 1 kHz and 10 kHz offset frequencies, respectively. As shown in Table 6, the phase noises are improved by at least 22 dBc/Hz under IESS-308, which is a standard for Intelsat base stations, and the 19.25 GHz K-band after multiplication by two.

In addition, the measurement results are consistent with the

Table 6. Comparison of phase noises measured at 9.625 GHz, 19.25 GHz after multiplication, and IESS-308 standard

Offset freq.	100 Hz	1 kHz	10 kHz	100 kHz	1 MHz
9.625 GHz	-75.2	-99.9	-109.1	-117.8	-132
19.25 GHz	-69.4	-96.5	-103.2	-113.4	-127
IESS-308	-60	-70	-80	-90	-

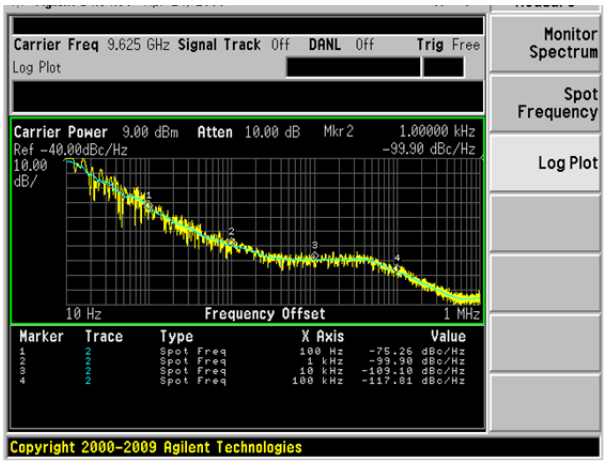

Fig. 11. Measurement results of the phase noises at the 9.625 GHz output frequency (before multiplication by two).

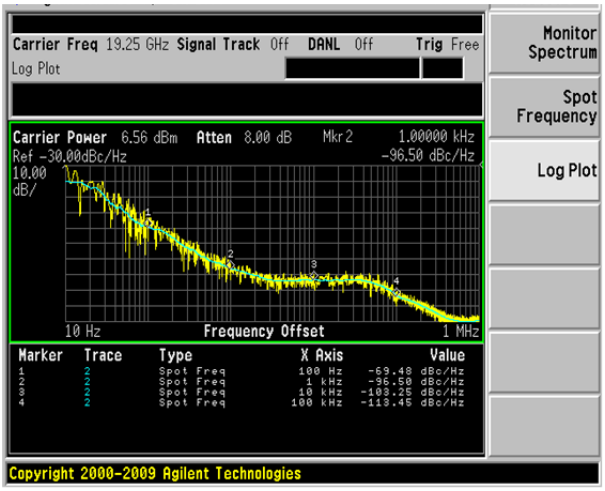

Fig. 12. Measurement results of the phase noises at 19.25 GHz output frequency (after multiplication by two).

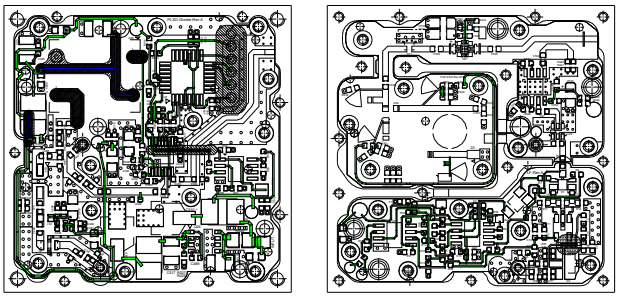

Fig. 13. CAD model of the proposed PLDRO.

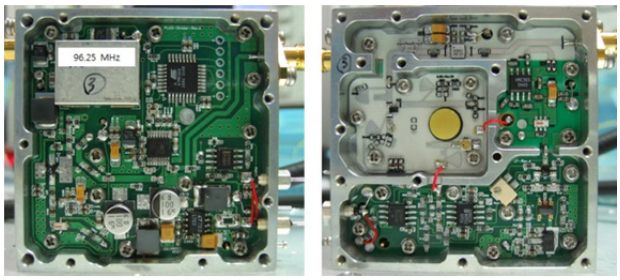

Fig. 14. Real photos of the proposed PLDRO.

phase noise values analyzed and predicted in Section III. The results demonstrate that the proposed PLDRO structure is effective.

Figs. 13 and 14 show the CAD file and photos of the inside of the proposed PLDRO actually fabricated. The left figure illustrates the digital PLL circuit and the right one shows the analog PLL circuit.

V. Conclusion

In the present study, a new PLDRO structure with excellent phase noise characteristics is proposed. PLDROs with low phase noises have been developed to be used as local oscillators in the field of wireless communication, in which PLDROs are installed at the front end of devices.

Based on the proposed structure, the PLDRO in the new form is designed to be used as a local oscillator of transmitter/receiver modules of microwave communication systems, such as radars and EW, without any deterioration of phase noises despite increases in the *N* divider ratio.

The proposed PLDRO structure enables the free adjustment of output frequencies without any deterioration of phase noise characteristics. Moreover, it enables the phase locking at all frequencies regardless of the precision of the frequency of the internal VCXO.

The proposed PLDRO structure is designed in a way that the output frequency of the DRO is coupled and made to pass the divider. The phase is directly compared at the external reference frequency (10 MHz) in the PLLIC, and the error voltage corresponding to the phase difference is used to control the VT terminal of the VCXO. Therefore, the proposed structure does not cause any phase noise deterioration within the loop filter bandwidth in analog PLL circuits. The measured values of the phase noises at the K-band (19.25 GHz) after multiplying 9.625 GHz by two are –96.5 dBc/Hz and –103.3 dBc/Hz at 1 kHz and 10 kHz offsets frequencies, respectively.

This study paves the way for future studies on areas in which complicated (integer multiple of the reference frequency) output frequencies are required using the general external frequency of 10 MHz without causing phase noise deterioration.

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