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FPGA implementation of overhead reduction algorithm for interspersed redundancy bits using EEDC

Hi-Seok Kim*★

Abstract

Normally, in data transmission, extra parity bits are added to the input message which were derived from its input and a pre-defined algorithm. The same algorithm is used by the receiver to check the consistency of the delivered information, to determine if it is corrupted or not. It recovers and compares the received information, to provide matching and correcting the corrupted transmitted bits if there is any. This paper aims the following objectives: to use an alternative error detection-correction method, to lessens both the fixed number of the required redundancy bits *'r'* in cyclic redundancy checking (CRC) because of the required polynomial generator and the overhead of interspersing the *r*in Hamming code. The experimenta lresults were synthesized using Xilinx Virtex-5 FPGA and showed a significant increase in both the transmission rate and detection o frandom errors. Moreover, thisp roposal can be a better option for detecting and correcting errors.

Key words: FPGA, enhanced error detection, Cyclic redundancy checking (CRC), redundancy bits, Hamming code

* Dept. of Electronics Engineering, Cheongju University
★ Corresponding author
e-mail : khs8391@cju.ac.kr, tel : 043-229-8452
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I. Introduction

They are several factors affecting the transmission delay of any data network [1] as it shown in Equation 1. The time to propagate the signal across the medium *t*, the total number of bits in the transmitted message *L*, *R* as the speed of the digital trans mission system and measured in bps, while *d* is the distance covered, measured in meters and the speed of light *c*, respectively are components that affect the transmission delay.

$$Delay = t_{prop} + \frac{L}{R} = \frac{d}{c} + \frac{L}{R} \ (seconds) \qquad (1)$$

These propagation delay problems can be reduced or eliminated by several methods. Previous papers like data compression which minimizes L [2] and the use of higher-speed modulation-demodulation that in creases R [3]

were presented. In doing such methods, it requires a preservation of all the original information, and the data compressions need to belossless [4], or reversible. Therefore, from above equation, reducing the total transmitted bits can lead to a higher transmission rate and the occurrences of errors or corrupted bits needs to be minimized. In able to secure a reliable data transmission, a good error detection and correction scheme is necessary.

In a normal transmission, an extra parity or check bits are added to the input message that derived from this input with a deterministic algorithm. The receiver uses the same algorithm to check the consistency of the delivered information, to determine for any occurrences of errors. It also recovers and compares the received information to provide matching and correction of the corrupted transmitted bits. Remarkable codes about error detections such as the cyclic redundancy checking (CRC) [5] and with correction implementation like the Hamming code are in existence [6]. However, in CRC code, due to the assigned polynomial generator, it reduces the transmission rate. Also, in Hamming code operation, the overhead of interspersing of the computed r is being utilized [7] because of the bit's position follows the power of two bit's system (2^0, 2^1, 2^2…).

In this paper, an alternative error detection-correction method called as enhanced-error detection-correction (EEDC) code is proposed. It is a modified version of any existing error detection and correction codes that eliminates the drawbacks of CRC and Hamming code that causes the reduction of the transmission rate and the overhead of interspersing of the computed r, respectively. The experimental results show that the performance of EEDC performs better against CRC and Hamming codes in terms of transmission rate and detection of random errors, respectively.

The rest of this paper is organized as follows. Section II shows some related literature as the basis of this proposed algorithm. Section III covers the proposed algorithm as an alternative technique for error detections and corrections code. While in Section IV shows the experimental testing and results. Finally, section V concludes this paper.

II. Related Works

1. Cyclic Redundancy Checking (CRC) code

Cyclic Redundancy Checking code is an example of polynomial codes referring to the corresponding polynomial of a codeword [8]. The idea is to represent every codeword $C(x)=C_{n-1}C_{n-2}\cdots C_0$ as a polynomial of degree $n-1$.

That is,

$$C(x) = \sum_{i=0}^{n-1} C_i x^i \qquad (2)$$

The key idea in CRC (or in any cyclic codes) is to ensure that every valid code polynomial is a multiple of a generator polynomial $g(x)$. This polynomial code is the basis for powerful error-correction methods, but it has a fixed number of check bits based on the n^{th} degree of the generator polynomial that is required to attach during transmission, therefore it reduces the transmission rate of the network [9]. Moreover, CRC codes do not implement correction, it only enforced retransmission whenever an error is detected.

Equation (3) shows the straightforward construction of CRC. Taking the input message, assemble the $m(x)$, multiply by x^{n-k}, and then divide that by $g(x)$. The remainder R forms the check bits, acting as the digest for the entire message, and will be appended to the message.

$$C(x) = x^{n-k}m(x) + R\left\{\frac{x^{n-k}m(x)}{g(x)}\right\} \quad (3)$$

The decoding process is identical to the encoding step, it separated each word received into the message and the remainder portion, and it verifies whether the calculated remainder from the message matches the sent bits. A mismatch means that an error has occurred and the receiver will request for retransmission (ARQ) [10] of the message. Although, CRC is simple to implement in binary hardware, it is not suitable for protecting against intentional alteration of data. Also, an overflow of data is possible in CRC.

2. Hamming Codes

Hamming code is a class of error-correcting and linear block codes which used to detect and correct error bits that occur during transmission [11]. In Hamming code, the redundancy bits *'r'* or a parity bits are added to an *n*-bit data word (D), forming a new word of $D + r$ bits and must comply the required number of *'r'* such that

$$2^r \geq D + r + 1 \quad (4)$$

These redundancy bits are to be distributed at bit positions of power of 2 with the original data bits [12]. Then, all other bit positions are assigned for the data to be encoded in the remaining positions (i.e., 3, 5, 6, 7, 9, 11, 13, 14, 15, 17, etc.). As a result, an increase in overhead because of interspersed redundancy bits both for the transmitter and receiver parts. In general, the rule position can be seen in Table 1, the X value is for a non-sequential or random format (don't care).

Table 1. Bits position of data and the assigned Hamming bits for a 7-bit information

Bit Position	1	2	3	4	5	6	7
power of 2 position	2^0	2^1		2^2			
Encoded position	r_1	r_2	D_1	r_3	D_2	D_3	D_4
Required parity bits position for 'r'	r_1		X		X		X
		r_2	X			X	X
				r_3	X	X	X

Moreover, Hamming code is effective on networks where the data streams are prone to a single-bit error as one of its advantages. However, if multiple errors occur, the errors can be detected but the resultant could cause another bit that is correct to be changed, causing the data to occur another error.

III. Proposed Algorithm

Enhanced-Error Detection-Correction (EEDC) codes

The proposed algorithm is a modified version of the conventional Hamming codes. In each valid codeword of C bits contains the valid input data bits D_i. Also, in any valid D_i entity, there are C bits that can be changed to give an invalid codeword. Thus the total number of codeword scorresponding to a valid data entity is C+1. As there are 2^{Di} valid data patterns, the total number of codewords is $(C+1)2^{Di}$. In D_i bit codewords, the possible number of patternsis2^c and this limits the number of valid plusinvalid codes that can exist. Thus,

$$(C+1)2^{Di} \leq 2^c \quad (5)$$

and, it can be written that

$$C = D_i + r \quad (6)$$

and

$$(Di + r + 1)2^{Di} \leq 2^{Di+r} \qquad (7)$$

so the total number of the required redundancy bits should satisfy first the given condition of the inequality below

$$(D_i + r + 1) \leq 2^r \qquad (8)$$

Both the data information D_i and the required r will be constructed into a polynomial form with a degree of n-1 such as

$$D(x) = \sum_{i=0}^{n-1} Dix^i \qquad (9)$$

and

$$r(x) = \sum_{i=0}^{n-1} r_i x^i \qquad (10)$$

Then, the degree of polynomial $D(x)$ will increase with the nth value of r, in such that

$$G(x) = D(x) \bullet X^n \qquad (11)$$

Thus, the complete form of Enhanced Error Detection-Correction codes, as shown in (12).

$$EEDC\,codes = G(x) + r(x) \qquad (12)$$

As an example, let us consider a 7-bit data using this proposed EEDC codes.
The information of this 7-bit data is given as 1001110 in binary form, and its polynomial form is $X^6+X^3+X^2+X$. Therefore, the least number of r to satisfy the above inequality of (8) is4, and its polynomial form will be $r_3X^3+r_2X^2+r_1X+r_0$ and its binary sequence is 10010110000. While the polynomial in (11), $G(x)isX^{10}+X^7+X^5+X^4$.

Then, to identify the appropriate bit of the redundancy bits, considering the above example: r_3, r_2, r_1, and r_0 are in position 8, 9, 10 and 11, respectively. Below are the solutionsin identifying the values of these redundancy bits.
The check bits in position 8 are 1, 3, 5 and 7 positions. Even parity, so r_3 is set to 0.

The check bits in position 9 are 2, 3, 6 and 7 positions. Even parity, so r_2 is set to 1.

The check bits in position 10 are 4, 5, 6 and 7 positions. Even parity, so r_1 is set to 1.

The check bits in position 11 are only on the redundancy bits r_3, r_2, and r_1. Even parity, so r_0 is set to 0.

Then, the EEDC codes for this 11-bit data to be transmitted as $X^{10}+X^7+X^5+X^4+X^2+X$ in polynomial form and it is equivalent $to1001110r_3r_2r_1r_0$, where the bit values of r_3, r_2, r_1, and r_0 are 0110 respectively. The required redundancy bits are to be appended at bit positions 8, 9, 10, and 11.
Thus, the 11-bit data to be transmitted will be 10011100110. The proposed algorithm and architecture is shown in Fig. 1 and Fig. 2, respectively

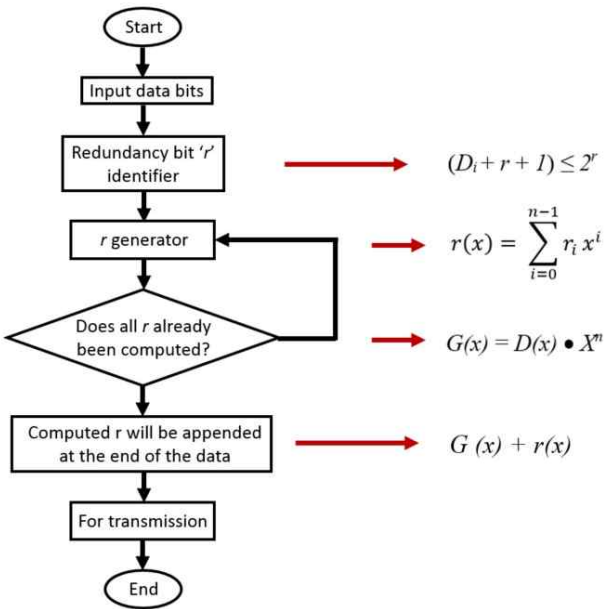

Fig. 1. Algorithm of the proposed method

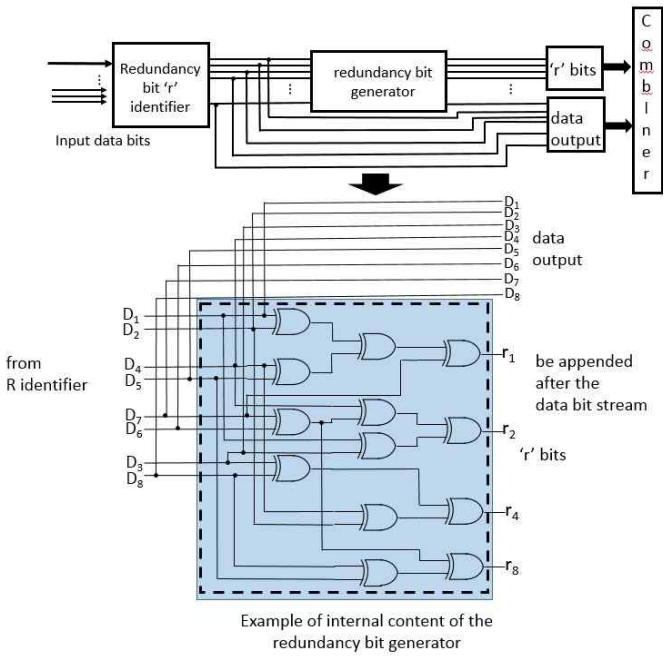

Fig. 2. Architecture of the proposed method

Ⅳ. Experimental Testing and Results

Experimental Testing and Result: This proposed algorithm is synthesized to Xilinx Virtex 5 FPGA by using Xilinx ISE. Table 2 shows the comparison results of the simulated transmission rate between CRC, Hamming codes and the proposed EEDC tested in an 8 bits to 8 bytes data frame of the controller area network (CAN) 2.0A-Frame that includes some of the necessary bits like the Start-of-Frame (SOF) bits, id bits, control bits and etc. The presentation below shows only the data frame portion of CAN.

Table 2. Data rate comparison between CRC, Hamming and the proposed EEDC codes

Transmitted data (bytes)	Data Rate (bits per second)		
	CRC	Hamming	EEDC
1	16,640	19,600	21,040
2	14,280	16,392	20,032
3	12,656	14,280	15,648
4	11,232	12,496	12,800
5	10,200	11,104	11,376
6	9,256	10,000	11,184
7	8,472	9,088	10,752
8	7,872	8,400	8,952

It shows that the transmission rate of the proposed implementations is faster compare with CRC and Hamming Codes. Fig. 3 shows the error detection performance of this proposed algorithm is better to compare with CRC and Hamming codes.

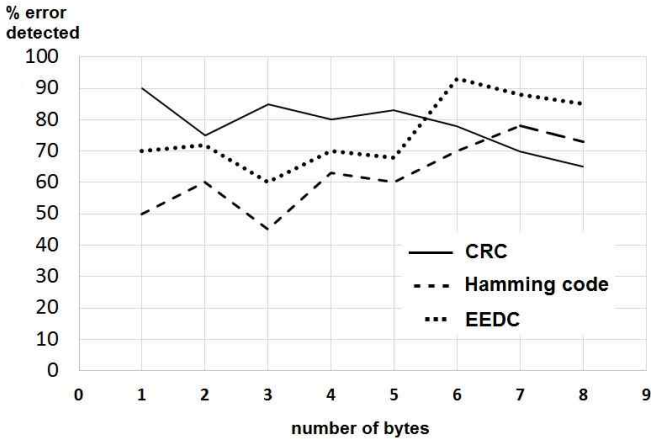

Fig. 3. Error detection performance of CRC, hamming and EEDC codes

Ⅴ. Conclusion

In this letter, the proposed enhanced error correction and detection (EEDC) codes can be used as an alternative error detection and correction scheme in data communication. The simulation results show that the objectives meet its target in aiming a faster transmission rate compare with the implementation of CRC because of the fix data frame of the required polynomial generator and to avoid the overhead payload that exists in Hamming codes. Moreover, it shows that the error detection performance has a better result.

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BIOGRAPHY

Hi-Seok Kim (Member)

1980 : BS degree in Electronic Engineering, Hanyang University.
1985 : MS degree in Electronic Engineering, Hanyang University.
1987 : Ph. D degree in Electronic Engineering, Hanyang University.
1987~current : Professor, Dept. of Electronics Engineering, Cheongju University, CheongJu-si, South Korea.
2012 : General Chair and a committee member of many Korean an International Conferences, including International SoC Design Conference and IEEE ISCAS 2012
<Research interests> digital video/audio system design, multi-view imaging, 3D image processing, and FPGA design.