JOURNAL OF SEMICONDUCTOR TECHNOLOGY AND SCIENCE, VOL.17, NO.3, JUNE, 2017
https://doi.org/10.5573/JSTS.2017.17.3.438
ISSN(Print) 1598-1657
ISSN(Online) 2233-4866

A Low-power High-resolution Band-pass Sigma-delta ADC for Accelerometer Applications

Cao Tianlin[1], Han Yan[1,*], Zhang Shifeng[1], Ray C. C. Cheung[2], and Chen Yaya[1]

***Abstract*—This paper presents a low-power high-resolution band-pass ΣΔ ADC for accelerometer applications. The proposed band-pass ΣΔ ADC consists of a high-performance 6-th order feed-forward ΣΔ modulator with 1-bit quantization and a low-power, area-efficient digital filter. The ADC is fabricated in 180 nm 1P6M mixed-signal CMOS process with a die area of 5 mm^2. This high-resolution ADC got 90 dB peak signal to noise plus distortion ratio (SNDR) and 96 dB dynamic range (DR) over 4 kHz bandwidth, while the intermediate frequency (IF) is shifting from 100 KHz to 200 KHz. The power dissipation of the chip is 5.6 mW under 1.8 V (digital)/ 3.3 V (analog) power supply.**

***Index Terms*—Band pass, ΣΔ ADC, low-power, high-resolution, accelerometer**

I. INTRODUCTION

The demand of high performance accelerometer is growing rapidly in many areas, such as guidance, navigation, seismometry, and automotive applications [1]. All of these applications require low power consumption and high accuracy readout circuits, in other words the analog to digital converters (ADCs). Recently, many works have taken advantage of the micro-machined silicon accelerometers and assembled it with the ADCs, to realize an acceleration transducer SOC (system on chip). Meanwhile in those kinds of accelerometer systems, the performance of the ADC could be the bottle neck of the whole system [2, 3].

ΣΔADC which can achieve high resolution without stringent accuracy requirements on the analog components is proved to be the most efficient way to achieve demands of both power and accuracy [4, 5]. In many micro mechanical sensor applications, the signal frequency is at hundreds of kilohertz, while the bandwidth is not that high [6]. Therefore, a band-pass ΣΔADC is the proper way to meet the accelerometer applications' demands.

However, none of the band-pass ΣΔADC has been published with the similar characters: working at hundreds of kilohertz with low power and high resolution in sensor bandwidth. This paper proposed a low-power high-linearity band-pass ΣΔADC aim at accelerometer applications. A full feed forward topology band-pass sigma delta modulator is proposed to achieve high resolution and stability at the same time. Section II is devoted to the description of the analog modulator architecture and stability considerations. The main circuits of the modulator and the digital filter are described in section III. Section IV presents the experimental results of the proposed design. This paper is concluded in section V.

II. ARCHITECTURE

Fig. 1 shows the architecture of the proposed band-pass sigma delta modulator. A 6th order loop filter with 1 bit quantizer is chosen to achieve a high dynamic range over 4 KHz bandwidth. Considering stability and spectral tones rejection, a single loop feed-forward architecture is proposed. The high-order single-bit modulator is

Manuscript received Oct. 12, 2016; accepted May. 12, 2017
[1] Institute of Microelectronics, Zhejiang University, China
[2] Department of Electronic Engineering, City U, Hong Kong
E-mail : hany@zju.edu.cn

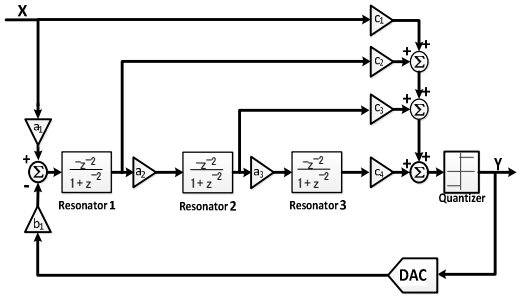


Fig. 1. Block diagram of the 6-th order feed-forward modulator.

competitive due to their intrinsic linearity, no power or area overhead is needed for the feedback circuits [7].

The most popular architecture of band-pass ΣΔ modulator is cascaded resonators with feedback loop (CRFB) [8, 9]. But the feedback topology needs high performance analog amplifiers, and the overload level is low. It suffers from linearity and stability problems, especially in the high order single loop designs [10]. This paper adopted the full feed-forward structure in band-pass ΣΔ modulator design, to reduce the analog block requirements and enhance the system stability. By analyzing the signal flow of the sixth order full feed-forward architecture from Fig. 1, the signal transfer function (STF) $H_s(z)$, and noise transfer function (NTF) $H_E(z)$ can be obtained as following equations:

$$H_s(z) = 1 \tag{1}$$

$$H_E(z) = 1 \Big/ \left[1 + H_f(z)\right] \tag{2}$$

where $H_f(z)$ is the forward path transfer function.

Then the input signal of the first resonator $RI_1(z)$ is:

$$RI_1(z) = X(z) - Y(z) \tag{3}$$

$$Y(z) = H_S(z) \cdot X(z) + H_E(z) \cdot E(z) \tag{4}$$

$$RI_1(z) = -H_E(z) \cdot E(z) \tag{5}$$

The full feed-forward topology with reduced sensitivity to integrator nonlinearities [11, 12], makes it appropriate in high resolution applications. Compared to a feedback topology, the quantization noise transfer function of the feed-forward topology remains the same and the signal transfer function is unity. It's clearly shown that the loop filter only processes the quantization noise, and this means that not only the voltage swing inside the loop is reduced, but also the distortions introduced by the switches and analog amplifiers are attenuated. So that the proposed modulator is hard to be affected by the non-idealities of analog building blocks and reduces the voltage swing inside the loop at the same time. In this modulator, the internal signal swing can be well controlled by optimizing the loop coefficients, thus reducing modulator distortion significantly. Besides, the fact that only one feedback DAC is needed remarkably simplifies the feedback circuit, which is especially helpful for high-order design.

One of the key design parameters of ΣΔM is the maximum out of band quantization noise gain (Qmax) [13]. When the gain is high, the in-band noise shaping provides sharper attenuation of the quantization noise. However, increasing Qmax beyond a certain level can also deteriorate the modulator stability. The poles of the NTF tends to induce internal oscillations at their respective frequencies. It is necessary to have an optimum Qmax for which the modulator can reach a maximum SNDR within the stability limit. The selection of Qmax is a trade-off between stability and the aggressiveness of the noise shaping. According to Lee's rule, the Qmax of a single bit modulator must be less than 2 to maintain stable modulator performance, which is also applicable for band-pass type SDMs. In this work, the value of Qmax is set at 1.96, which is close to 2, to get a good noise shaping performance while the modulator remain stable. Fig. 2 shows the poles, zeros and the noise transfer function of the proposed modulator.

The modulator consists of three stages of switched capacitor resonators. And the feedback reference voltages are selected as VDD and GND, in which way it can not only reduce power consumption but also enlarge the modulator's input range to full scale. Bootstrap switches are adopted in the sampling and hold circuit in order to provide sufficient low switch resistance, and improve the switch linearity [14]. Considering power and area cost, CMOS and NMOS switches are used in other signal paths. The switched-capacitor resonators are controlled by multi-phase, non-overlapping clocks. Clocks at the sampling circuits are designed with advanced falling edge clocks, in order to suppress the channel charge injection.

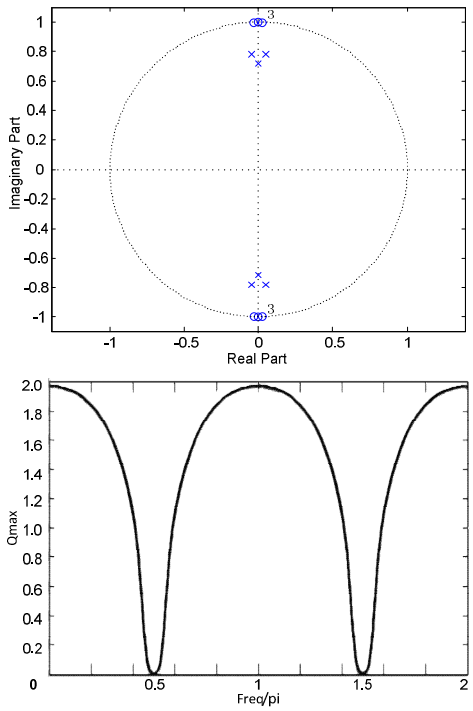


Fig. 2. Poles, Zeros and NTF.

III. CIRCUIT DESCRIPTION

1. Operational Transconductance Amplifier

A two-stage telescopic operational trans-conductance amplifier is adopted for high voltage gain, low power dissipation and low noise. Fig. 3 shows the details of the OTA circuit. The cascade structure is adopted in the first stage to achieve a high voltage gain. The second stage is a common source NMOS with an active PMOS load to get large output range. A miller capacitance introduces the first pole between two stages, and the output pole becomes the second one. With a compensatory resistor, the RHP (right half plane) zero can be cancelled. Therefore the OTA is stable. M13~M19 form a CMFB (common mode feedback) circuits. So that the common mode and differential mode input stages share current mirrors and output loads [15, 16]. It could not only reduce the power consumption, but also equalize the AC characteristic of these two paths. Moreover, once the differential loop is stable, the common loop is stable.

According to different requirements of loads and noise levels, the OTAs in different stages were optimized separately. The GBW and power consumption of three OTAs in three resonators are listed in Table 1.

Table 1. parameters of three OTAs

OTAs	GBW/ MHz	Power/ mW
1st stage	60	1.44
2nd stage	40	0.97
3rd stage	45	1.06

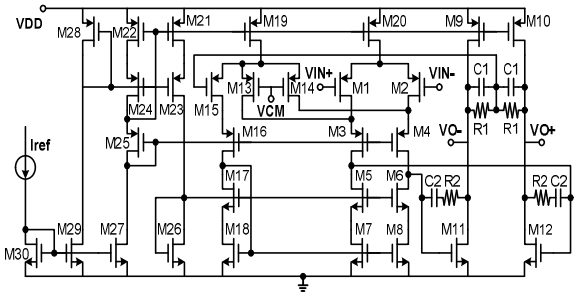


Fig. 3. Fully differential two-stage telescopic OTA with CMFB.

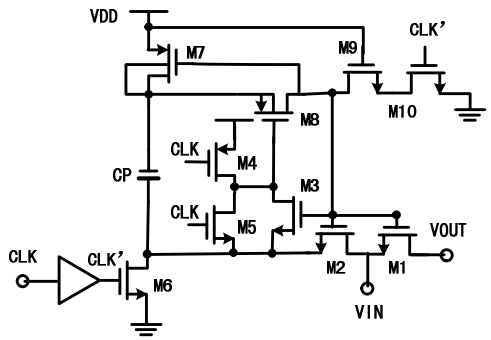


Fig. 4. Bootstrap switch.

2. Bootstrap Switches

High linearity and low on-resistance switches are needed in the sampling and hold circuits. The performance of the switches directly influences the harmonic distortion and inter-modulation, which are very important to the sigma delta modulator. Since common CMOS switches can't satisfy high linearity demand, Bootstrap switches are appropriate choice [14, 17]. The schematic of the bootstrap switch circuit is shown in Fig. 4. The switch is controlled by clock CLK. When CLK is low, the switch is off. MOSFETs M4, M6, M7, M9, M10 turn on, and M1, M2, M3, M5, M8 turn off. The voltage of is capacitor CP is charged to VDD at the same time. When CLK becomes high, M1, M2, M3, M5, M8 turn on, the voltage between M1's gate and drain remains VDD, irrespective of input voltage. M5, M9 are used to ensure

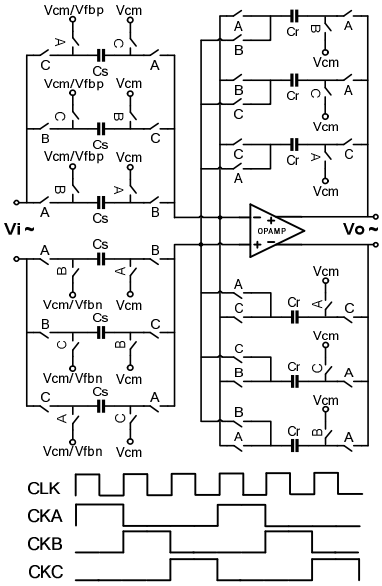


Fig. 5. Operation mode of the SC resonator.

the reliability of the circuit [18]. Simulation results prove that the harmonic distortion of this switch is 50 dB less than CMOS switch.

3. Resonators

Fig. 5 illustrates the operation mode of the SC resonator. Signal scaling can be realized by appropriately choosing the ratio between C_s and C_r. The transfer function of the resonator $\mathrm{H_r(z)}$ is:

$$H_r(z) = -\frac{C_s}{C_r} \cdot \frac{Z^{-2}}{1+Z^{-2}} \tag{6}$$

From the transfer function of the resonator, we can find a way to realize the band-pass modulator from the low pass modulator directly by changing the parameter Z^{-1} to $-Z^{-2}$. In this way, the central signal frequency is at a quarter of the sampling frequency f_s [19]. In this proposed modulator, the frequency of the operation clocks CLKA, CLKB, CLKC are all 1/3 times of f_s, which means the distortion introduced by the operation clocks appears at 1/3 f_s, 2/3 f_s and f_s. Those are all located outside the signal band.

With a comprehensive consideration of capacitance mismatch, noise level and area, the value of C_s and C_r in three resonator stages are chosen as Table 2.

Table 2. Capacitance Value

Capacitance / pF	C_s	C_r
1st stage	6	20
2nd stage	2	5
3rd stage	2.4	6

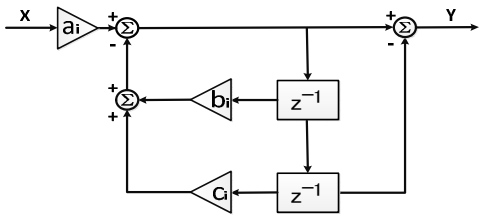


Fig. 6. Architecture of the i-th stage in digital filter.

4. Digital Filter

The sigma delta modulator removes most of the quantization noise inside signal band. A band-pass digital filter is cascaded behind the sigma delta modulator to attenuate the noise floor out of band to the same level as the in band noise. Though the analog modulator is the determined part of the ADC, the digital filter also plays an important role in layout area and power dissipation, especially in applications which have strict requirements with the out-of-band noise. In this project, we designed a band-pass digital filter which has only 0.001 dB pass band ripple and 110 dB stop band attenuation.

The multi-stage architecture offers significant reduction of computation and storage requirements compared to a single stage, which is a main target of the design [20]. In this paper, a 10 stages digital filter is adopted. Since the pass band is at a quarter of sampling frequency f_s, we can design the basic digital filter transfer function as :

$$H_F(z) = \frac{a \cdot \left(1 - Z^{-2}\right)}{1 + b \cdot Z^{-1} + c \cdot Z^{-2}} \tag{7}$$

Fig. 6 shows the architecture of the i-th stage of the band-pass digital filter. By carefully choosing the value of parameter a_i, b_i, and c_i, the gains and poles of the transfer function $H_F(z)$ can be optimized until the 10 stage filter meet the requirement. When i+j=11, the i-th parameters are symmetric with the j-th parameters, resource sharing is also considered in the RTL coding to

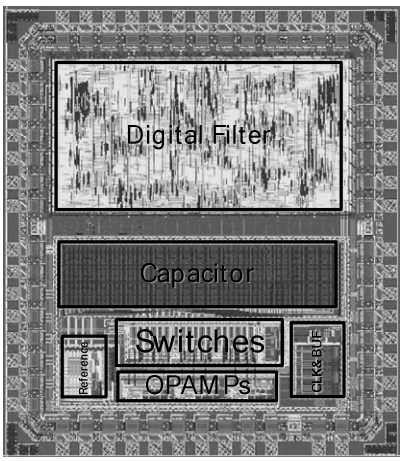


Fig. 7. Microphotograph of proposed ΣΔ ADC.

save the hardware cost. There are 31 coefficient in total, including a normalization parameter at the output stage. The gate count of the digital filter is 49.75 thousands.

IV. MEASUREMENT RESULTS

The proposed ΣΔ ADC is implemented in a standard 180-nm 1P6M CMOS mixed-signal process. The chip microphotograph is shown in Fig. 7.

The reference circuits are used to generate reference currents (Iref in Fig. 3) for the OTAs. The whole chip (including IO pads) occupies a core area of 2.39×2.1 mm^2. The analog modulator consumes 5.0 mW from a single 3.3-V power supply, the digital filter consumes 0.6 mW under 1.8-V power supply. The power consumption of the whole chip is 5.6 mW.

Fig. 8 shows the band-pass sigma delta modulator's output spectrum at 156 KHz IF with 2^18 points DFT. The detailed spectrum and SNDR vs. input signal power curve of the proposed band-pass ΣΔ ADC are exhibited in Fig. 9.

The ADC performs a 96-dB DR, 90-dB SNDR within 4 KHz bandwidth. The chip was also tested under 10% supply voltages, the DR and SNDR vary within 1 dB. The analog modulator part is also tested separately under same conditions, the results illustrated that the deterioration introduced by the digital filter is smaller than 0.6 dB.

Table 3 summarizes the specifications of the proposed ΣΔ ADC. Since the accelerometer application is very special, few of similar and recently reported BPSDMs can be found. Besides, only sigma delta modulators

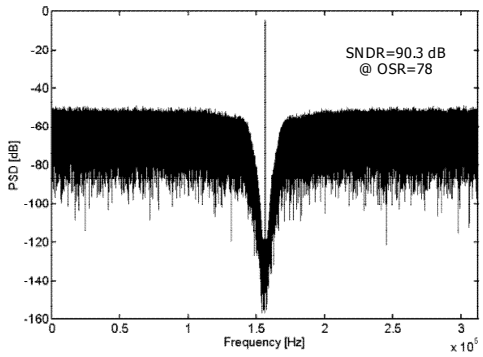


Fig. 8. Measured band-pass ΣΔ modulator Output spectrum.

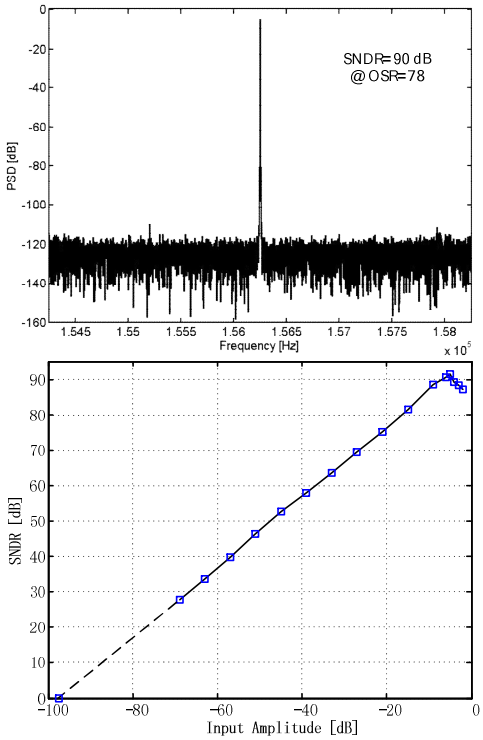


Fig. 9. Measured ADC Output spectrum & SNDR versus input signal power, IF=156 KHz.

(without digital filter) can be found in the published articles. Comparisons of the modulators between this work and some similar literature are listed in Table 4.

We use two kinds of FOMs [19, 24] to measure the performance. The FOMs are defined as:

$$FOM_{SNDR} = \frac{\text{Power}}{2^{(SNDR-1.76)/6.02} \times 2 \times \text{BW}} \quad \text{(the smaller the better)} \tag{7}$$

$$FOM_{DR} = DR + 10 \cdot \log\left(\frac{\text{BW}}{\text{Power}}\right) \quad \text{(the bigger the better)} \tag{8}$$

Table 3. ΣΔ ADC performance summary

Specification	value
Power supply	3.3/1.8 V
Oversampling ratio	50~100
Bandwidth	4 KHz
Sampling rate	400~800 KHz
Power consumption	5.6 mW
SNDR	90 dB
Dynamic range	96 dB
Area	5 mm^2
Process	180 nm

Table 4. Comparison of modulators

	Ref. [21]	Ref. [22]	Ref. [23]	This work
Process/ μm	0.25	0.35	0.35	0.18
Supply/ V	1.0	3.3	3.3	3.3
Power/ mW	8.45	61	76	5.0
BW/ kHz	30	200	200/9	4
DR/ dB	82	85	74/88	97
SNDR/ dB	78.5	73	61/75	90.3
FOM_1/ pJ/step	20.4	41.58	206/914	23.25
FOM_{DR}/ dB	148	153	138/139	156

Here, DR, SNDR, BW and Power represent the dynamic range, signal to noise plus distortion ratio, signal bandwidth, and the power consumption, respectively. Compared to other published modulators, the proposed modulator shows good performance in terms of FOMs.

V. CONCLUSIONS

A low power high resolution band-pass ΣΔ ADC for accelerometer applications is implemented in 180 nm mix-signal CMOS technology, integrating a high performance analog modulator and a digital filter in a single chip. With single-bit quantification and high linearity bootstrap switches, the modulator gets a high SNDR and DR. Using a low noise large output swing OTA, not only the noise can be greatly inhibited, but also the power consumption is reduced. Also, a low-power, area-efficient band-pass digital filter was designed. The measurement result shows a 90 dB peak-SNDR and 96 dB DR are achieved over 4 KHz bandwidth. The power consumption of the ADC chip is 5.6 mW, which is suitable for low power high resolution sensor applications.

ACKNOWLEDGMENTS

This work was supported by a grant from National Natural Science Foundation of China (General Program, No. 61274035).

REFERENCES

[1] Yazdi N, Ayazi F and Najafi K. Micromachined inertial sensors. PIEEE 1998; 86(8): 1640–1659.

[2] K Najafi, J Chae, H Kulah, G He, Micromachined silicon accelerometers and gyroscopes [C]. IEEE International Conference on Intelligent Robots & Systems, vol. 3, no. 3, pp. 2353-2358, 2003.

[3] Zhu, Zhongyi; Liu, Yidong; Jin, Zhonghe, A low power digital processing circuit for capacitive accelerometer [J]. Proceedings of the Institution of Mechanical Engineers Part N: Journal of Nano-engineering & Nanosystems, 227(2), pp 51-55, 2013.

[4] CANDY J.C., TEMES G.C. EDS. :‘Oversampling delta– sigma data converters: theory, design, and simulation’ . IEEE Press, New York, 1992.

[5] Liao Lu, Sun Ying, Han Yan etc. A 65-nm low-power high-linearity sigma delta ADC for audio applications[J]. Science China Information Sciences, 57(4), pp 1-7, 2014

[6] Zhang X, Wang H, Zheng X-D, et al. Modeling and noise analysis of a fence structure micromachined capacitive accelerometer system [J]. Journal of Zhejiang Univ: Sc C 2010; 11(12):1009–1015.

[7] Ritoniemi T, Karema T, Tenhunen H, A fifth order sigma-delta modulator for audio A/D-converter [C]. Analogue to Digital and Digital to Analogue Conversion, 1991.International Conference on. Page(s):153 - 158

[8] R.G. Chang, C.Y. Chen, J.H. Hong, S.Y. Lee, Wide dynamic-range sigma-delta modulator with adaptive feed-forward coefficients[J]. Circuits, Devices & Systems, IET , Volume:4, Issue: 2, pp.99 – 112, March 2010.

[9] H Luo, Y Han, R C C. Cheung , X P Liu, T L Cao. A 0.8-V 230-W 98-dB DR Inverter-Based sigma delta Modulator for Audio Applications [J]. IEEE Journal of Solide State Circuits, Volume.48, Issue.10, pp.2430-2441, 2013

[10] S. M. Moussavi, B. H. Leung, "High-Order Single-Stage Single-Bit Oversampling A/D Converter Stabilized with Local Feedback Loops,"[J] IEEE Trans. Circuits & Syst. II, vol.41, no.1, pp.19-25, Jan.1994.

[11] J. Silva, U. Moon, J. Steensgaard, and G.c. Ternes, "Wideband low-distortion delta-sigma ADC topology"[J]. Electronics Letters, vol. 37, no. 12, pp. 737-738 , June 2001.

[12] L. Yao, M. Steyaert and W. Sansen Low-Power Low-Voltage Sigma-Delta Modulators in Nanometer CMOS, 2006 :Springer

[13] R. Jiang, T. S. Fiez, A 14-bit ΔΣ ADC with 8×OSR and 4-MHz Conversion Bandwidth in a 0.18-um CMOS Process, IEEE J. Solid State Circuit, 39(1) (2004) 63-74.

[14] M. Daliri M. Maymandi-Nejad K. Mafinezhad. Distortion analysis of bootstrap switch using volterra series [J]. Circuits, Devices & Systems, IET , Volume:3, Issue: 6, pp.359 – 364, December 2009.

[15] M Banu, J M Khoury, Y Tsividis. Fully differential operational amplifiers with accurate output balancing[J]. IEEE Journal of Solid-State Circuits, 1988, Vol. 23, pp. 1410-1414.

[16] Mariadel Mar Hershenson, Stephen P. Boyd, Thomas H. Lee, Optimal Design of a CMOS Op-amp via Geometric Programming[J], IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2001, Vol. 20, pp. 1-21

[17] M. Dessouky, A. Kaiser, 'Very low-voltage digital-audio ΔΣ modulator with 88-dB Dynamic Range using local switch bootstrapping' [J]. IEEE J. Solid-State Circuits, Vol.36, No.3, March 2001, pp.349-355.

[18] Fayomi C J B, Robers G W, Sawan M. Low-voltage CMOS analog bootstrapped switch for sample-and-hold circuit: design and chip characterization[C]. IEEE international Synposium on Circuits and Systems. Kobe: [S.N.], 2005: 220

[19] R. Schreier, G. C. Temes, Understanding Delta-Sigma Data Converters. New Jersey: John Wiley & Sons, 2005.

[20] J. C. Candy, "DECIMATION FOR SIGMA DELTA-MODULATION," IEEE Transactions on Communications, 1986, 34(1): pp. 72-76.

[21] C. Kuo and S. Liu, "A 1-V 10.7-MHz fourth-order bandpass ΔΣ modulators using two switched opamps," IEEE J. Solid-State Circuits, vol.39, no. 11, pp. 2041–2045, Nov. 2004

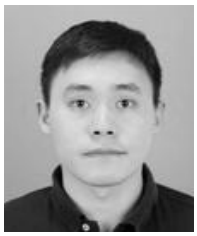
[22] M.Kwon and G.Han,"An I-Q-channel time-interleaved band-pass Sigma-Delta modulator for a low-IF receiver"[J]. IEEE Trans. Circuits Syst. II, Exp. Briefs., vol. 54, no. 3, pp. 252–256, Mar. 2007.

[23] P. Cusinator, D. Tonietto, F. Stefani, and A. Baschirotto, "A 3.3-V CMOS 10.7-MHz sixth-order bandpass modulator with 74-dB dynamic range," IEEE J. Solid-State Circuits, vol. 36, no. 4, pp. 629–638,Apr. 2001.

[24] J. Zhang, Y. Lian, L. Yao, et al. A 0.6-V 82-dB 28.6-μW Continuous-Time Audio Delta-Sigma Modulator, IEEE J. Solid-State Circuits, Oct. 2011, 46(10), pp.2326-2335.

Cao Tianlin received the B.S. degree in the Department of Information Science and Engineer-ing from Ocean University of China, China, in 2011. He is currently working toward the Ph.D. degree at the Institute of Micro-electronics and Nanoelectro-nics, Zhejiang University, Zhejiang, China. His current research mainly focuses on CMOS mixed-signal integrated circuits. His ongoing work includes low voltage bandgap reference and high resolution sigma-delta data converters.

Han Yan received the B.S., M.S., and Ph.D. degrees from the Electrical Engineering Department, Zhejiang University, China, in 1982, 1990, and 1995. She is currently with the Institute of Microelectronics and Nanoelectronics, Zhejiang University, where she was appointed a Professor in 2002, and Ph.D. supervisor in 2003. Her research team ICLAB of Zhejiang University focuses on the following research topics: high performance mixed signal ICs, RF ICs, power ICs, ASICs and ESD protection.



Zhang Shifeng was born in Hangzhou, China, in 1986. He received the B.S degree in electronics science and technology, the Ph.D. degree in microelectronics from Zhejiang University, China in 2009 and 2014, respectively. Now he is associate researcher in Zhejiang University. His research interests are in the area of smart power integrated circuit and power device design.

Ray C. C. Cheung received the B.S. and M.S. degrees in computer engineering and computer science and engineering from the Chinese University of Hong Kong, Hong Kong, in 1999 and 2001, and the Ph.D. degree and D.I.C. degree in computing from Imperial College London, U.K., in 2007. He is currently an Assistant Professor in the Department of Electronic Engineering at City University of Hong Kong. His research focuses on the following topics: reconfigurable trusted computing, SoC VLSI designs, cryptography, and embedded biomedical VLSI designs.

Chen Yaya received the B.S. degree in electronic science and technology from Hunan University, Hunan, China, in 2013 and is working for the Ph.D. degree in electronic science and technology from Zhejiang University, Zhejiang, China, from 2013. Her doctoral work is focused on the design of high-speed high-precision delta-sigma DACs.