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Effects of Ohmic Area Etching on Buffer Breakdown Voltage of AlGaN/GaN HEMT

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This study is on how ohmic area etching affects the buffer breakdown voltage of AlGaN/GaN HEMT. The surface morphology of the ohmic metal can be improved by whole etching on the ohmic area. The buffer breakdown voltages of the samples with whole etching on the ohmic area were improved by the suppression of the metal spikes formed under the ohmic contact regions during high-temperature annealing. The samples with selective etching on the ohmic area were investigated for comparison. In addition, the buffer leakage currents were measured on the different radii of the wafer, and the uniformity of the buffer leakage currents on the wafer were investigated by PL mapping measurement.

Keywords: HEMT, AlGaN/GaN, Buffer breakdown, Leakage current

1. INTRODUCTION

AlGaN/GaN heterostructure transistors are great candidates for power and switching applications because of their high-saturation electron velocity and high breakdown voltage [1,2].

The breakdown voltage of the AlGaN/GaN HEMT was affected by gate breakdown or the GaN buffer-layer breakdown. The gate breakdown voltage has been improved by using field plates or certain surface-treatment processes [3,4]. Therefore, the GaN buffer-layer breakdown on AlGaN/GaN HEMT needs to be further investigated. The AlGaN buffer was used to improve the breakdown voltage of the AlGaN/GaN HEMT [5]. Dora et al. reported the effect of ohmic contacts on the buffer leakage in GaN transistors [6]; the generation of high buffer leakage current was attributed to the electric-field lines concentrated at the metal spikes in the alloyed region of the ohmic contacts. InAlN/AlN/GaN MISHEMT with a higher breakdown voltage was reported [7], and the metal spikes on the smooth surface of the ohmic contacts were reduced by using the schottky source/drain structure [8]. Effects of metal spikes on the leakage current of the GaN buffer were reported, and the formation of the metal spikes under the ohmic contacts was related to the temperature of the ohmic metal annealing [9]. In this paper, processes to etch the different ohmic areas were used to investigate the GaN buffer layer breakdown. Moreover, the distribution of the buffer-layer leakage current on different radii of the wafer was analyzed by a photoluminescence mapping measurement.

2. DEVICE FABRICATION

The test structures were fabricated on Al0.27Ga0.73N/GaN heterojunctions grown by depositing metal-organic chemical vapor (MOCVD) on a (0001) sapphire substrate. The growth process was started with a 330 μm sapphire substrate, followed by the growth of a 1.8-μm unintentionally doped GaN buffer layer, a 20 nm unintentionally doped AlGaN barrier layer, and finally a 1 nm undoped GaN cap layer. The test structure of the buffer breakdown voltage is shown in Fig. 1. The distance between two ohmic contact electrodes was 2 μm. The 2-D electron gas (2DEG) outside the electrodes was etched. I-V measurement between the two ohmic contact electrodes was used to characterize the leakage current and the buffer breakdown voltage between the mesas. The golden regions in Fig. 1 were ohmic metal electrodes. Figure 2 shows the

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Fig. 1. Picture of buffer leakage test structure.

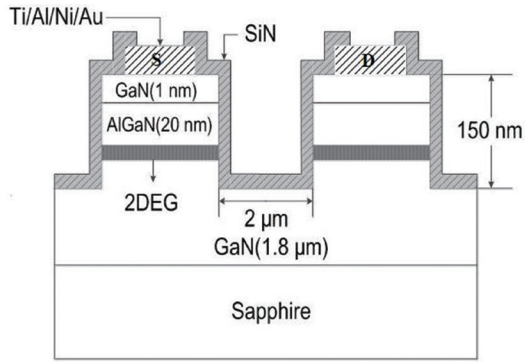

Fig. 2. The cross section of ISO test structure.

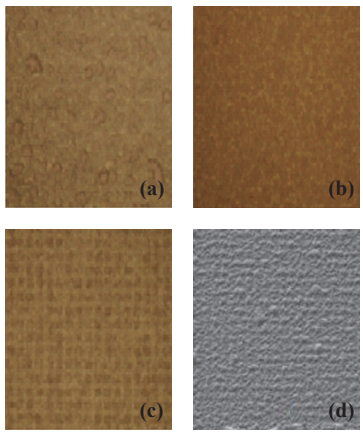

Fig. 3. Surface morphology of ohmic electrode regions: (a) conventional ohmic electrode surface, (b) whole etching ohmic electrode surface, (c) selective etching ohmic electrode surface, and (d) SEM of selective etching ohmic electrode surface.

cross section of the test structure.

The device isolation of the active region was formed by using Cl_2 plasma etching of a reactive ion etching (RIE) system, and the depth of etching was 150 nm. Before the ohmic metal deposition, there were three different preprocessing conditions—listed as A, B, and C—for the ohmic electrodes area.

Condition A was the conventional preprocess for the ohmic area. Before ohmic electrodes metal deposition, the ohmic area was treated in 30s O_2 plasma + 30s HCl solution to remove the residual photoresistance.

In condition B, the ohmic area was treated on 15s~25s Cl_2 plasma in RIE + 30s HCl solution to etch a certain thickness of the material surface.

In condition C, the ohmic area was treated with selective etching in 15s~25s Cl_2 plasma in RIE + 30s HCl solution to etch a partial material surface.

Condition A, B, and C used a partitioning exposure process of the stepper on the same wafer. The ohmic contact electrode metal was formed with Ti/Al/Ni/Au annealed at 830℃ for 30s. The surface morphologies of the ohmic electrode regions in conditions A, B, and C were observed by an optical microscope, as shown in Fig. 3. The SEM of a selective etching ohmic electrode surface is shown in Fig. 3(d).

The photos of the ohmic electrode regions revealed that the surface of a conventional ohmic electrode surface had the roughest surface morphology, whereas the whole etching structures showed the smoothest surface. The selective etching process improved the surface morphology more than that on the conventional structures to some extent as well. By applying the etching process, irregular oxide layers and pollutants on the surface of the AlGaN were removed, which helped to reduce the spikes in the alloyed region of the ohmic contacts. The characteristics of the buffer leakage current were measured by using the Keithley 4200 semiconductor parameter analyzer, and contact resistances were determined by current-voltage measurements employing a linear transfer line method (TLM).

3. RESULTS AND ANALYSIS

TLM patterns with spacings from 3 to 20 μm were used for the contact resistance measurement. Resistance measurements between each pair of contacts can be used to construct the TLM graph, as shown in Fig. 4. The measured total resistance is R = (L/W)RS + 2RC. From the graph, the parameter RC can be determined. In the limit of a zero-length resistor, the total resistance would be just twice the contact resistance. These can be found from Fig. 4 by extrapolating back to L = 0. The contact resistance for conventional structures, whole etching structures, and selective etching structures were 0.46 Ω · mm, 0.35 Ω · mm, and 0.18 Ω · mm, respectively.

The contact resistances of the whole etching structures and the selective etching structures in terns of varying etching times. Compared with conventional structures (represented by an etching time of 0s), after 20s of etching time, the contact resistance decreased from 0.46 Ω · mm for conventional to a minimum of 0.35 Ω · mm for the whole etching structure and 0.18 Ω · mm for the selective etching structure. On the one hand, the lower contact

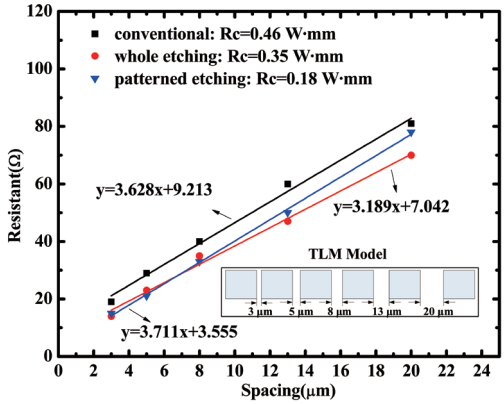

Fig. 4. Linear curve fits of the TLM measurement results for determining contact resistances.

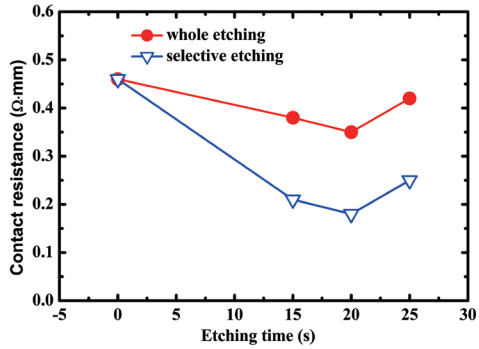

Fig. 5. Dependence of the contact resistances on the etching times of whole etching structures and selective etching structures.

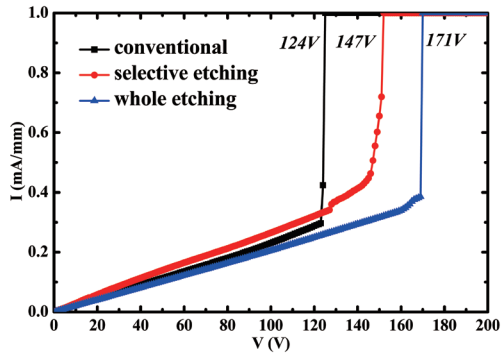

Fig. 6. Breakdown voltages of conventional structures, selective etching structures, and whole etching structures.

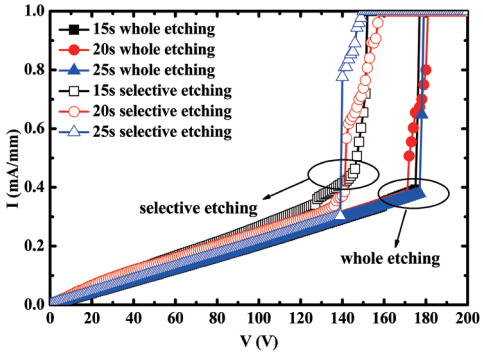

Fig. 7. Breakdown voltages of selective etching structures and whole etching structures with various etching times.

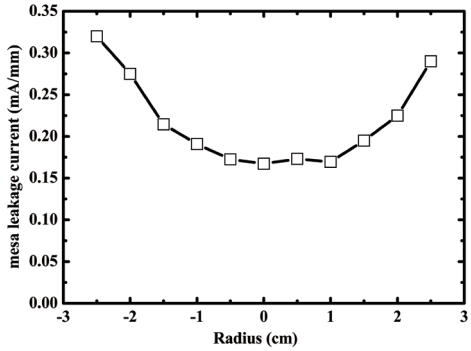

Fig. 8. The mesa leakage currents in the direction of the wafer radius.

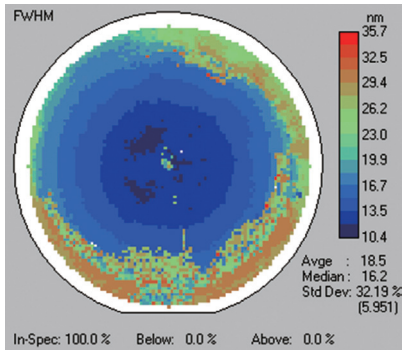

Fig. 9. The FWHM of PL.

resistance of the selective etching structure was attributed to the removal of the irregular surface oxide layers and pollutants by the etching process. On the other hand, selective etching will produce a large sidewall area, which reacts with Ti to form TiN after annealing. It will generate more N vacancies and increase the tunneling current to reduce the connect resistance.

Figure 6 compares the I-V characteristics of the three kinds of structures. The buffer breakdown voltages of conventional structures (A), whole etching structures (B), and selective etching structures (C) were extracted as 124 V, 147 V, and 171 V, respectively. The figure shows that both the selective etching and the whole etching on the ohmic area of the AlGaN layers could improve the breakdown voltages of the buffer layer, because some deep spikes could be formed under the ohmic contact regions in conventional structures, which resulted from the diffusion of metal in high-temperature annealing [6].

Under a high bias voltage, electrical field lines would gather in deep spikes and superpose into a strong electric field. Therefore, a local carrier could be injected into a GaN buffer and then drift to the peak electric-field region underneath the ohmic contact regions. The local carriers were accelerated to high energies to initiate intraband or interband impact ionization and subsequently induce buffer layer breakdown [7]. In addition, the generated deep spikes reflected the rougher surface morphology on conventional structures. In contrast, selective etching and whole etching structures had better metal surface morphology, as shown in Fig. 3. It is plausible that there were few deep spikes under ohmic contacts caused by the etching process, and the suppression of the metal spikes could reduce the high-energy electric field under the ohmic contacts; as a result, the strong electron injection from metal spikes was avoided. Therefore, the improved buffer-layer breakdown voltages were obtained. Figure 7 shows the breakdown voltages of selective etching structures and of whole etching structures with various etching times. For the selective etching structures with different times, the breakdown voltages were close. For the whole etching structures, the breakdown voltages were almost the same at different etching times. We concluded that the breakdown characteristics of buffer layers did not depend on the etching depths within a certain range.

Figure 8 shows the mesa leakage currents measured at different positions on the same wafer. As we can see in Fig. 8, at the center area of the wafer, the leakage current between mesas was about 0.16 mA/mm at 50 V, and the leakage current increased with the increase of the wafer radius. At the wafer edges, the leakage current increased to about 0.33 mA/mm. GaN heteroepitaxial growth necessarily introduces lattice defects and threading dislocations (TDs) at the wafer edges. Under a certain voltage, owing to the existence of trap centers, the electrical field lines would gather and then electron-hole pairs would be generated by impact ionization, so that the

leakage current increases suddenly. The material defects might be related to the metal spikes formed under the ohmic contact regions [9].

The density of TDs was directly reflected in the full width of half maximum (FWHM) of the photoluminescence (PL) peak, as shown in Fig. 9. The FWHM value near the center of the wafer (in blue) was below 16.7 nm, indicating less TDs in the GaN layer and a high crystalline quality with little defects. At the wafer edges, the FWHM value increased to around 30 nm, which was a greater than average FWHM value of 18.5 nm. A large FWHM indicated more TDs in the GaN layer and poor material quality. With the increase of wafer radius, the value of FWHM increased and the quality of the material deteriorated. The buffer leakage current on the wafer edges was larger than that on the center, which suggested that the generated leakage current resulted from dislocation in the material and depended on the quality of the wafer crystal [10].

4. CONCLUSIONS

The whole etching and selective etching on the ohmic electrodes area were done to investigate the buffer breakdown voltage of the AlGaN/GaN HEMT. The better ohmic metal surface morphology and higher buffer breakdown voltages were obtained by using etching preprocesses under the ohmic metal electrodes. The samples of selective etching and whole etching had better metal surface morphologies; that is, fewer deep spikes formed under the ohmic contacts, so the strong electric field focused on the metal spike was reduced. The leakage current between mesas increased with the larger wafer radius, and the PL mapping measurements indicated that more lattice defects and threading dislocations on the edge of the wafer would result in higher FWHM value; so the increment of leakage current between mesas was attributed to the increased defects and dislocations at the edges of the wafer.

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