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Neutral-point Potential Balancing Method for Switched-Inductor Z-Source Three-level Inverter

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Abstract – Switched-inductor (SL) Z-source three-level inverter is a novel high power topology. The SL based impedance network can boost the input dc voltage to a higher value than the single LC impedance network. However, as all the neutral-point-clamped (NPC) inverters, the SL Z-source three-level inverter has to balance the neutral-point (NP) potential too. The principle of the inverter is introduced and then the effects of NP potential unbalance are analyzed. A NP balancing method is proposed. Other than the methods for conventional NPC inverter without Z-source impedance network, the upper and lower shoot-through durations are corrected by the feedforward compensation factors. With the proposed method, the NP potential is balanced and the voltage boosting ability of the Z-source network is not affected obviously. Simulations are conducted to verify the proposed method.

Keywords: Switched-inductor, Z-source inverter, Voltage boosting, Neutral-point-clamped, Neutral-point potential balancing

1. Introduction

Three-level neutral-point-clamped (NPC) inverters are widely used in high voltage and high power applications due to the low voltage stress of switching devices, the low output harmonics and the low operating frequency [1-3]. However, the NPC inverters can only perform voltage step down operation, so the input dc voltage must be higher than the amplitude of the output ac line voltage, which limits its application. Voltage step up can be realized by connecting dc-dc converters to the NPC converters, which increases the cost and reduces the reliability.

Z-source inverters have drawn much research interest in recent years. The difference between the Z-source inverters and the conventional inverters is the presence of an X-shaped LC impedance network, also known as Z-source impedance network, which gives voltage boosting abilities to Z-source inverters. This impedance network can also be introduced to the three-level NPC inverter, but the voltage boosting ability is limited because of the restriction between the boost factor and the modulation index [4-6]. Switched-inductor (SL) Z-source impedance network is derived by replacing the two inductors in the traditional network with two SL cells to obtain higher voltage boost factor. Several topologies based on SL Z-source impedance network are investigated in literatures [7-9]. However, the SL Z-source three-level NPC inverter has not attracted much attention from researchers. Like any other NPC inverter, the neutral-point (NP) potential of the SL Z-source three-level inverter must be balanced. Various NP potential balancing methods were proposed for conventional NPC inverters [10-17], most of them alter redundant small vector durations so that the average neutral wire current becomes zero and thus the NP potential is balanced. In [18], a space vector modulated NP potential balancing method is proposed for Z-source three-level T-type inverter. However, it is not suitable for the SL Z-source three-level inverter.

In this paper, interest is focused on the NP potential balancing method for SL Z-source three-level inverter. Section 2 introduces the inverter topology, its voltage boosting ability and its pulse-width modulation method. Section 3 analyzes the effects of NP potential unbalance on dc-link voltage and output voltages. Section 4 describes a novel NP potential balancing method by correction of shoot-through durations. The performance of the method is evaluated through simulation, and the results are shown in Section 5.

2. Principle of Switched-inductor Z-Source Three-level Inverter

Fig. 1 shows the topology of a switched-inductor Z-source three-level NPC inverter with a Z-source impedance network connected between the two split capacitors (C_{S1} and C_{S2}) and the dc-link for voltage boosting. The Z-source network consists of two capacitors (C_1 and C_2) and two SL cells, each of which is composed of two inductors and three diodes. Assuming circuit symmetry, the voltages of the four inductors are considered as being equal ($u_{L1}=u_{L2}=u_{L3}=u_{L4}=u_L$), as well as the voltages of the two capacitors ($u_{C1}=u_{C2}=u_C$).

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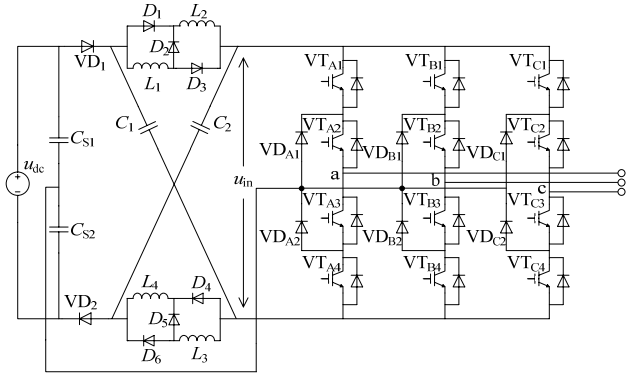
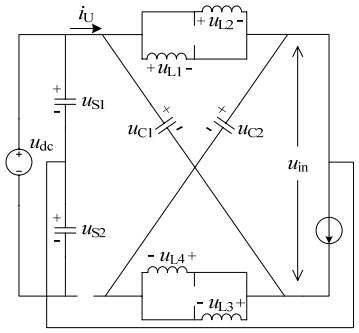
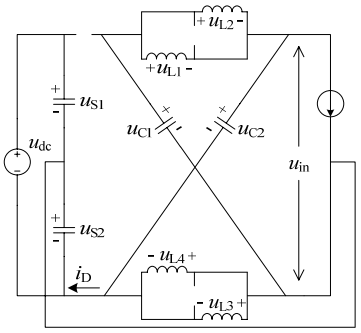


Fig. 1. Topology of a switched-inductor Z-source three-level inverter



(a) Upper shoot-through state



(b) Lower shoot-through state

Fig. 2. Equivalent circuits of the half shoot-through states

Voltage boosting within the Z-source three-level inverter is achieved by introducing half shoot-through states, which include upper shoot-through state and lower shoot-through state, to its modulation state sequence.

Fig. 2(a) shows the equivalent circuit in upper shoot-through state. Comparing with Fig. 1, we know that for phase a, switches VT_{A1}, VT_{A2} and VT_{A3} conduct, as well as diode VD_{A2}. In the Z-source impedance network, diodes VD_1, D_1, D_3, D_4, D_6 conduct, while D_2 and D_5 block. Current i_U flows to the Z-source network. Fig. 2(b) shows the equivalent circuit in lower shoot-through state. For phase a, switches VT_{A2}, VT_{A3}, VT_{A4} and diode VD_{A1} conduct. In the impedance network, diodes VD_2, D_1, D_3, D_4, D_6 conduct, while D_2 and D_5 block. Current i_D flows from the

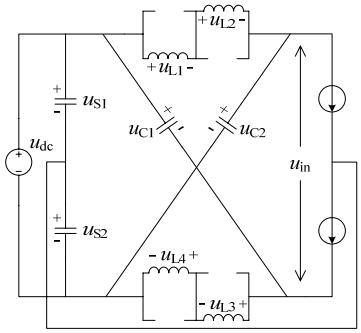


Fig. 3. Equivalent circuits of the non-shoot-through state

Z-source network. The voltage equations in both states are

$$\begin{cases} u_{\mathrm{L}} = u_{\mathrm{dc}} / 2 \\ u_{\mathrm{inH}} = u_{\mathrm{C}} - u_{\mathrm{L}} \end{cases} \tag{1}$$

where u_{inH} is the dc link high peak voltage, and u_{dc} is the dc supply voltage. The upper shoot-through and the lower shoot-through have equal durations.

Fig. 3 shows the equivalent circuit in non-shoot-through state. In this case, diodes VD_1, VD_2, D_2 and D_5 conduct, while diodes D_1, D_3, D_4 and D_6 block. The voltage equations are

$$\begin{cases} 2u_{\mathrm{L}} + u_{\mathrm{C}} = u_{\mathrm{dc}} \\ u_{\mathrm{inH}} = u_{\mathrm{C}} - 2u_{\mathrm{L}} \end{cases} \tag{2}$$

Because the inductor voltage-second balance in steady state, the capacitor voltage is derived from (1) and (2) as

$$u_{\mathrm{C}} = \frac{u_{\mathrm{dc}}}{1-2d_{\mathrm{s}}} \tag{3}$$

where d_{s} is the duty cycle of the upper shoot-through as well as the lower shoot-though.

From (2) and (3), the dc link high peak voltage is deduced as

$$u_{\mathrm{inH}} = 2u_{\mathrm{C}} - u_{\mathrm{dc}} = \frac{1+2d_{\mathrm{s}}}{1-2d_{\mathrm{s}}} u_{\mathrm{dc}} = Bu_{\mathrm{dc}} \tag{4}$$

where B is known as boost factor.

Fig. 4 plots relationships between the shoot-through duty cycle and the boost factor for the conventional Z-source three-level inverter and the SL Z-source three-level inverter. As shown in the figure, the boost factor of the SL type inverter is much higher than that of the conventional inverter.

The SL cells can be cascaded to further increase the boost factor. Now a SL cell consists of one inductor L_i and three diodes D_{i1}, D_{i2} and D_{i3} for the ith cell, as shown in Fig. 5(a). The SL cells are connected as in Fig. 5(b) for the upper bus. Note that inductor L_{n+1} is not included in the SL cells. For the lower bus, the SL cells are numbered from $n+2$ to $2n+2$.

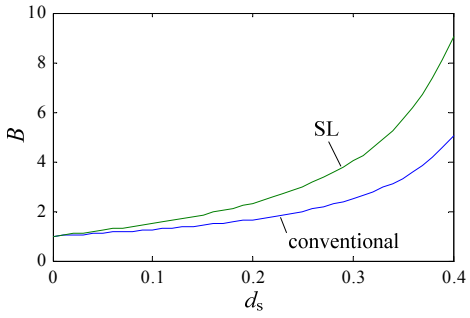
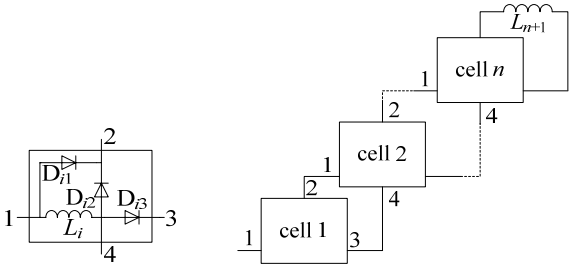


Fig. 4. Comparison of voltage boosting ability of the SL topology and the conventional topology



(a) SL cell (b) Connection of the SL cells

Fig. 5. Multicell SL

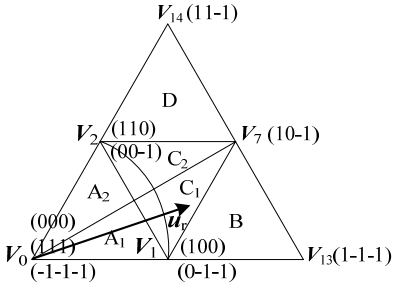


Fig. 6. Division of sector S_1

Similarly, the dc-link high peak voltage is deduced as

$$u_{\text{inH}} = \frac{1+2nd_s}{1-2d_s}u_{\text{dc}} = Bu_{\text{dc}} \tag{5}$$

The boost factor increases with total SL cells number $2n$. However, n cannot be too large because the voltage stress of capacitors C_1 and C_2 will be too high.

SL and multicell SL Z-source three-level inverters use same space vector pulse width modulation (SVPWM) method derived from the modulation method for traditional three-level NPC inverter. Fig. 6 illustrates the division of sector S_1, which is divided into five triangles. The reference vector $\boldsymbol{u}_\mathbf{r}$ is synthesized by its nearest three vectors. For example, if $\boldsymbol{u}_\mathbf{r}$ is located inside triangle C_1 in a certain switching period, it can be synthesized by vectors $\boldsymbol{V}_1$, $\boldsymbol{V}_2$ and $\boldsymbol{V}_7$.

Fig. 7 shows the PWM state sequences in triangle C_1 of a conventional three-level inverter and a Z-source three-level inverter, where two equal-interval shoot-through states (marked as ① and ② in the figure) are inserted at the two state transitions of {100} → {10–1} → {0–1–1} in the first half switching period, and the two half periods are symmetrical. The duration of {10–1} is t_0, so the time remaining in a switching period is T_s–t_0. The lower shoot-through state can be inserted during the {100} interval of conventional three-level inverter, while the upper shoot-through state can be inserted during the {00–1} interval and the {0–1–1} interval of the traditional three-level inverter to achieve as much duration time for shoot-through as possible. In half a switching period, the {100} interval is set equal to the sum of the {00–1} interval and the {0–1–1} interval, that is $(T_s–t_0)/4$. Thus, the durations available for insertion of the lower shoot-through vector and the upper shoot-through vector are identical.

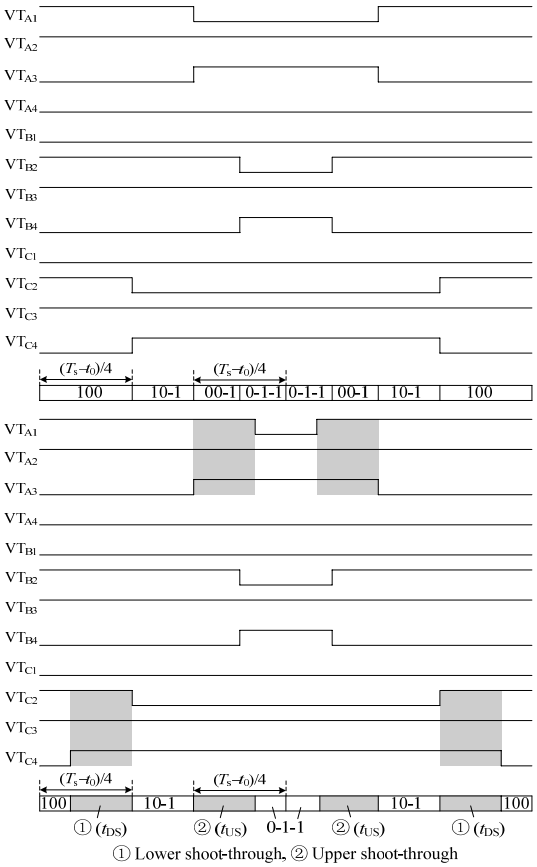


Fig. 7. Modulation of conventional and SL Z-source NPC inverters

3. Effects of Neutral-point Potential Unbalance

The voltages of the split capacitors are u_{S1} and u_{S2} respectively. In the case of unbalance, the two voltages are $u_{S1} = u_{dc}/2 + \Delta U$ and $u_{S2} = u_{dc}/2 - \Delta U$, where ΔU is the voltage deviation from $u_{dc}/2$. The KVL equations in unbalanced condition are rewritten as follows:

1) Upper shoot-through:

$$\begin{cases} u_{\mathrm{L}} = u_{\mathrm{dc}} / 2 + \Delta U \\ u_{\mathrm{inL1}} = u_{\mathrm{C}} - u_{\mathrm{L}} = u_{\mathrm{C}} - u_{\mathrm{dc}} / 2 - \Delta U \end{cases} \tag{6}$$

2) Lower shoot-through:

$$\begin{cases} u_{\mathrm{L}} = u_{\mathrm{dc}} / 2 - \Delta U \\ u_{\mathrm{inL2}} = u_{\mathrm{C}} - u_{\mathrm{L}} = u_{\mathrm{C}} - u_{\mathrm{dc}} / 2 + \Delta U \end{cases} \tag{7}$$

3) Non-shoot-through:

$$\begin{cases} (n+1)u_{\mathrm{L}} + u_{\mathrm{C}} = u_{\mathrm{dc}} \\ u_{\mathrm{inH}} = u_{\mathrm{C}} - (n+1)u_{\mathrm{L}} \end{cases} \tag{8}$$

The average voltage of the inductors should be zero over one switching period, thus from (6)~(8), the voltage of the Z-source network capacitor is deduced as

$$u_{\mathrm{C}} = \frac{1 + (n-1)d_{\mathrm{S}}}{1 - 2d_{\mathrm{S}}} u_{\mathrm{dc}} \tag{9}$$

The output phase to neutral-point voltages of the inverter can be expressed as

$$\begin{cases} U_{\mathrm{io+}} = u_{\mathrm{dc}} / 2 + \Delta U - (n+1)u_{\mathrm{L}} = u_{\mathrm{inH}} / 2 + \Delta U \\ U_{\mathrm{io-}} = u_{\mathrm{dc}} / 2 - \Delta U - (n+1)u_{\mathrm{L}} = u_{\mathrm{inH}} / 2 - \Delta U \end{cases} i\text{=a, b, c} \tag{10}$$

which indicate that the NP potential unbalance causes the phase to neutral-point offset voltages to occur. The dc-link high peak voltage increases with the voltage boost factor, while the offset becomes less obvious.

4. Neutral-point Potential Balancing Method Based on Correction of Shoot-through Durations

4.1 NP potential balancing method for SL Z-source three-level inverter

The NP potential balancing method for conventional three-level NPC inverter is reviewed briefly at first. The method utilizes the redundancy of the small vectors. The positive and negative small vectors come in pairs in a switching period. As an example, the redundant vector of {100} is {0–1–1}, as shown in Fig. 6. The durations of the positive and negative small vectors in half a switching period are t_{p} and t_{n} respectively, which are equal without considering the NP potential balancing, i.e., t_{p}=t_{n}. A balancing control factor k is introduced to correct t_{p} and t_{n}. The durations after correction would be

$$\begin{cases} t_{\mathrm{p}}^{'} = \dfrac{1+k}{2} t_{\mathrm{p}} \\ t_{\mathrm{n}}^{'} = \dfrac{1-k}{2} t_{\mathrm{p}} \end{cases} \tag{11}$$

In order to balance the NP potential, the total injected charge to the neutral-point is set to zero. Thus the balancing control factor is deduced as

$$k = \frac{-C_{\mathrm{S}}(u_{\mathrm{S1}} - u_{\mathrm{S2}}) - i_{\mathrm{o1}} t_1 - i_{\mathrm{o2}} t_2}{i_{\mathrm{op}} t_{\mathrm{p}}} \tag{12}$$

where i_{o1} and i_{o2} are the neutral currents when the other two vectors are applied, t_1 and t_2 are the durations of the other two vectors in half a switching period, i_{op} is the neutral current when the positive small vector is applied. The split capacitor voltages can be balanced by using (11) and (12) to correct the durations of the positive and negative small vectors.

Next, the effects of shoot-through on average neutral current for SL Z-source three-level inverter are analyzed. As an example, it is still assumed that $\boldsymbol{u}_{\mathbf{r}}$ is located in triangle C_1. There are two cases: low boost factor and high boost factor. Using Fig. 7 for reference, in the first case, the upper shoot-through state is inserted only within {00–1}. The average neutral current is expressed as

$$\begin{aligned} \overline{i_{\mathrm{o}}} &= (d_{\mathrm{1P}} - d_{\mathrm{S}})(i_{\mathrm{b}} + i_{\mathrm{c}}) + d_7 i_{\mathrm{b}} + (d_{\mathrm{2N}} - d_{\mathrm{S}})(i_{\mathrm{a}} + i_{\mathrm{b}}) + d_{\mathrm{1N}} i_{\mathrm{a}} \\ &\quad + [i_{\mathrm{a}} + i_{\mathrm{b}} - (n+1)(i_{\mathrm{L1}} + i_{\mathrm{L2}})] d_{\mathrm{S}} \\ &\quad + [(n+1)(i_{\mathrm{L1}} + i_{\mathrm{L2}}) + i_{\mathrm{b}} + i_{\mathrm{c}}] d_{\mathrm{S}} \\ &= d_{\mathrm{1P}}(i_{\mathrm{b}} + i_{\mathrm{c}}) + d_7 i_{\mathrm{b}} + d_{\mathrm{2N}}(i_{\mathrm{a}} + i_{\mathrm{b}}) + d_{\mathrm{1N}} i_{\mathrm{a}} \end{aligned} \tag{13}$$

where d_{1P}, d_7, d_{2N} and d_{1N} are the duty cycles of vectors {100}, {10–1}, {00–1} and {0–1–1} respectively; i_{L1} and i_{L2} are the upper and lower inductor currents respectively; i_{a}, i_{b} and i_{c} are the three phase inverter output currents.

In the second case, the upper shoot-through state is inserted within both {00–1} and {0–1–1}. The average neutral current is written as

$$\begin{aligned} \overline{i_{\mathrm{o}}} &= (d_{\mathrm{1P}} - d_{\mathrm{S}})(i_{\mathrm{b}} + i_{\mathrm{c}}) + d_7 i_{\mathrm{b}} + (d_{\mathrm{1N}} + d_{\mathrm{2N}} - d_{\mathrm{S}}) i_{\mathrm{a}} \\ &\quad + [i_{\mathrm{a}} + i_{\mathrm{b}} - (n+1)(i_{\mathrm{L1}} + i_{\mathrm{L2}})] d_{\mathrm{2N}} \\ &\quad + [(n+1)(i_{\mathrm{L1}} + i_{\mathrm{L2}}) + i_{\mathrm{b}} + i_{\mathrm{c}}] d_{\mathrm{S}} \\ &\quad + [i_{\mathrm{a}} - (n+1)(i_{\mathrm{L1}} + i_{\mathrm{L2}})](d_{\mathrm{S}} - d_{\mathrm{2N}}) \\ &= d_{\mathrm{1P}}(i_{\mathrm{b}} + i_{\mathrm{c}}) + d_7 i_{\mathrm{b}} + d_{\mathrm{2N}}(i_{\mathrm{a}} + i_{\mathrm{b}}) + d_{\mathrm{1N}} i_{\mathrm{a}} \end{aligned} \tag{14}$$

From (13) and (14), we know that the shoot-through states do not affect the average neutral current if the upper and lower shoot-through states have equal durations in a switching period. Same conclusions can be drawn when $\boldsymbol{u}_{\mathbf{r}}$ is located in other triangles. Therefore, the NP potential can be balanced if the average neutral current is adjusted to zero during the non-shoot-through intervals. It seems that the principle of the NP potential balancing for a SL Z-source three-level inverter is similar to that of a conventional three-level NPC inverter. However, as previously mentioned, the time duration available for shoot-through vector insertion is $(T_{\mathrm{s}}–t_0)/4$, which varies with the rotation of the reference voltage vector $\boldsymbol{u}_{\mathbf{r}}$ and its

minimum value equals the shoot-through duration. When $(T_s-t_0)/4$ reaches the minimum, the durations of the positive and negative small vectors equal zero and cannot be adjusted. Consequently, the NP potential balancing method for conventional three-level NPC inverter is not applicable to the SL Z-source three-level inverter.

This paper utilizes shoot-through vectors instead of redundant small vectors to stabilize the split capacitor voltages. The designing methodology is based on the charging and discharging processes of the split capacitors during the shoot-through states. From Fig. 2, it can be seen that in upper shoot-through state, the upper split capacitor discharges and u_{S1} decreases, the lower split capacitor charges and u_{S2} increases, and $u_{S1}+u_{S2}$ always equals to u_{dc}. As a result, ΔU decreases. Similarly, the lower split capacitor discharges and the upper split capacitor charges in lower shoot-through state, so u_{S2} decreases and u_{S1} increases, which makes ΔU increases. As mentioned before, without considering NP potential balancing, the upper shoot-through duration t_{US} equals the lower shoot-through duration t_{DS}. But in the proposed method, they can be corrected to balance the NP potential. If $u_{S1}>u_{S2}$, reduce t_{US} and do not correct t_{DS}. Instead, if $u_{S1}<u_{S2}$, reduce t_{DS} and do not change t_{US}. Based on this idea, define feedforward compensation factors as

$$\begin{cases} k_u = 1+\dfrac{\mathrm{sgn}(\Delta U)-1}{2}k_p|\Delta U| \\ k_d = 1-\dfrac{\mathrm{sgn}(\Delta U)+1}{2}k_p|\Delta U| \end{cases} \tag{15}$$

where $\mathrm{sgn}(x)$ is the sign function, $\mathrm{sgn}(x)=1$ with $x>0$, $\mathrm{sgn}(x)=0$ with $x=0$ and $\mathrm{sgn}(x)=-1$ with $x<0$, k_p is a proportional coefficient greater than zero. Therefore, from (15), we know that $k_u\le 1$ and $k_d\le 1$. The value of the two feedforward compensation factors cannot be too small to guarantee the voltage boosting ability of the inverter. So amplitude limiting is used to the two factors:

$$\begin{cases} k_u = k_{umin} & \text{if } k_u < k_{umin} \\ k_d = k_{dmin} & \text{if } k_d < k_{dmin} \end{cases} \tag{16}$$

where k_{umin} and k_{dmin} are the minimum values of k_u and k_d respectively.

After correction, the upper and lower shoot-through durations are

$$t_{US}^{'} = k_u t_{US}, \quad t_{DS}^{'} = k_d t_{DS} \tag{17}$$

If $u_{S1}-u_{S2}=2\Delta U>0$, from (15) we know that $k_u=1$ and $k_d=1-k_p|\Delta U|<1$, so $t_{US}^{'} < t_{DS}^{'}$ and ΔU decreases. On the contrary, if $u_{S1}-u_{S2}=2\Delta U<0$, we have $k_u=1-k_p|\Delta U|<1$ and $k_d=1$, thus $t_{US}^{'} > t_{DS}^{'}$ and therefore ΔU increases. With the adjustment of k_u and k_d, the difference between the split capacitor voltages will approach zero eventually. Thus the NP potential is balanced.

4.2 The effect of NP potential balancing on inverter output voltage

Due to the operation of NP potential balancing control, the durations of the upper and lower shoot-through are not equal. Set $k_u<1$ and $k_d=1$ for simplification purpose, the volt-second balance equation of any of the inductors is written as

$$\begin{aligned} &\frac{(u_{dc}-u_C)}{n+1}[1-(1+k_u)d_S]+ \\ &(u_{dc}/2+\Delta U)k_u d_S+(u_{dc}/2-\Delta U)d_S=0 \end{aligned} \tag{18}$$

The Z-source network capacitor voltage is deduced as

$$u_C = \frac{\left[1+\dfrac{n-3+(n+1)k_u}{2}d_S\right]u_{dc}+(1-k_u)(n+1)d_S\Delta U}{1-(1+k_u)d_S} \tag{19}$$

The dc-link high peak voltage is further derived as

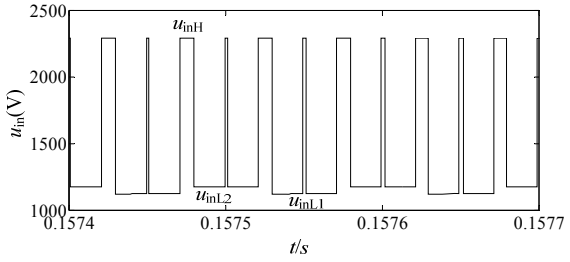
$$u_{inH} = \frac{1+[n-2+(n+2)k_u]d_S}{1-(1+k_u)d_S}u_{dc}+\frac{2(1-k_u)(n+1)d_S\Delta U}{1-(1+k_u)d_S} \tag{20}$$

The second item in (20) is much smaller than the first item, therefore it can be ignored. The voltage boost factor decreases compare with the ideal operation in which the split capacitor voltages are fixed and their values are equal. Generally, the inverter operates with the help of a closed-loop controller to regulate its output voltages, which can compensate the slight drop of the dc-link high peak voltage. Therefore, the impact of the proposed NP potential balancing method on inverter output voltage can be neglected.

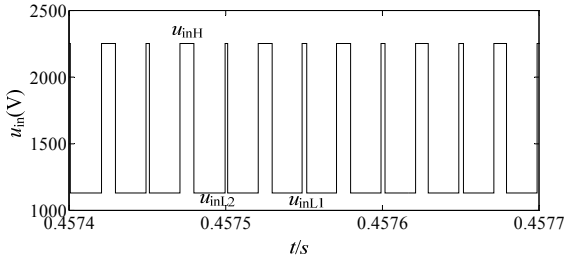
5. Simulation Studies

The proposed NP potential balancing method for SL Z-source three-level inverter is verified under MATLAB/ Simulink environment. The dc side voltage is u_{dc}=200V. The capacitance of the split capacitors is 2200μF. The initial voltages u_{S1} and u_{S2} are 130V and 70V respectively, so ΔU=30V. The capacitance of the Z-source network capacitors C_1 and C_2 is 800μF. The number of the switched-inductor cells is $2n$=4. The inductance of the six inductors (L_1, L_2, L_3 for upper cells and L_4, L_5, L_6 for lower cells) is 1.2mH. The switching frequency f_s of the inverter is 10kHz. The boost factor B is 11.4.

Fig. 8 shows the dc-link voltage waveforms in steady

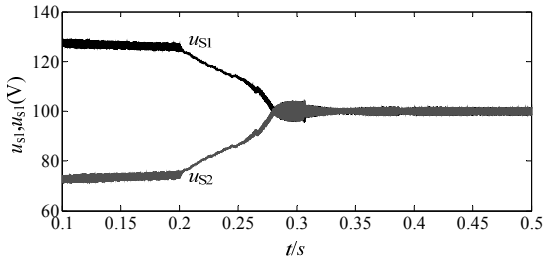


(a) Without NP potential balancing

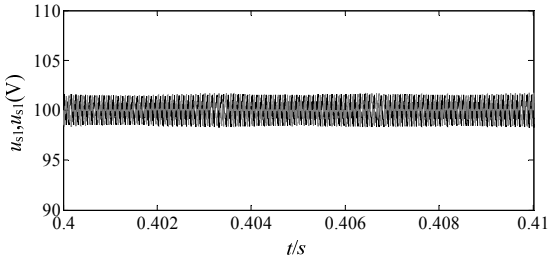


(b) With NP potential balancing

Fig. 8. Waveforms of the dc-link voltage in steady state



(a) Before and after the operation of NP potential balancing control



(b) Magnification after balancing

Fig. 9. Waveforms of the split capacitor voltages

and transient states. As seen from Fig. 8(a), without the operation of NP potential balancing, the dc-link high peak voltage u_{inH} has the same value as in ideal case (u_{inH}= Bu_{dc}=11.4×200=2280V), while the low peak voltage u_{inL1} in upper shoot-through state is about 60V less than the low peak voltage u_{inL2} in lower shoot-through state. The voltage difference equals to 2ΔU. The dc-link voltage with the operation of NP potential balancing is shown in Fig. 8(b), where the low peak voltages u_{inL1} and u_{inL2} are equal. The phase to neutral-point offset voltage decreases to zero.

The waveforms of split capacitor voltages are shown

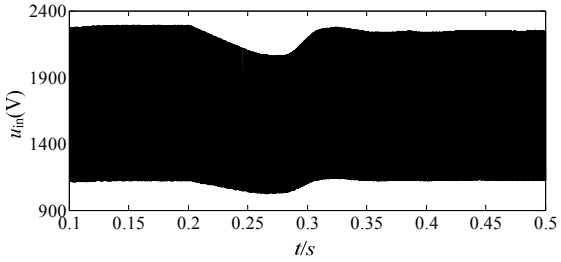


Fig. 10. Waveform of the dc-link voltage in transient state

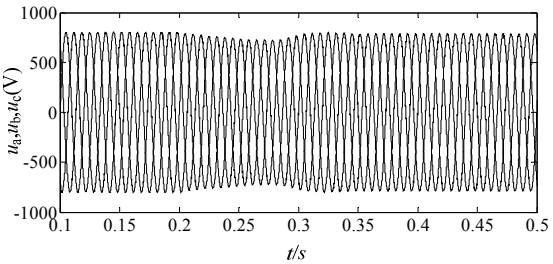


Fig. 11. Three-phase output voltages of the inverter

in Fig. 9. As seen in Fig. 9(a), the split capacitor voltages keep unbalance before 0.2s, while the proposed NP potential balancing method begins to operate at 0.2s, u_{S1} deceases rapidly and u_{S2} increases quickly, and they become equal from about 0.28s. The waveforms after magnification is shown in Fig. 9(b), where small ripples exist in the two voltages, but their amplitudes are less than 2V. The proposed method obtains good steady effect.

The transient state dc-link voltage is shown in Fig. 10. After 0.2s, both the high peak voltage and the low peak voltage fluctuate and recover to stable at about 0.34s. In addition, the dc-link high peak voltage is slightly smaller than it is before 0.2s due to the introduction of the feedforward compensation factors k_u and k_d.

The three-phase inverter output voltages are shown in Fig. 11. As the dc-link voltage, the output voltages also undergo transient processes. The voltage amplitudes become stable again at about 0.32s. Although open-loop control is adopted in the simulation, the steady state amplitudes almost keep unchanged with the proposed NP potential balancing method.

6. Conclusion

In this paper, a neutral-point potential balancing method for switched-inductor Z-source three-level inverter is proposed. This inverter outputs higher voltage than the Z-source three-level inverter and the three-level NPC inverter, but the conventional neutral-point potential balancing method for three-level NPC inverter is not apply to it. The upper and lower shoot-through durations are corrected by the feedforward compensation factors. With the proposed method, the NP potential is balanced

and the voltage boosting ability of the Z-source network is not affected obviously. Simulation results are provided to verify the effectiveness of the proposed method.

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