JOURNAL OF SEMICONDUCTOR TECHNOLOGY AND SCIENCE, VOL.17, NO.2, APRIL, 2017
https://doi.org/10.5573/JSTS.2017.17.2.302
ISSN(Print) 1598-1657
ISSN(Online) 2233-4866

Novel Pass-transistor Logic based Ultralow Power Variation Resilient CMOS Full Adder

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Abstract—**This paper proposes a new full adder design based on pass-transistor logic that offers ultra-low power dissipation and superior variability together with low transistor count. The pass-transistor logic allows device count reduction through direct logic realization, and thus leads to reduction in the node capacitances as well as short-circuit currents due to the absence of supply rails. Optimum transistor sizing alleviates the adverse effects of process variations on performance metrics. The design is subjected to a comparative analysis against existing designs based on Monte Carlo simulations in a SPICE environment, using the 22-nm CMOS Predictive Technology Model (PTM). The proposed ULP adder offers 38% improvement in power in comparison to the best performing conventional designs. The trade-off in delay to achieve this power saving is estimated through the power-delay product (PDP), which is found to be competitive to conventional values. It also offers upto 79% improvement in variability in comparison to conventional designs, and provides suitable scalability in supply voltage to meet future demands of energy-efficiency in portable applications.**

Index Terms—**Full adder, pass-transistor logic (PTL), power-delay product (PDP), ultralow power (ULP), variability**

Manuscript received Apr. 13, 2016; accepted Nov. 23, 2016
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I. INTRODUCTION

There has been a major paradigm shift in the industry today as the need for lower power dissipation has become a critical parameter in face of other considerations such as performance, area, cost and reliability for a VLSI designer. The primary driving force towards this shift has been the extensive growth of mobile and portable computing devices as well as wireless communications systems which demand high-speed computation while keeping power consumption low [1]. The increased levels of integration today allow the designer to use the vacated area for extra circuits to compensate for the device speed reduction due to lower supply voltages [2-4].

This generation of devices demand advanced processors that accomplish this need. A full adder is one of the most critical components of a processor which determines its throughput as it is used in the ALU, the floating-point unit, and for address generation in case of cache or memory access [5-11].

Power dissipation in CMOS circuits is caused by three main sources: 1) leakage current, consisting of reverse bias current in the parasitic diodes as well as the sub-threshold current from the inversion charge, 2) the short-circuit current due to the DC path between the supply rails during output transitions, and 3) the charging and discharging of load capacitances during logic changes. The total power is estimated by the following equation [2, 12]:

$$P = \sum_i V_{DD} V_{sw} C_l f P_i + V_{DD} \sum_i I_{sc} + V_{DD} I_l \qquad (1)$$

where V_{DD} is the supply voltage, V_{sw} is the voltage swing of the output, C_l is the output load capacitance at node i, f is the system clock frequency, P_i is the switching activity at node i, I_{sc} is the short circuit current at node i, and I_l is the leakage current. The summation is over all the nodes of the circuit. A reduction in any of the appropriate components in the above equation will thus reduce power consumption [5].

As CMOS technology continues to scale down, significant variations occur in process, voltage, and temperature (PVT) parameters which affect circuit response, performance, and reliability of such circuits [13, 14]. Critical sources of process variations are random dopant fluctuation (RDF), short-channel effect (SCE), drain-induced barrier lowering (DIBL), line edge roughness (LER), line width roughness (LWR), interface roughness, etc. Variability has thus become a metric of equal importance to power, delay, and area under modern processes in sub-100-nm integrated circuits [15].

Pass Transistor Logic (PTL) is known to reduce the overall transistor count by directly using transistors to pass logic levels and thus eliminating redundant transistors. This makes it suitable to implement power reduction techniques. Switching activity in the circuit can be improved by controlling the delays of each pass transistor through suitable sizing, effectively reducing the switching node capacitances. There are fewer connections between supply rails, so that they draw the least amount of short circuit power. However, this comes with a disadvantage of threshold voltage drop, requiring restoration of output levels in order to maintain full swing outputs and to avoid static currents [16, 17].

In this paper, we propose a new ultralow power (ULP) full adder design based on PTL, designed to eliminate excessive power dissipation at ultralow supply voltages through both the internal node capacitances as well as short circuit currents. It also maintains an adequate trade-off in power-delay product (PDP) in comparison to existing conventional designs, and retains its performance throughout the temperature range.Superior results in terms of variability of performance metrics are also obtained, with suitable scalability of supply voltage.

The rest of this paper is organized as follows. Section II describes basic features of the various existing full adder topologies analyzed in this paper. The three modules composing the proposed full adder are analyzed in Section III. Section IV describes the proposed ULP adder design and its characteristics, and Section V evaluates the performance of the design in terms of power, delay and PDP through a comparative analysis. It also contains detailed analyses in terms of temperature, variability, and voltage scalability. Section VI finally concludes the paper, outlining its contributions.

II. EXISTING FULL ADDER DESIGNS

In recent times, several full adder (FA) designs with low transistor counts (8-12) have been proposed in literature with the aim of reducing area and power. These include the 8T, 10T [18], SERF [5], CLRCL [19], and 12T [20] adders, among many others. However, when simulated in the required ultralow power regime, these circuits fail to give satisfactory output swings, leading to erroneous logic levels. Thus these designs are rendered unusable under the required conditions, and the power and area improvements offered by them become redundant.

In comparison, some conventional as well as non-conventional FA topologies with higher transistor counts were observed to offer full swing outputs and reliable waveforms under the same conditions. However they have huge area costs associated with them. The best performing circuits among the same are chosen for a comparative analysis in this paper and are briefly described below.The Static CMOS FA shown in Fig. 1(a) uses a simple implementation of the adder logic [21].

The major drawback of this design is its large transistor count (28T) and existence of the slower PMOS block. The Mirror FA [11] is derived from the Static CMOS by directly connecting the series PMOS transistors to the supply both in the carry and sum circuits to mirror the NMOS transistor network. The adder is shown in Fig. 1(b).

The Complementary Pass-transistor Logic (CPL) FA has differential inputs and outputs and has an NMOS pass-transistor network with cross-coupled PMOS transistors (Fig 1(c)) [12]. This topology has large power dissipation due to the presence of a lot of internal nodes and static inverters. The Hybrid FA shown in Fig. 1(d) proposed in [22] uses a XOR-XNOR circuit that generates full swing outputs simultaneously. The design was reported to be energy efficient, without significant

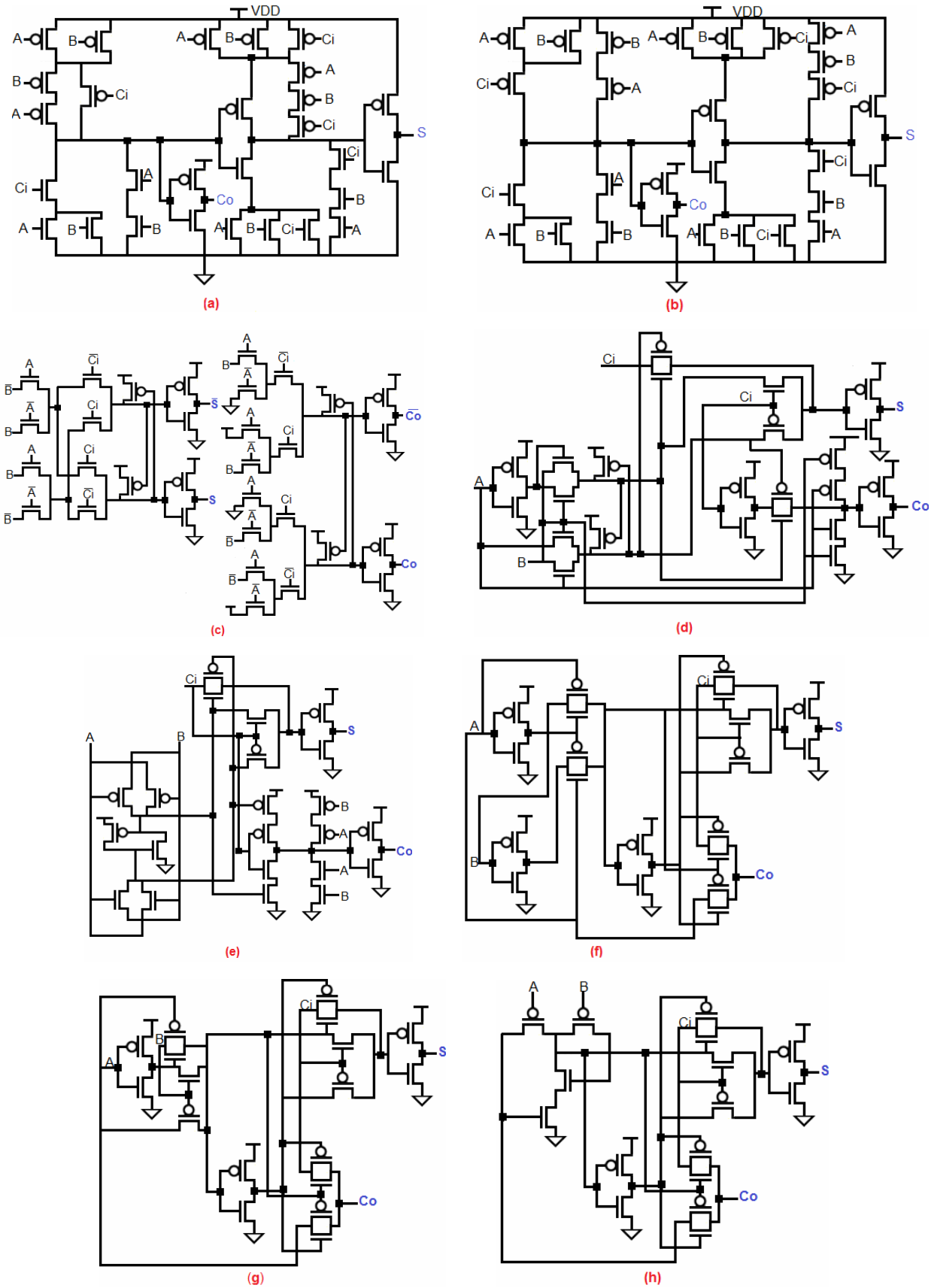


Fig. 1. Full adder topologies analyzed (a) Static CMOS, (b) Mirror, (c) CPL, (d) Hybrid, (e) HPSC, (f) Cell 3, (g) Cell 8, (h) Cell 11 adders.

loss in driving capability.

In the Hybrid Pass logic with Static CMOS (HPSC) adder (Fig. 1(e)), PTL style has been used to efficiently generate the XOR and XNOR functions simultaneously and a carry out with good drivability has been generated by a novel complementary CMOS style [23]. A number of low power full adder designs were proposed in [6] using a modular approach for various components. FA Cells 3 (Fig. 1(f)), 8 (Fig. 1(g)) and 11 (Fig. 1(h)) in the original paper are selected as the best choices for the given conditions.

III. Analysis of Full Adder Modules

The standard full adder logic equations can be expressed in a number of ways for different implementations. Assuming S is the full adder sum, C_i and C_o are the input and output carry signals respectively, A is one of the full adder inputs, H is the half sum $(A \oplus B)$ and H' is complement of H [23], a conventional implementation takes the form:

$$S = H \oplus C_i \tag{2}$$

$$C_o = A \cdot H' + C_i \cdot H \tag{3}$$

The design can thus be broken down into 3 distinct modules. We now analyze each of these stages separately and optimize various design choices to achieve best results. The module choices offering superior characteristics in terms of PDP are chosen to form the proposed ULP adder.

1. Design Options for Modules I, II and III

The first module generates the H and H' signals either by a XOR circuit followed by an inverter, or by generating both signals simultaneously through a XOR-XNOR circuit. Fig. 2 shows three different choices, I(a)-I(c) corresponding to Fig. 2(a)-(c) respectively, is using either 5 or 6 transistors. Designs with higher number of transistors are not chosen since they are not expected to provide competitive results for the required ULP design with area constraints in mind.

Module I(a) is the 6T XOR-XNOR circuit described in [25] which generates simultaneous H and H' signals using a feedback connection between XOR and XNOR

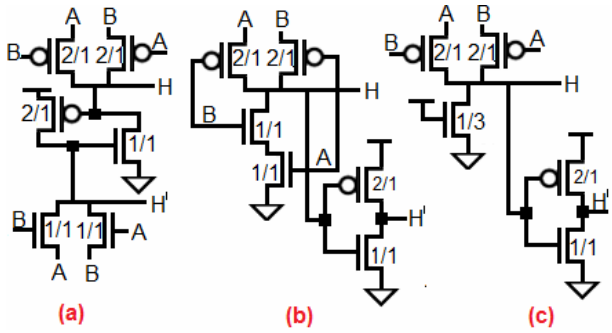


Fig. 2. Design choices for Module I.

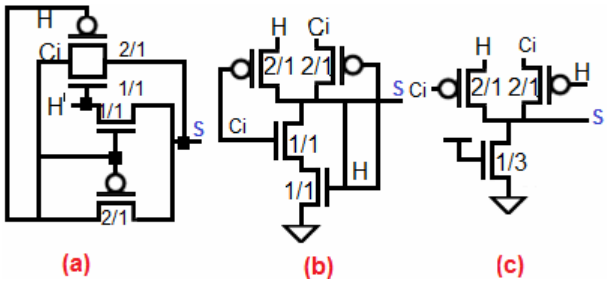


Fig. 3. Design choices for Module II.

outputs to eliminate the non-full-swing operation. Module I(b) uses the 4T XOR circuit proposed in [26] followed by an inverter to produce H'. Module I(c) is a proposed design based on the individual 3T XOR circuit in [27]. The original circuit does not provide good output levels for transitions to the '00' input state due to the poor low level transmitted by either pMOS, where the nMOS also remains in the OFF state. Instead, the nMOS is implemented as a permanent level restorer in the form of PTL by supplying a constant high level at its gate in the form of V_{DD}. The transistor is sized appropriately so that it does not interfere with the outputs during other transitions, as described in the next subsection.

Module II is a XOR circuit generating the S output. Fig. 3(a)-(c) show three choices for Module II. Module II(a) is a conventional transmission function (TF) based 4T XOR circuit [15], which requires both H and H' signals. Modules II(b) and (c) correspond to the XOR circuit implementations in Modules I(b) and (c) respectively, without an added inverter.

Module III is a 2:1 multiplexer generating the C_o output. Fig. 4 shows the proposed circuit for this module implemented in PTL.The logic function in (3) is applied to pMOS transistors using H and H' as the control inputs, followed by a level restoring nMOS transistor similar to those in Modules I(c) and II(c).

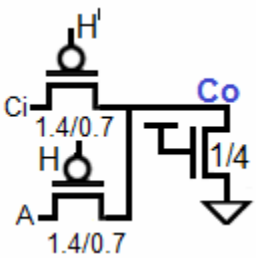


Fig. 4. Proposed design for Module III.

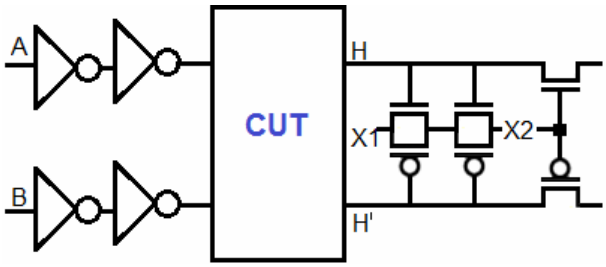


Fig. 5. Input and output loading for analysis of Module I.

This enables a minimum-transistor implementation capable of full-swing outputs as well as driving capability due to the level restoration. Other options for this module include the 4T TG based multiplexer commonly used in full adder designs [22, 24] and the 2T multiplexer implemented in designs with less transistors [18-20]. The former does not have adequate driving capabilities due to directly coupled inputs and outputs [21, 22], while the latter does not give adequate full swing outputs under the given conditions. Thus the proposed circuit is selected as the only choice for this module.

2. Transistor Sizing

All transistors in the sub-circuits described above are sized iteratively to yield optimized results. The transistors are first set to minimum sizes, and input patterns are applied to them with all possible transitions. The waveforms are observed and the transistors causing any incomplete swings are appropriately sized. The iteration is continued until the best outputs swings are obtained.

Next, following the iterative method in [24], the highest delay in the output waveform is observed, and the appropriate transistors are sized, while conserving the shape of the waveforms. In this way, all transistors are optimized for minimum power-delay product (PDP). Fig. 2-4 report the sized transistor dimensions in the form of multipliers to width W = 44 nm and length L = 22 nm, chosen according to the 22-nm technology implemented.

3. Simulation Test Bench

The propagation delay is not only a function of the circuit technology and topology, but also is a function of the slope of the input signal of a circuit. Since the delay of a circuit depends on the input slope, we passed signals A, B, and C_i through buffers (two cascaded inverters) to obtain a realistic input slope (for example see Fig. 5, where module I is analyzed with input signals A and B). While doing so we observed that the rise time of the outputs of buffers (i.e., the inputs of CUT in Fig. 5) is ≈ 10% of the pulse width of the signals A and B, whose frequency was taken to be 1 MHz and which was simulated at 0.4 V. Our choice of rise time to be 10% of the pulse width aligns with the choices of authors in [27-30].

Module I is analyzed first, by appropriately loading its outputs H and H'.The average load is calculated from the designsused for Modules II and III, found to be an average of 2 gates and 1 source/drain.The circuit under test (CUT) is thus connected appropriately to represent an equivalent load, as shown in Fig. 5 and its characteristics are analyzed.

Modules II and III are then analyzed using actual inputs from the selected design for Module I offering best results. The S output is loaded by similar buffers, while the C_o is cascaded into the input of an identical adder.

4. Simulation Results

Power, delay and PDP values for Modules I, II and III are reported in Tables 1-3 respectively. Module I(c) is seen to provide superior values for all 3 design metrics. Removing one of the series nMOS transistors in I(b) leads to lesser number of internal nodes, and thus reduced average power dissipation, while design I(a) faces the worst power dissipation due to an even greater number of internal nodes leading to larger capacitive dissipation. Further, although it is expected that the simultaneous generation of H and H' in I(a) should lead to improved delay, the feedback loop between XOR and

Table 1. Simulation Results for Module I

Design	Device Count	Power (10^{-11} W)	Delay (10^{-6} s)	PDP (10^{-17}Ws)
I(a)	6	2.169	1.173	2.545
I(b)	6	1.980	1.168	2.313
I(c)	5	1.556	1.166	1.814

Table 2. Simulation Results for Module II

Design	Device Count	Power (10^{-12} W)	Delay (10^{-7} s)	PDP (10^{-19}Ws)
II(a)	4	1.773	4.930	8. 740
II(b)	4	1.765	4.943	8. 724
II(c)	3	2.163	5.026	10.871

Table 3. Simulation Results for Module III

Design	Device Count	Power (10^{-12} W)	Delay (10^{-7} s)	PDP (10^{-18}Ws)
III	3	2.163	5.026	1.087

XNOR circuits causes greater delay than the other designs. Thus, I(c) exhibit the best overall PDP value.

In Module II, even though II(b) provides the best PDP value, it is observed that the XOR circuit fails to provide adequate low outputs during '00' input transitions. The incomplete swings under described loading conditions provide lower power consumption, which is not desirable. II(a) provides efficient power consumption on account of minimum transistor sizes and absence of V_{DD} and *GND* rails, while II(c), although having lesser number of transistors, requires somewhat more power in comparison due to the added size of the nMOS transistor required for level restoration, and the static power loss on account of its permanent ON state. This design also faces slightly more delay due to the weaker restoration by the sized level restoring transistor (W/L ratio = 1:4), thus affecting the high-to-low transition delay.

Module III, implemented with minimum transistors and level restoration, provides adequately low PDP and full swing outputs enabling cascading of multiple adders.

IV. Proposed ULP Full Adder Design

The critical step of our design strategy is the appropriate sizing of the devices and selection of design modules for the proposed full adder design. The best choices for each module in Section III have thus been used to design a novel 12T ULP full adder, illustrated in Fig. 6.

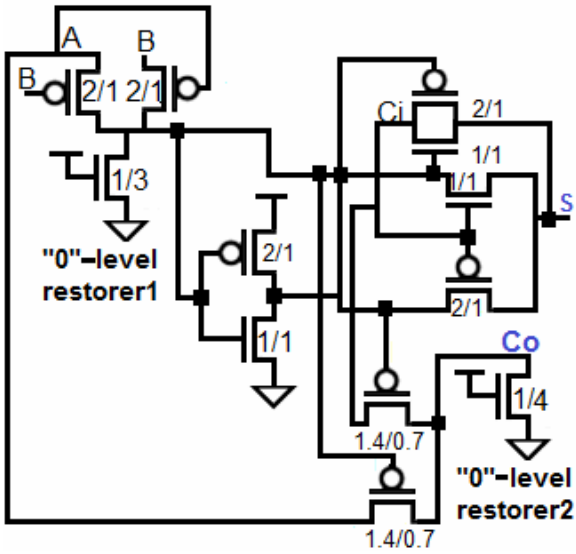


Fig. 6. Proposed ULP full adder design.

Module I(c) is the chosen design for the first module since it was observed to offer the best results for all 3 metrics, while also offering the minimum transistor choice (5T). Due to lower delay, it produces almost synchronous and balanced full-swing outputs, which improves the overall performance of the other modules relying heavily on the intermediate signals *H* and *H'*.

The design uses Module II(a) for the *S* output. Due to the absence of supply rails there are no short circuit currents, leading to inherently lower average power. Moreover, the circuit has improved delay due to the high-speed TG-based design with single-stage outputs obtained directly from the input combinations without any level restoration [15]. Thus it is expected to offer competitive results for overall PDP.

Module III was chosen as the only competitive design due to least number of transistors (3T) and full swing output waveforms.

Under the realistic inputs described earlier, the proposed design was observed to provide sharp transitions in output waveforms and sufficient levels to eliminate any errors. Fig. 7 shows sample input and output waveforms for the proposed adder at a supply voltage of 400 mV, simulated in a SPICE environment after suitably loading the circuit under test. It is seen to offer maximum and minimum high output levels at 400 and 375 mV respectively.

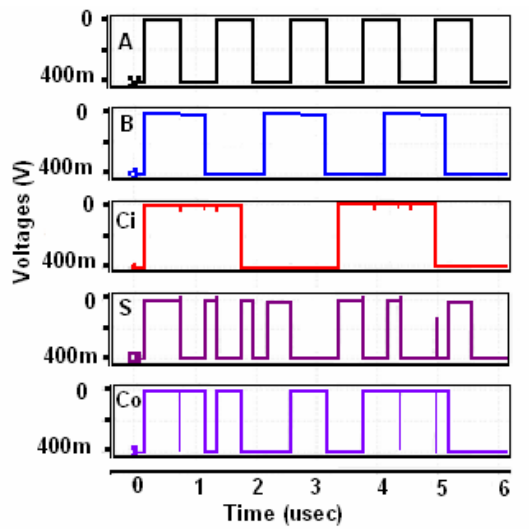


Fig. 7. Sample input and output waveforms for the proposed ULP adder.

V. Performance Evaluation

1. Simulation Strategies

To compare the performance of the full adder designs, we have performed extensive Monte Carlo simulations in a SPICE environment, estimating the average power dissipation (P_{avg}), propagation delay (t_p), and PDP at 22-nm technology using the predictive technology model (PTM) [32]. Low-to-high propagation delay (t_{plh}) of the critical signal C_o is estimated from the point when C_i reaches its 50% point, to the point when C_o reaches its 50% point from an initial low level. High-to-low propagation delay (t_{phl}) is estimated similarly from an initial high level. The propagation delay is then estimated as the average of these two ($t_p = (t_{plh} + t_{phl})/2$). P_{avg} is estimated by averaging the power supplied to the cell by the supply voltage (V_{DD}) during t_p. PDP is then evaluated as the product of P_{avg} and t_p.

To ensure completely functional circuits and accurate results, all possible input combinations are considered while scaling the supply voltage in an ultralow range (0.25-0.4 V), using a maximum input frequency of 1 MHz. The input pattern alternates the high frequency at the input nodes by concatenating patterns withdifferent frequency distributions among the 3 input signals [24].

To avoid underestimating effects of realistic input waveforms on design metrics, a simulation test bench is used which uses a 5-bit ripple carry adder (RCA) using

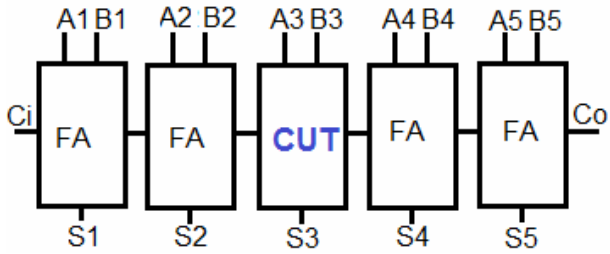


Fig. 8. Simulation test bench.

nominal copies of the 1-bit cell(Fig. 8).

Design metrics are then calculated for the middle cell, which implies equal loading on both input and output sides. Inputs A, B, and C_i and output S are suitably loaded with input buffers to provide realistic slopes.

To estimate realistic PVT variations, [33] anticipated ±10% variations in parameters such as channel length (L), gate width (W), channel doping concentration ($NDEP$), oxide thickness (t_{ox}), threshold voltage (V_t), and supply voltage (V_{DD}). Various process and environmental parameters are thus varied as independent Gaussian distributions with a 3σ variation of 10% in order to follow projected trends [34]. Standard deviation (σ) is a measure of the dispersion in design metrics that states numerically the extent to which individual observations vary from the average. Variability, defined as the ratio of the standard deviation (σ) to the mean value (μ), is then calculated for each of the three chosen metrics.

2. Power Comparison

Cosmetic perfection in device sizing helps in achieving ultralow power consumption for the proposed design. Fig. 9(a) illustrates power dissipation for various supply voltages scaled in the ultralow range (0.25-0.4 V). The proposed ULP adder is observed to offer excellent power characteristics at all V_{DD} values, hence validating the expected results. Among existing designs, the Static CMOS and Mirror adders provide the lowest average power while the CPL faces the highest values, following projected trends in previous comparisons. All other designs offer intermediate power between the two extremes, with FA Cells 3, 8 and 11 offering better characteristics due to their inferior driving ability [21, 22]. The proposed ULP design offers 38% saving with respect to the Static CMOS and Mirror adders, and as much as 75% improvement with respect to the CPL

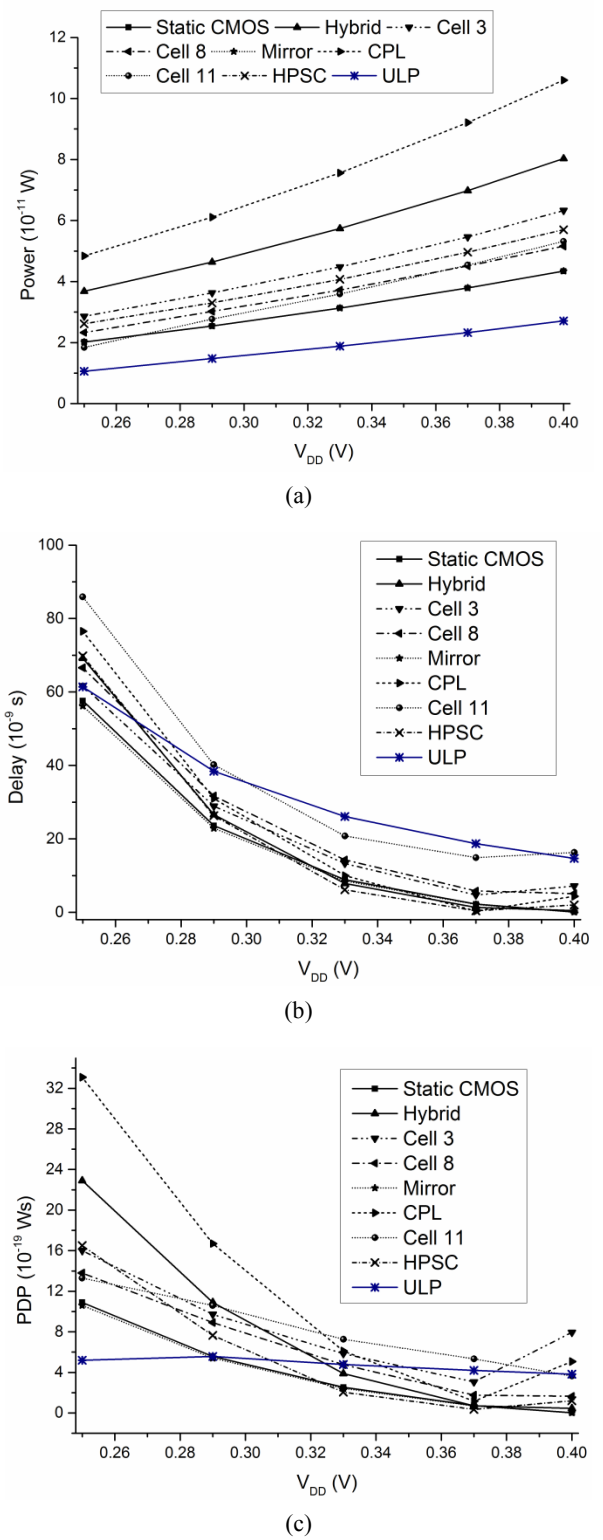


Fig. 9. Comparison of (a) power, (b) delay, (c) PDP characteristics against varying supply voltage.

adder at V_{DD} = 0.4 V.

As discussed earlier, the proposed design offers a minimum-transistor option to meet the desired requirements where other low-transistor designs fail to provide adequate waveforms. Modules I and III in this adder were optimized for reduced power with least transistor count. Further, due to the absence of supply rails in Module II(a) and thus no short circuit currents, the ULP design offers efficient power savings.

3. Delay Comparison

Propagation delay for all considered adder topologies are plotted in Fig. 9(b) against supply voltage. As observed, the proposed design faces comparable but slightly higher delay than other topologies due to the trade-off between power and delay in order to achieve ultralow power dissipation. This is largely on account of the threshold voltage loss in the pass-transistor circuits incorporated, which adversely affect the delay [23]. Among existing designs, the Static CMOS and Mirror adders provide the best delay characteristics due to efficient switching of internal transistors, whereas the HPSC and FA Cell 11 face the worst delay due to circuit complexity either in the input or output modules. All other adders have intermediate delay between the two, where topologies with inferior driving capabilities offer better values at nominal loads [21, 22].

The proposed adders use level restoration transistors in various modules which alleviate the threshold voltage loss in the pass transistor circuitry. These have to be effectively sized so that they do not affect the logic levels of other transitions and thus offer slower compensation, adding to the overall delay. The ULP adder design manages to provide competitive delay performance, especially at low supply voltages since the level restoration is quicker, although the characteristics degrade with increasing V_{DD}. In particular, it offers 28% improvement in delay in comparison to FA Cell 11 at 0.25 V, while being only 7% higher than the Static CMOS design.

In addition to the above delay comparison among all the cells, we also performed path delay analysis of our proposed design. The delays with reference to Fig. 8 from A1/B1 to Co and A1/B1 to S5 are estimated and reported in the Table 4.

4. PDP Comparison

The purpose of this section is to illustrate the overall

Table 4. Comparison of Delay from A1/B1 to Co and S5 in Proposed ULP Full Adder Cell @ V_{DD} = 0.4 V

Delay path	Input vectors					Delay (ns)
A1-Co	A1 = 0→1, B1 = 1, Ci = 0	A2 = 1, B2 = 0	A3 = 0, B3 = 1	A4 = 1, B4 = 0	A5 = 0, B5 = 1	86.62
B1-Co	A1 = 0→1, B1 = 0, Ci = 0	A2 = 0, B2 = 1	A3 = 1, B3 = 1	A4 = 0, B4 = 0	A5 = 1, B5 = 1	61.61
A1-S5	A1 = 0→1, B1 = 0, Ci = 0	A2 = 0, B2 = 1	A3 = 1, B3 = 1	A4 = 0, B4 = 0	A5 = 1, B5 = 1	51.58
B1-S5	A1 = 0→1, B1 = 0, Ci = 0	A2 = 0, B2 = 1	A3 = 1, B3 = 1	A4 = 0, B4 = 0	A5 = 1, B5 = 1	73.42

usefulness of the proposed adder while considering the trade-off in the PDP in order to achieve desired superior power characteristics and device count, which provides a quantitatively effective way to compare overall characteristics.

Fig. 9(c) shows the PDP characteristics of the adder topologies against varying supply voltage. The proposed ULP topology is observed to offer competitive PDP values with respect to the best results in existing designs at lower supply voltages.

Among conventional designs, the Static CMOS and Mirror adders offer the best PDP values for all supply voltages owing to the efficient CMOS logic implementation, but incur high area costs due to significantly high transistor count. The CPL and Hybrid adders face the worst PDP characteristics at low supply voltages, but the Hybrid adder performs better at higher values. The HPSC adder and FA Cells 3, 8, and 11 maintain good results for the intermediate supply voltage range.

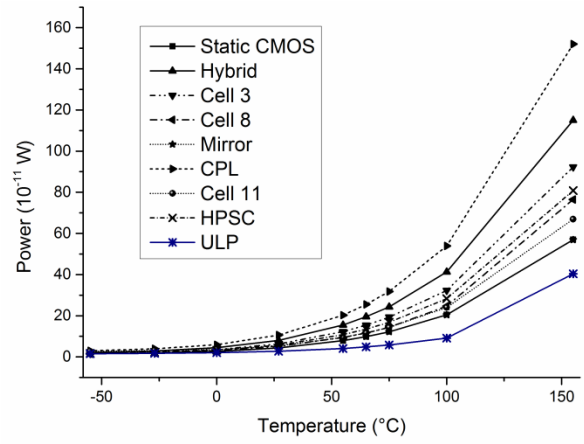
The proposed ULP adder offers stable PDP characteristics throughout the supply voltage range, offering significant improvement compared to existing designs at lower voltages. In particular it offers as much as 52% improvement in PDP at 0.25 V with respect to the Static CMOS FA, while being close to the best values at higher voltages. It thus maintains an adequate trade-off between power and delay in order to achieve ultralow power characteristics, offering competitive PDP characteristics throughout the chosen subthreshold voltage range.

5. Temperature Analysis

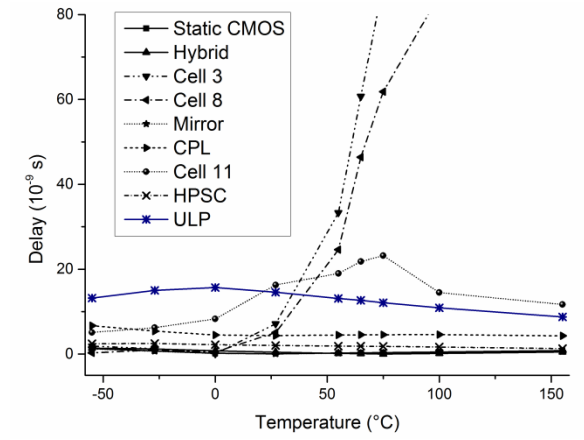
Digital systems in highly scaled technology nodes face considerable variations in temperature that significantly affect the performance of the circuits. The purpose of this subsection is to verify the stability of the proposed design even under extreme ambient conditions. To investigate the impact of the same, the performance metrics are estimated within a range of -55 to 155°C, the estimated range for testing of current fabricated microprocessors. The supply voltage is fixed at 0.4 V and the process variations described earlier are retained in the Monte Carlo simulations.

The power, delay and PDP characteristics are plotted in Fig. 10(a)-(c) against varying temperature. The average power in Fig. 10(a) is seen to uniformly rise with increasing temperature for all full adder designs.The CPL adderfaces the worst rise in power due to the added circuital complexity. The proposed adder is seen to retain the best power characteristics throughout the range of temperatures, verifying its operational stability even under extreme environmental conditions. In particular, it outperforms the Static CMOS FA by upto 41% at the upper temperature limit of 155°C.

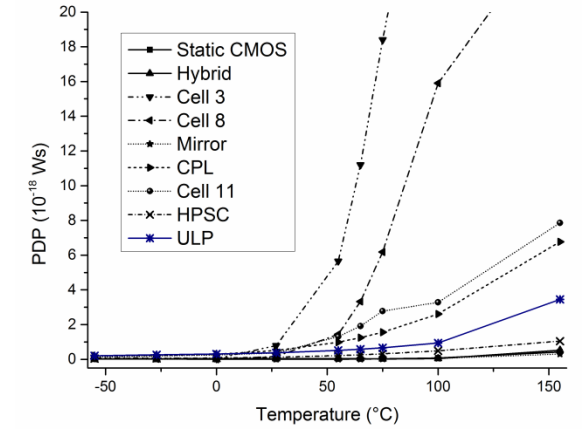
The conventional adder designs retain relatively constant values of propagation delay in Fig. 10(b), indicating that it is not significantly affected by temperature provided the circuit maintains stable outputs. The non-conventional FA Cells 3, 8 and 11 on the other hand are seen to be adversely affected by varying temperature, making them unsuitable for fail-safe use. Cells 3 and 8 are seen to undergo a breakdown above 50°C with sharply rising delay, while Cell 11 has a significant rise in delay without breaking down. The ULP design maintains relatively stable values similar to conventional circuits. As discussed in Section V-C, although it faces slightly higher delay due to the trade-off between power and delay, it is comparable to conventional values while offering lower delay than Cells 3, 8 and 11 at higher temperatures (> 50°C). PDP, numerically representing the effective trade-off between power and delay, is observed to be relatively stable over the temperature range in Fig. 10(c) for both conventional as well as ULP designs, with a slight rise at temperatures above 100°C due to the steady rise in power. The CPL adder is seen to have progressively rising PDP above



(a)



(b)



(c)

Fig. 10. Comparison of (a) power, (b) delay, (c) PDP characteristics against varying temperature.

27°C since it faces the worst rise in power dissipation, whereas the FA Cells 3, 8 and 11 face the worst PDP due to the adverserise in delay. The ULP design is seen to offer stable PDP values very close to the best conventional adders throughout the temperature range, while offering significantly better characteristics than the inferior existing designs. In particular, it offers up to 49% and 56% savings respectively with respect to the CPL and Cell 11 FAs at 155°C. Thus its use for ultralow power and area-efficient design without facing excessive trade-off costs in delay is validated.

6. Variability Analysis

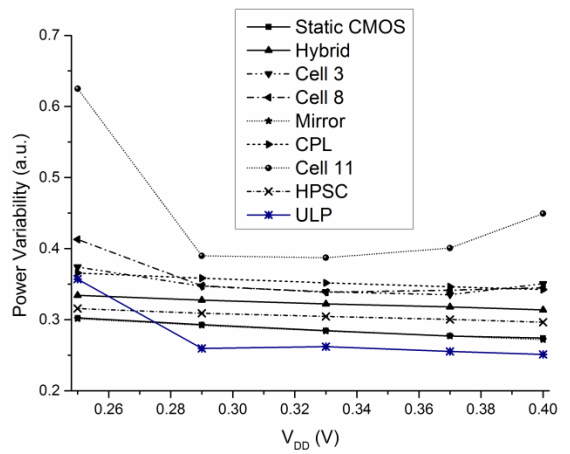
Digital circuits are subject to adverse PVT variations under ultra-deep submicron (UDSM) technology processes which affect their performance and trigger unexpected deviation from anticipated outputs, especially when operated in the sub-threshold region where the current follows an exponential dependency [33, 34]. The variability for each of the three performance metrics are estimated as described in Section V-A and are plotted in Fig. 11(a)-(c). It is observed from Fig. 11(a) that power variability remains effectively constant with varying supply voltage regardless of the topology.

This can be explained by the fact that due to deep subthreshold operation, the impact of SCEs such as DIBL is less pronounced in comparison to the superthreshold region. Hence it is not significantly affected by changes in the supply voltage. Among existing designs, Static CMOS, Mirror and HPSC FAs are seen to have the lowest variability by virtue of the increased V_t due to body effect of the stacked transistors, which has been shown to reduce the effect of variations [13-15]. The CPL and the non-conventional Cells 3, 8 and 11 FAs face the worst variability in the same range.

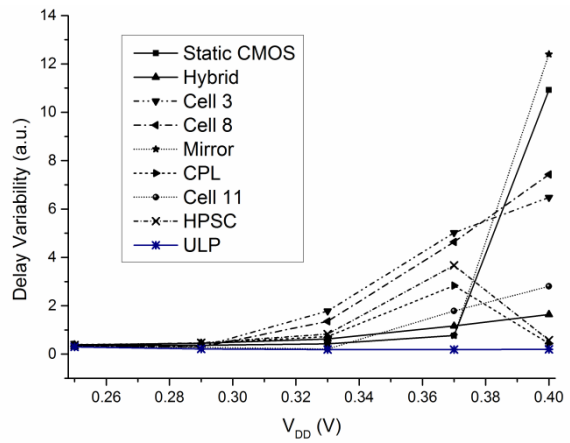
Delay is conventionally estimated by the following model

$$t_p = \frac{C_L}{I_{DS}} \cdot \frac{V_{DD}}{2} \tag{5}$$

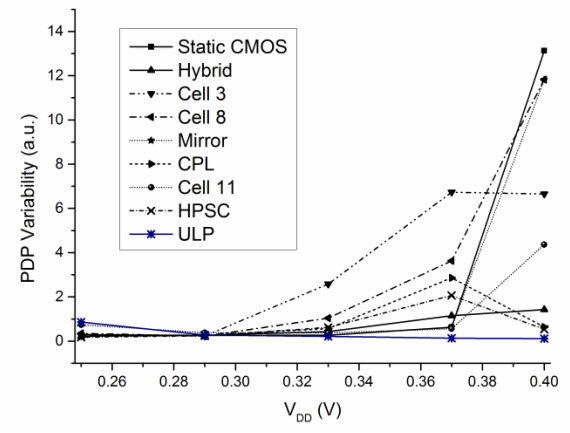
where C_L is the load capacitance and I_{DS} is the drain-to-source current [36]. It was shown in [15] that variations in C_L only have a minor impact on delay variability. Thus, they are largely dependent on I_{DS}, which intrinsically depends on the topology and size of the circuits. This is verified in Fig. 11(b), where the FA designs follow dissimilar trends in delay variability, even though it increases in general with increasing V_{DD}. The higher



(a)



(b)



(c)

Fig. 11. Comparison of (a) power, (b) delay, (c) PDP variability against varying supply voltage.

logic depth and stacking effect in conventional designs with high transistor counts including Static CMOS, Mirror and Hybrid adders reduce relative variations [37]. Above 0.35 V, these follow dissimilar trends where variability increases slightly for the Hybrid FA, increases sharply for the Static CMOS and Mirror FAs, and decreases slightly for the HPSC and CPL adders. The FA Cells 3 and 8 face the worst effect of such variations, while Cell 11 manages to perform better.

The proposed ULP adder is seen to offer the best results in terms of both power and delay variability throughout the voltage range. In particular, it offers up to 8% improvement in power variability at 0.37 V with respect to the best resultsoffered by the Static CMOS FA, with delay variability offering improvements up to even 75% at the same voltage. This can be attributed to the optimum transistor sizing, i.e. increased lengths for the pull-down transistors and increased area for the pull-up transistors, which have been shown to alleviate the effects of process variations in subthreshold circuits from critical sources including RDF, SCE and DIBL [35, 38]. The V_t and subthreshold slope largely depend on the channel length, variations in which can lead to significant mismatch in transistor drive strengths. Thus lengthening the channel alleviates SCEs such as DIBL. Moreover, the V_t variation induced by RDF is inversely proportional to the square root of the channel area ($\delta V_t \approx 4/(W \times L)^{1/2}$) [37]. Thus the increased transistor size in the proposed design serves to ease out the effects of random process variations, achieving superior variability. Considering the combined effect of power and delay, the ULP adder provides the best characteristics in PDP variability in Fig. 11(c), where the remaining adders follow similar trends as described above. In particular, up to 79% improvement in PDP variability is seen at 0.37 V with respect to the Static CMOS FA.

Variability of design metrics, particularly, timing variability grows dramatically as V_{DD} reduces. This is due to the fact that the device current is exponentially sensitive to V_t, V_{DD}, and inverse subthreshold slope [39]. Authors in [38] showed that the device ON-current ($I_{ON\text{-}SUB}$) and OFF-current ($I_{OFF\text{-}SUB}$) in subthreshold operation (V_{DD} = 200 mV) are extremely sensitive to decrease/ increase/mismatch in V_{DD}/V_t as compared to superthreshold operation (V_{DD} = 1 V) (see Table 5).

Subthreshold (sub-V_t) operation differs from superthreshold (super-V_t) operation mainly because the ON-current ($I_{ON\text{-}SUB}$) in sub-V_t operation depends exponentially on threshold voltage (V_t) and power supply voltage (V_{DD}), while the ON-current ($I_{ON\text{-}SUPPER}$) in super-

Table 5. Comparison of key Subthreshold, Near-threshold, and Super-threshold NMOSFET Sensitivities

	Sub-V_t	Near-V_t	Super-V_t
Operation voltage (V_{DD})	200 mV	400 mV	1 V
Sensitivity of I_{ON} to 100-mV V_{DD} reduction	18×	4.6×	1.2×
Sensitivity of $I_{ON}$to 100-mV V_t increase	11×	3.7×	1.17×
Sensitivity of $I_{OFF}$to 100-mV V_t increase	16×	15×	12×
Sensitivity of $I_{ON,N\text{-}FET}/I_{ON,P\text{-}FET}$ ratio to 100-mV V_t mismatch	10×	3.7×	1.17×

V_t operation depends roughly linearly on V_t and V_{DD} [38].

As can be seen, the impact of variation is far more severe when V_{DD} is scaled down. The strong dependence on V_t, and V_{DD} leads to wide fluctuations in both delay and energy (power-delay product). Therefore, the variability of PDP is higher in the proposed circuit in the lower voltage range (see Fig. 11) even though its mean value is lower (see Fig. 9).

7. Supply Voltage Scaling

A critical requirement for any novel design is scalability into future technologies. An increasing demand for energy-constrained design has motivated designers to continually scale supply voltage, which significantly reduces both active and static components of power [33].

In the subthreshold region, circuits face various adverse effects like process variations, increased leakage and lower switching speeds, which limit further scalability. While the other factors adjudge circuit performance, the switching speed essentially decides the logical functionality of the circuit; the circuit is no longer usable if the switching speed becomes too slow.

The suitability of the output waveform can be evaluated in terms of the rise time t_r, which effectively decides how fast the circuit is able to respond to a logical transition in the input waveforms. If t_r becomes too high, the waveform might not be able to keep up with the clock circuitry used to read the outputs and lead to serious logical errors. We thus evaluate the output rise time with respect to the critical output carry (C_o) signal while scaling the supply voltage down to the minimum possible values. The obtained results are plotted in Fig. 12.

As observed, the conventional high-transistor count designs allow more scalability due to efficient implementation based on traditional logic families which tend to have full swing outputs. The lower switching speeds are averaged out over the increased number of stages, so that the output is ultimately able to respond efficiently to input transitions. On the other hand the non-conventional FA Cells 3, 8 and 11 face inferior voltage scalability with increased rise times. This can be attributed to their inherent lack of driving capability due to the use of transmission gates in the output modules, which tend to degrade outputs when connected in a chain of adders. The proposed ULP adder is seen to offer intermediate values between the two, allowing scaling of supply voltage up to 0.18 V. Thus its outputs efficiently account for logical transitions in the inputs with a reasonable rise time in order to be read using fast-switching clock circuitry for the entire voltage range.

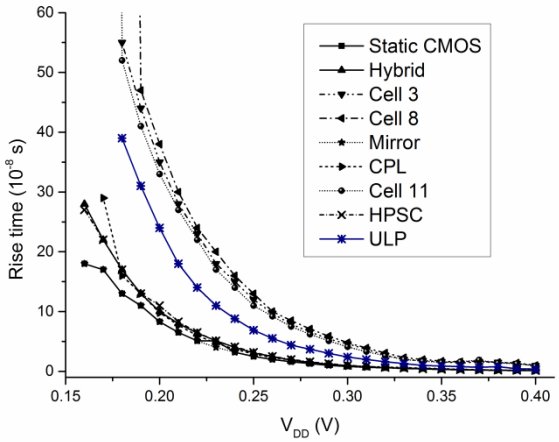


Fig. 12. Comparison of voltage scalability in terms of rise time against varying supply voltage.

8. Leakage Power Comparison

It is a known fact that down scaling of devices results in leakier devices compared to long channel devices. In short channel devices,the major shareholder in total power dissipation is leakage power. Therefore, estimation and reduction of leakage power is very important for designing ultralow power circuits. Leakage power is known as the power consumed when the circuit is operated in standby mode. It is expressed as

$$P_{Leakage} = V_{DD} I_{OFF} \tag{6}$$

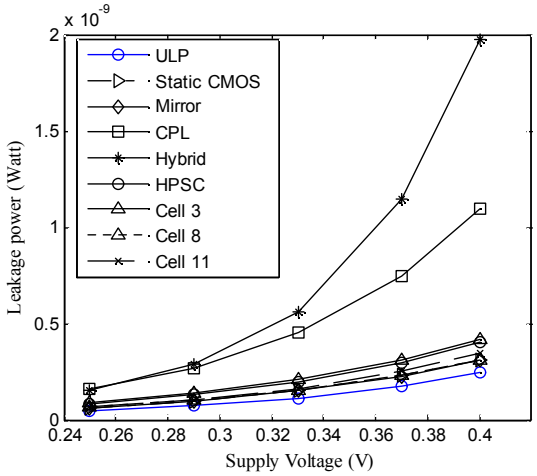


Fig. 13. Comparison of leakage power against varying supply voltage.

where I_{OFF} is the leakage current in the circuit. In this work, to calculate leakage power of all the full adder circuits, the inputs are considered to be '0'. Estimated leakage powers of all the full adder cells are plotted in Fig. 13. The proposed ULP adder is observed to consume lower leakage power at all considered V_{DD} values compared to that of other full adder circuits. This is achieved due to proper sizing of devices, particularly of "0"-level restorers, in the proposed circuit. The "0"-level restorer1 and "0"-level restorer2 are sized 3× and 4× longer than the minimum sized NMOSFET respectively. The proposed design have direct path for certain input patters such as A/B = 1/0 or 0/1 and output such as Co = 1. This may lead to higher static current flow resulting in higher static power dissipation in superthreshold region of operation. However, we have proposed the circuit for subthreshold operation, where current through the MOSFET decreases exponentially with the decrease in gate voltage (V_{GS}). This exponential dependent of current on V_{GS} dramatically increases channel resistance and hence decreases static power dissipation. This is clearly observed by performing DC operating point analysis of an NMOSFET (see Table 6 and Fig. 14). As can be observed, the channel resistance of a minimum sized NMOSFET is 0.132 MΩ in subthreshold region (@ V_{DD} = 0.4 V), whereas that in superthreshold region (@ V_{DD} = 0.8 V) is 0.025 MΩ. As can be seen, the static power consumption of a minimum sized NMOSFET is 1.211 μW in subthreshold region (@ V_{DD} = 0.4 V), whereas that in superthreshold region (@ V_{DD} = 0.8 V) is

Table 6. Comparison Channel Resistance and Power Consumptoon Through an NMOSFET @ 22-nm Technology Node for Channel Lengths 22 nm, 66 nm, and 88 nm

V_{DD} (V)	W/L = 22 nm/22 nm		W/L = 22 nm/66 nm		W/L = 22 nm/88 nm	
	$R_{Channel}$ (MΩ)	Pwr (μW)	$R_{Channel}$ (MΩ)	Pwr (μW)	$R_{Channel}$ (MΩ)	Pwr (μW)
0.4	0.132	1.211	3.484	0.046	5.070	0.032
0.8	0.025	107.343	0.101	88.342	0.133	86.768

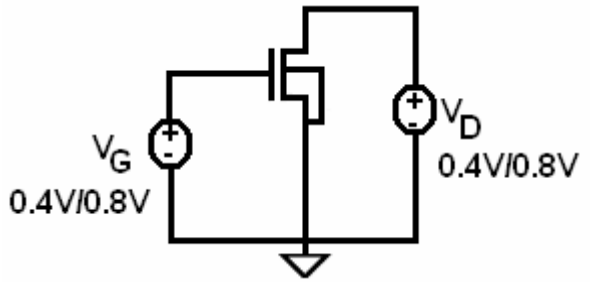


Fig. 14. DC Analysis of nMOS transistor.

107.343 μW . The "0"-level restorer1 (sized as W/L = 22 nm / 66 nm) exhibits much higher (26.39×) channel resistance and hence consumes much lower (26.32×) static power compared to its minimum sized counterpart @ V_{DD} = 0.4 V. The "0"-level restorer2 (sized as W/L = 22 nm/88 nm) shows much higher (38.41×) channel resistance and hence consumes much lower (37.84×) static power compared to its minimum sized counterpart @ V_{DD} = 0.4 V. Therefore, even though there is direct path due to "0"-level restorers, static power consumption is considerably lower compared to that of other full adder circuits considered for comparison.

VI. Conclusion

This paper proposes a novel full adder design based on pass-transistor logic. The major advantage of Pass Transistor Logic (PTL) is its low device count, which results in saving of silicon area. Lower device count also implies lower static power consumption since static power is inversely proportional to device count/silicon area. Reduced number of transistors also signifies lower internal node capacitances, which results in lower dynamic power dissipation. Therefore, the proposed PTL based design is suitable for ultralow power applications.

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