

Triple-gate Tunnel FETs Encapsulated with an Epitaxial Layer for High Current Drivability

Jang Woo Lee and Woo Young Choi

Abstract—The triple-gate tunnel FETs encapsulated with an epitaxial layer (EL TFETs) is proposed to lower the subthreshold swing of the TFETs. Furthermore, the band-to-band tunneling based on the maximum electric-field can occur thanks to the epitaxial layer wrapping the Si fin. The performance and mechanism of the EL TFETs are compared with the previously proposed TFET based on simulation.

Index Terms—Tunnel field-effect transistor (TFET), band-to-band tunneling (BTBT), vertical tunneling, Si fin, epitaxial layer (EL)

I. INTRODUCTION

Recently, the rapid progress of CMOS downscaling has enhanced both chip density and performance. On the other hand, power consumption becomes a critical issue for mobile applications. A tunnel field-effect transistor (TFET) is regarded as a promising solution to extremely-low-power applications due to the extremely low off-current (I_{off}) and sub-60 mV/dec subthreshold swing (SS) at room temperature [1, 2]. Although TFETs feature sub-60-mV/dec SS by using the band-to-band tunneling (BTBT) mechanism, and the BTBT occurs only at low current region. Thus, it is difficult to boost the on-current (I_{on}) of TFETs while keeping their I_{off} low [3-5]. In order to improve the performance of the TFETs, some vertical

BTBT structures have been reported [6-9]. Y. Morita *et al.* proposed the parallel electric field TFETs (PE TFETs) and synthetic electric field TFETs (SE TFETs) which used vertical BTBT through the epitaxial layer (EL) grown on the source [10-12]. SE TFETs show higher I_{on} than that of PE TFETs since SE TFETs have lower SS than that of PE TFETs and it is due to the enhanced electric field at the both sides of the EL as shown in Fig. 1(a). However, although there is the synthetic electric field effect in SE TFETs, it is less efficient for vertical BTBT. It is because the direction of the maximum synthetic electric field inclines towards the side of the fin. Thus, it is important to improve the tunneling efficiency of vertical TFETs.

In this paper, EL TFETs are proposed to maximize vertical band-to-band tunneling (BTBT) efficiency by using the ultrathin epitaxial layer surrounding the fin as shown in Fig. 1(b). The performance and device characteristics of EL TFETs are simulated in comparison with SE TFETs. Unlike SE TFETs, the vertical BTBT of EL TFETs can occur towards the direction of the maximum electric field at the corner of the fin. Therefore, EL TFETs have lower SS than that of SE TFETs.

II. SIMULATION CONDITIONS

Three-dimensional (3D) TCAD simulations for n-type TFET structures shown in Fig. 1 have been performed by using Synopsys Sentaurus [13]. All the device simulation parameters are summarized in Table 1. The performance of two kinds of TFETs is compared in terms of effective SS (SS_{eff}). Their definitions are shown in Table 2. The BTBT generation rate (G_{BTBT}) is calculated by the dynamic nonlocal path BTBT model. The Kane tunneling

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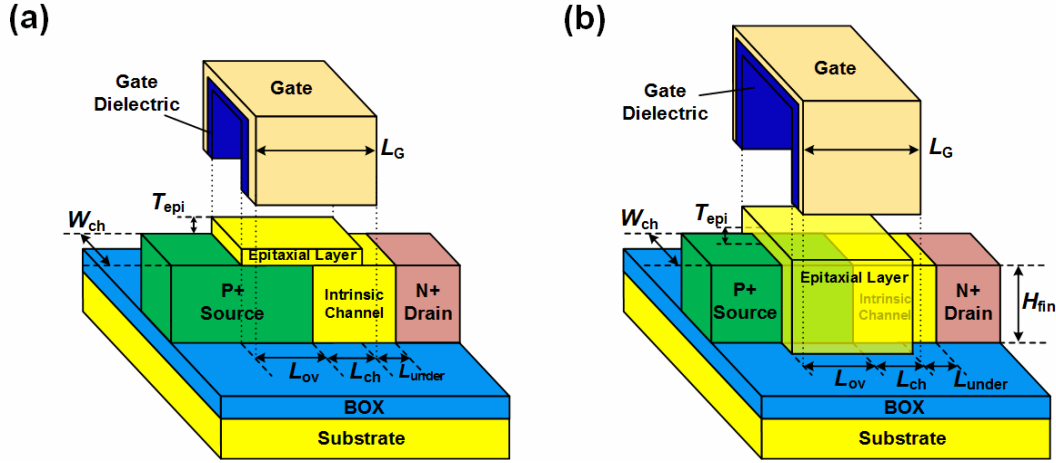


Fig. 1. Schematics of (a) SE TFETs, (b) EL TFETs.

Table 1. Simulation parameters of the TFETs

Source/Drain doping concentration	$1 \times 10^{20} \text{ cm}^{-3}$
Channel doping concentration	$1 \times 10^{16} \text{ cm}^{-3}$ (p-type)
EL doping concentration	$1 \times 10^{16} \text{ cm}^{-3}$ (p-type)
Gate length (L_G)	200 nm
Gate-source overlap length (L_{ov})	100 nm
Gate-drain underlap length (L_{under})	20 nm
Height of the fin (H_{fin})	40 nm
Width of the fin (W_{fin})	10 nm
Thickness of epitaxial layer (T_{epi})	2 nm
Gate dielectric EOT (t_{ox})	0.4 nm

Table 2. Performance parameters of the TFETs

Turn-on voltage ($V_{turn-on}$)	V_G when I_D exceeds 10 fA/ μm
Overdrive voltage (V_{ov})	$V_G - V_{turn-on}$
On-current (I_{on})	I_D when $V_{ov} = 0.7 \text{ V}$
Effective subthreshold swing (SS_{eff})	Average slope when I_D increases from 10 fA/ μm to 0.1 nA/ μm
Drain bias voltage (V_D)	0.7 V

parameters A and B are determined as $3.29 \times 10^{15} / \text{cm}^3 \cdot \text{s}$ and 23.8 MV/cm , respectively [14].

Furthermore, Fermi-Dirac statistics, band gap narrowing, Shockley-Read-Hall (SRH) recombination and Lombardi mobility model are used for simulations. In addition, the modified local density approximation (MLDA) model is applied to consider the quantization effect [15].

III. RESULTS AND DISCUSSIONS

Fig. 2 shows the transfer characteristics of the SE

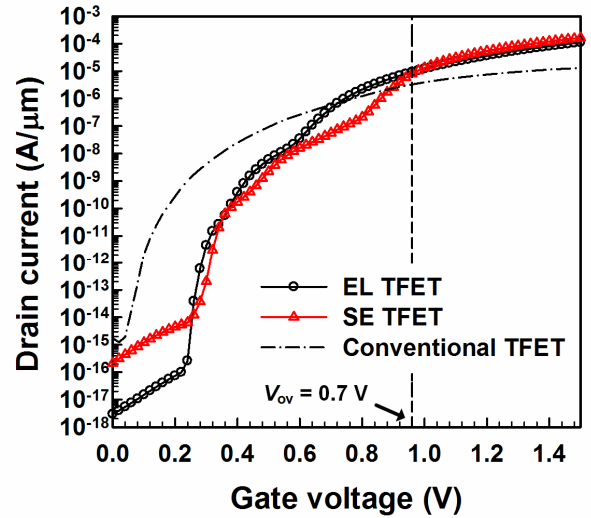


Fig. 2. Transfer characteristics of the SE TFETs, EL TFETs, and conventional TFETs. $L_{under} = 20 \text{ nm}$ is set to suppress the ambipolar current of TFETs. The $I_{on} = 7.9 \mu\text{A}/\mu\text{m}$, $9.1 \mu\text{A}/\mu\text{m}$, and $1.1 \mu\text{A}/\mu\text{m}$, and $SS_{eff} = 30.34 \text{ mV/dec}$, 24.37 mV/dec , and 33.09 mV/dec for SE TFETs, EL TFETs, and conventional TFETs, respectively.

TFETs, EL TFETs, and conventional TFETs as a function of gate voltage (V_G). TFETs with an EL exhibits higher I_{on} than that of the conventional TFETs because the tunneling direction is parallel to the electric field by applied V_G . Until $V_{ov} = 0.7 \text{ V}$, SS_{eff} of EL TFETs is lower than that of SE TFETs since EL TFETs can utilize vertical band-to-band tunneling based on the maximum electric field due to the EL on the both sides of the fin. To compare the synthetic electric field effect of SE and EL TFETs, the electric field intensity is drawn in Fig. 3 at the V_{ov} of 0.5 V, respectively. As illustrated in the Fig. 3, the maximum electric field, which is formed at the corner,

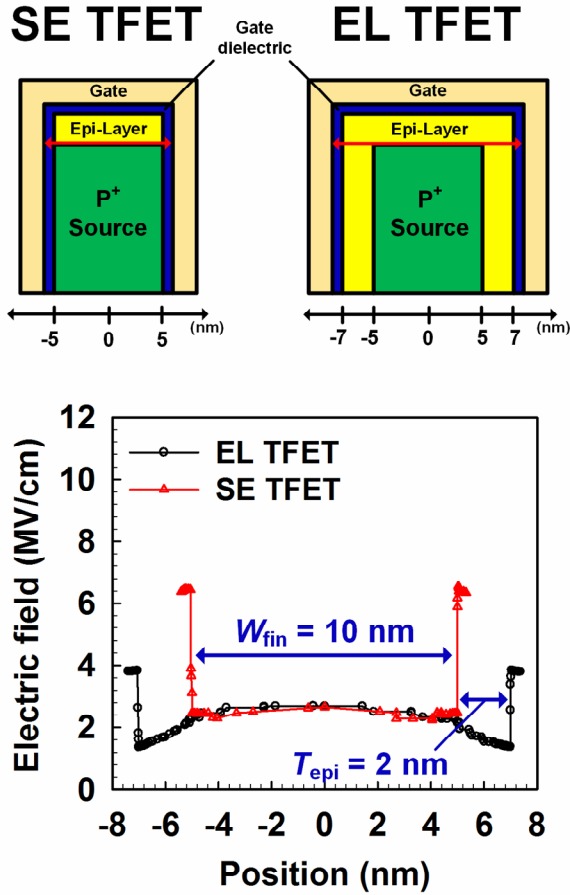


Fig. 3. Electric field intensity of SE TFETs and EL TFETs at the $V_{ov} = 0.5$ V is extracted along the source-to-EL junction at the top of the Si fin, respectively.

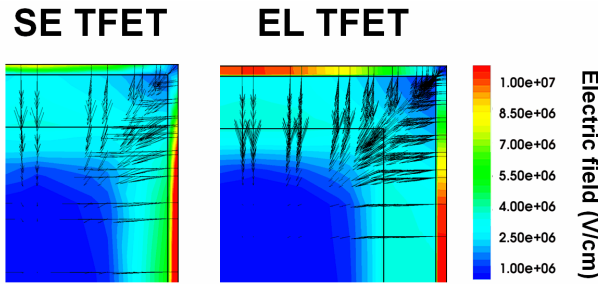


Fig. 4. 2-D electric field contour plots which are cross-sectional views of SE TFETs and EL TFETs. Cross-sectional view at the half of source with $V_{ov} = 0.5$ V. The direction of electric field is also depicted in the plots.

of SE TFETs is always stronger than that of EL TFETs because the EL at the both sides of fin alleviates the synthetic electric field in EL TFETs. However, the direction of the maximum electric field inclines towards the side of the fin as depicted in the Fig. 4. It means that the enhanced electric field is less efficient for SE-TFETs than that of EL TFETs because there is no tunneling-

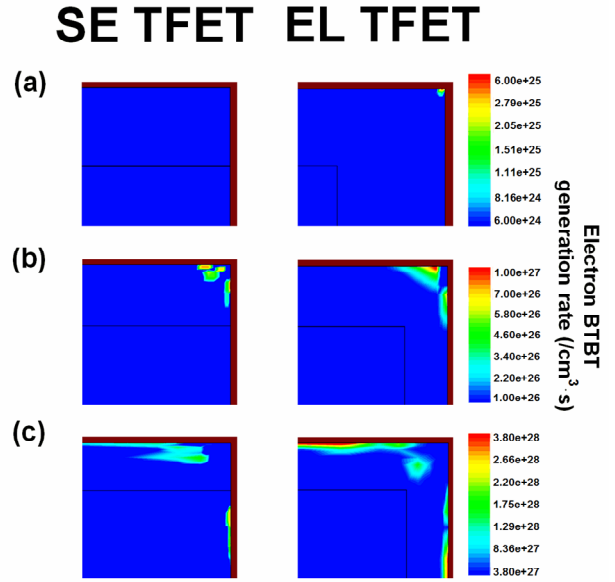


Fig. 5. BTBT generation rate (G_{BTBT}) of SE TFETs and EL TFETs. G_{BTBT} is illustrated at (a) $V_{ov} = 0.02$ V, (b) $V_{ov} = 0.2$ V, (c) $V_{ov} = 0.5$ V, respectively. G_{BTBT} is observed at the range from the maximum value to 10 times below. Maximum G_{BTBT} value is $6.0 \times 10^{25} / \text{cm}^3 \cdot \text{s}$, $1.0 \times 10^{27} / \text{cm}^3 \cdot \text{s}$, $3.8 \times 10^{28} / \text{cm}^3 \cdot \text{s}$ for (a), (b), and (c), respectively.

available area at the side of the fin in the case of SE TFETs. On the other hand, the BTBT based on the maximum electric field can be generated in the case of EL TFETs thanks to the EL on the both sides of the fin. Thus, although the maximum electric field intensity of EL TFETs is lower than that of SE TFETs, the BTBT rate can be more enhanced for EL TFETs. The G_{BTBT} of SE TFETs and EL TFETs are illustrated in Fig. 5 and therefore, G_{BTBT} of EL TFETs is always higher than that of SE TFETs until $V_{ov} = 0.7$ V. However, after the V_{ov} is equal to 0.7 V, the drain current of SE TFETs is higher than that of EL TFETs. It is because the electric field at both sides of the source, which directly face the side-gates, is so high that the G_{BTBT} overtakes that of EL TFETs.

Before the V_{ov} of 0.1 V, the abrupt change of drain current can be found in EL TFETs as shown in Fig. 2. It is because the BTBT occurs along the direction of maximum electric field at the two corners of source-to-channel junction where the electric field is enhanced and it is drawn in Fig. 5(a) [16]. Furthermore, the built-in potential drop by EL, which encapsulates those two corners, also conduces SS_{eff} of EL TFETs to be low. However, although this lower SS_{eff} is attributed to the BTBT at those two corners, the valid voltage range is

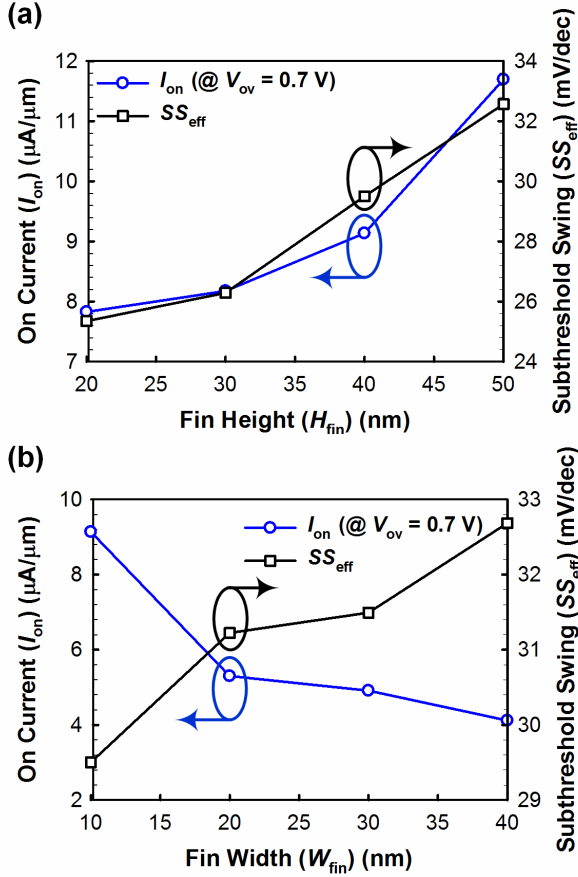


Fig. 6. I_{on} and SS_{eff} of EL TFETs with the variation of (a) H_{fin} , (b) W_{fin} .

small. It is because the two factors enhancing the electric field at the corners not depend on the V_{ov} below 0.1 V, and saturates after V_{ov} of 0.1 V. On the other hand, SE TFETs also have two corners at the source-to-channel junction. However, BTBT efficiency of SE TFETs is lower than that of EL TFETs. Thus, SS_{eff} is lower in the case of EL TFETs. Nevertheless, by the synthetic electric field effect in SE TFETs, an intersection is found in the transfer curves of SE TFETs and EL TFETs as shown in Fig. 2 at $V_{ov} = 0.1$ V.

Fig. 6(a) and (b) show the influence of the height (H_{fin}) and width (W_{fin}) of a Si fin on the EL TFETs. Because the EL is formed on the top and sidewall of a fin, the vertical BTBT cross-sectional area is proportional to H_{fin} . Therefore, the increase of H_{fin} leads to I_{on} boosting in the case of EL TFETs. However, I_{on} , which is a function of H_{fin} , declines non-linearly as H_{fin} decreases. It is because the enhanced gate controllability and it slightly improves SS_{off} . In the same manner, as W_{fin} is scaled down, SS_{eff} of EL TFETs becomes slightly lower and it results in

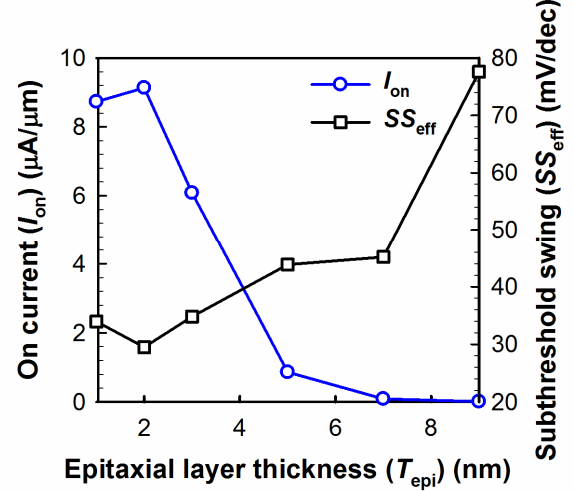


Fig. 7. I_{on} and SS_{eff} of EL TFETs with the variation of T_{epi} .

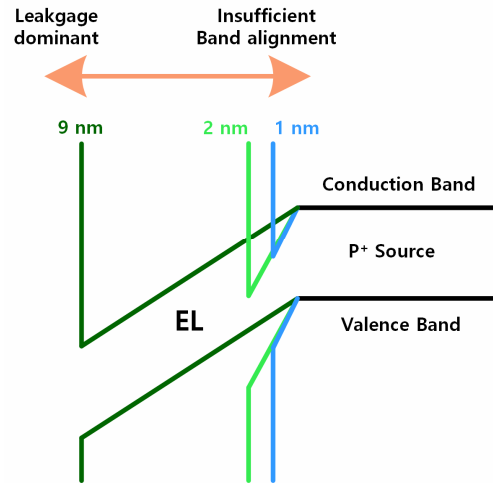


Fig. 8. On-state energy band diagram along the vertical direction of the tunneling region. The T_{epi} ranges from 2 to 9 nm.

increase of I_{on} because of enhanced gate controllability.

Fig. 7 illustrates the effect of an EL thickness (T_{epi}) on EL TFETs and the optimized T_{epi} is 2 nm. It is explained by the schematic on-state energy band diagram shown in Fig. 8. When T_{epi} is 1 nm, as an example of smaller than the optimized value of T_{epi} , it is difficult for the valence band edge of the EL to be aligned with the conduction band edge of the source, which means that higher V_G needs to be applied to turn on EL TFETs. On the other hand, when T_{epi} is 9 nm, as an example of higher than the optimized value of T_{epi} , BTBT barrier width across the EL is increased so that the electric field is decreased at the EL. Therefore, it degrades the vertical BTBT efficiency.

IV. CONCLUSIONS

EL TFETs are proposed and evaluated in comparison with previously reported SE TFETs. Because the BTBT occurs based on the maximum electric field, EL TFETs show higher performance than SE TFETs. Moreover, EL TFETs show low SS_{eff} by their own BTBT mechanism. For further improvement of EL TFETs, low bandgap materials such as SiGe or Ge can be introduced. As an extremely-low-power applications, the proposed EL TFET can be a promising solution.

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REFERENCES

- [1] W. Y. Choi, B. G. Park, J. D. Lee and T. J. K. Liu, "Tunneling Field-Effect Transistors (TFETs) with Subthreshold Swing (SS) Less Than 60 mV/dec," *IEEE Electron Device Letters*, vol. 28, no. 8, pp.743-745, 2007.
- [2] A. M. Ionescu, H. Riel, "Tunnel field-effect transistors as energy-efficient electronic switches," *Nature*, vol. 479, no. 7373, pp.329-337, 2011.
- [3] W. G. Vandenberghe, A. S. Verhulst, B. Soree, W. Magnus, Guido Groeseneken, Q. Smets, M. Heyns, and M. V. Fischetti, "Figure of merit for and identification of sub-60mV/decade devices," *Applied Physics Letters*, vol. 102, no. 1, pp.013510, 2013.
- [4] W. Cao, D. Sarkar, Y. Khatami, J. Kang, and K. Banerjee, "Subthreshold-swing physics of tunnel field-effect transistors," *AIP Advances*, vol. 4, no. 6, 2014.
- [5] U. E. Avci, D. H. Morris, and I. A. Young, "Tunnel Field-Effect Transistors: Prospects and Challenges," *Journal of the Electron Device Society*, vol. 3, no. 3, pp.88-95. 2015.
- [6] J. Knoch, S. Mantl, J. Appenzeller, "Impact of the dimensionality on the performance of tunneling FETs: Bulk versus one-dimensional devices," *Solid-State Electronics*, vol. 51, no. 4, pp.572-578, 2007.
- [7] K. Ganapathi, Y. Yoon, and S. Salahuddin, "Analysis of InAs vertical and lateral band-to-band tunneling transistors: Leveraging vertical tunneling for improved performance," *Applied Physics Letters*, vol. 97, no. 3, 2010.
- [8] L. D. Michielis, A. M. Ionescu "Electron-hole bilayer tunnel FET for steep subthreshold swing and improved ON current," *Proceedings of the European Solid-State Device Research Conference (ESSDERC)*, 2011.
- [9] S. W. Kim, J. H. Kim, T. J. K. Liu, W. Y. Choi, and B. G. Park, "Demonstration of L-Shaped Tunnel Field-Effect Transistors," *IEEE Transactions on Electron Devices*. vol. 63, no. 4, pp.1774-1778. 2016.
- [10] C. Alper, P. Palestri, J. L. Padilla, A. M. Ionescu, "The Electron-Hole Bilayer TFET: Dimensionality Effects and Optimization," *IEEE Transactions on Electron Devices*, vol. 64, no. 6, 2016.
- [11] Y. Morita, T. Mori, S. Migita, W. Mizubayashi, A. Tanabe, K. Fukuda, T. Matsukawa, K. Endo, S. O'uchi, Y. X. Liu, M. Masahara, and H. Ota, "Tunnel Field Effect Transistor with Epitaxially Grown Steep Tunnel Junction Fabricated by Source/Drain-first and Tunnel-junction-last Processes," *Japanese Journal of Applied Physics*, vol. 52, no. 4S, p.04CC25, 2013.
- [12] Y. Morita, T. Mori, S. Migita, W. Mizubayashi, A. Tanabe, K. Fukuda, M. Masahara, and H. Ota, "Performance Limit of Parallel Electric Field Tunnel FET and Improvement by Modified Gate and Channel Configurations," *IEEE Proceedings of the European Solid-State Device Research Conference (ESSDERC)*, 2013.
- [13] Y. Morita, T. Mori, S. Migita, W. Mizubayashi, A. Tanabe, K. Fukuda, T. Matsukawa, K. Endo, S. O'uchi, Y. X. Liu, M. Masahara, and H. Ota, "Performance Enhancement of Tunnel Field-Effect Transistors by Synthetic Electric Field Effect," *IEEE Electron Device Letters*, vol. 35, no. 7, 2014.
- [14] *Sentaurus Device User Guide Version: H-2013.03*, Synopsys Inc., Mountain View, CA, USA, 2013.

- [15] K.-H. Kao, A. S. Verhulst, W. G. Vandenberghe, B. Soree, G. Groeseneken, and K. D. Meyer, "Direct and Indirect Band-to-Band Tunneling in Germanium-Based TFETs", *IEEE Transactions on Electron Devices*, vol. 59, no. 2, 2012.
- [16] S. K. Kim, W. Y. Choi, "Impact of gate dielectric constant variation on tunnel field-effect transistors (TFETs)," *Solid-State Electronics*, vol. 116, pp.88~94, 2016.
- [17] S. W. Kim, W. Y. Choi, M. C. Sun, and B. G. Park, "Investigation on the Corner Effect of L-Shaped Tunneling Field-Effect Transistors and Their Fabrication Method", *Journal of Nanoscience and Nanotechnology*, vol. 13, no. 9, 2013.



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