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# Electrical Characteristics of $SiO_2$/4H-SiC Metal-oxide-semiconductor Capacitors with Low-temperature Atomic Layer Deposited $SiO_2$

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***Abstract*—4H-SiC has attracted attention for high-power and high-temperature metal-oxide-semiconductor field-effect transistors (MOSFETs) for industrial and automotive applications. The gate oxide in the 4H-SiC MOS system is important for switching operations. Above 1000°C, thermal oxidation initiates $SiO_2$ layer formation on SiC; this is one advantage of 4H-SiC compared with other wide band-gap materials. However, if post-deposition annealing is not applied, thermally grown $SiO_2$ on 4H-SiC is limited by high oxide charges due to carbon clusters at the SiC/$SiO_2$ interface and near-interface states in $SiO_2$; this can be resolved via low-temperature deposition. In this study, low-temperature $SiO_2$ deposition on a Si substrate was optimized for $SiO_2$/4H-SiC MOS capacitor fabrication; oxide formation proceeded without the need for post-deposition annealing. The $SiO_2$/4H-SiC MOS capacitor samples demonstrated stable capacitance–voltage (*C–V*) characteristics, low voltage hysteresis, and a high breakdown field. Optimization of the treatment process is expected to further decrease the effective oxide charge density.**

***Index Terms*—C-V, effective oxide charge density, gate leakage current, hysteresis, MOS, SiC, $SiO_2$**

## I. INTRODUCTION

Power semiconductor devices deliver or convert power flow; the cell density and power dissipation of power devices have steadily improved to reduce energy loss [1]. However, further improvement in the electrical characteristics of Si-based power devices, such as metal-oxide-semiconductor field-effect transistors (MOSFETs) and insulated gate bipolar transistors, has been restricted by the material limit of Si [2, 3]. This limit can be overcome using wide band-gap semiconductors. These wide band-gap materials have a high critical field, which enables a higher breakdown voltage at the same drift thickness, or a thinner drift layer at an identical breakdown voltage, compared with conventional Si. A thinner drift layer also decreases the on-resistance and power loss. Wide band-gap materials also have a low intrinsic carrier concentration even at high temperatures, which provides reliable operation.

One wide band-gap material, 4H-SiC, has an energy band gap of 3.26 eV [4] and a critical field of 2.8 MV/cm at a doping concentration of $3\times10^{16}$ /cm$^3$ when the electric field is parallel to the *c*-axis [5]. The intrinsic carrier concentration of 4H-SiC is only several $10^{-9}$ /cm$^3$ at room temperature; as such, 4H-SiC MOSFETs have attracted attention for hybrid vehicles, power supplies, and power distribution. The gate oxide in MOSFETs is important with regards to switching operations between on and off states. A $SiO_2$ gate oxide for a 4H-SiC MOS

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system has been grown in a high-temperature furnace [6-9]; however, post-deposition annealing was required, as the interface between $SiO_2$ and 4H-SiC showed considerable limitations including low field-effect mobility and high gate leakage current. A high oxide charge density on $SiO_2$/4H-SiC has been reported, resulting from carbon clusters and near-interfacial oxide defects [10]. There have been numerous reports on the deposition of the gate oxide for a 4H-SiC MOS system [11-13].

The purpose of this work was to report the electrical characteristics of $SiO_2$/4H-SiC MOS capacitors in which the gate oxide was formed under low-temperature $SiO_2$ deposition. Using this low-temperature approach, carbon cluster formation was suppressed, without the need for high-temperature post-deposition annealing. The capacitance–voltage ($C$–$V$) characteristics and gate leakage currents of the $SiO_2$/Si MOS capacitors were measured and analyzed, and the flat-band voltage ($V_{FB}$) and effective oxide charge density ($Q_{eff}$) values were extracted and compared to theoretical values.

## II. Fabrication

The MOS capacitors were fabricated on a 4H-SiC $N$-epitaxial layer on the Si-face of the 4H-SiC $N$+ substrate. The doping concentration and thickness of the $N$-epitaxial layer were $1.75\times10^{15}$/cm$^3$ and 15 μm, respectively. The resistivity of the $N$+ substrate was 19 mΩ-cm. The 4H-SiC was cleaned in a piranha solution of 4:1 $H_2SO_4$:$H_2O_2$. The native oxide on the surface was etched using dilute HF, and then the 4H-SiC was fully rinsed with deionized water.

For the formation of the gate oxide, $SiO_2$ was deposited on 4H-SiC using atomic layer deposition (ALD). The working pressure for the deposition was 100 mTorr and the number of ALD cycles was 160. The deposition temperature was less than 200°C. The thickness of the $SiO_2$ layer was about 16–17 nm. For the gate contact, 100-nm-thick TiN was sputtered and annealed at 400°C in flowing forming gas (5% $H_2$/95% $N_2$) for 30 min. It has been reported that forming gas annealing reduces the interface state density due to hydrogen passivation [13, 14]; this process also improves contact adhesion. Finally, 300-nm-thick aluminum was sputtered on the backside for ohmic contact.

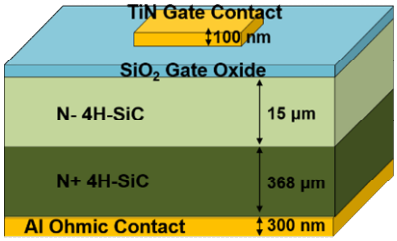


**Fig. 1.** Cross-sectional view of the $SiO_2$/4H-SiC metal-oxide-semiconductor (MOS).

Fig. 1 shows a cross-sectional view of the $SiO_2$/4H-SiC MOS capacitor; $SiO_2$/Si MOS capacitors were also fabricated using the same process for comparison. The doping concentration of the $n$-type Si was about $10^{15}$ cm$^{-3}$ and the area of the gate contact was measured for all devices using a microscope. The measured areas of the $SiO_2$/Si and $SiO_2$/4H-SiC MOS capacitors were $4.18\times10^{-4}$ and $3.28\times10^{-4}$ cm$^2$, respectively. The $C$–$V$ characteristics of the devices were measured at 10 kHz, 100 kHz, and 1 MHz, respectively, under the $C_pR_p$ mode of an Agilent E4980A LCR meter. The gate leakage current and breakdown field were measured using a HP4156A instrument.

## III. Result and Discussion

The electrical characteristics of the $SiO_2$/Si MOS capacitors were analyzed. The measured $C$–$V$ characteristics of the $SiO_2$/Si MOS system are shown in Fig. 2. The gate voltage cycled between 2 V and −2 V in steps of 0.1 V. The measured thickness of the gate oxide was 16.3 nm using ellipsometry. The voltage hysteresis at $10^{-7}$ F/cm$^2$ was 1.9, 2.9, and 4.2 mV under measurements at 10 kHz, 100 kHz, and 1 MHz, respectively, and the $C$–$V$ curves of the $SiO_2$/Si MOS capacitors were stable with low voltage hysteresis. Voltage hysteresis is caused by oxide, fixed, and interface states, based on MOS physics. Fig. 3 shows the measured gate leakage current of the $SiO_2$/Si MOS; the measured breakdown voltage and field were 14.4 V and 8.820 MV/cm, respectively. The high breakdown field and low leakage current indicate superior performance, even though the deposition temperature of the gate oxide was less than 200°C.

After optimizing the $SiO_2$ deposition, we investigated the $SiO_2$/4H-SiC MOS capacitor. Fig. 4 shows the measured $C$–$V$ characteristics of the $SiO_2$/4H-SiC MOS

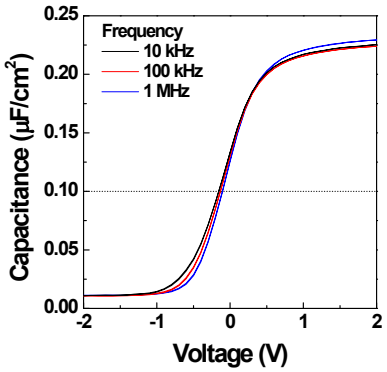


**Fig. 2.** Measured capacitance–voltage ($C$–$V$) of $SiO_2$/Si MOS at 10 kHz, 100 kHz, and 1 MHz.

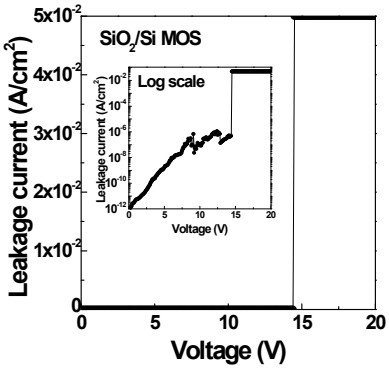


**Fig. 3.** Measured gate leakage current of $SiO_2$/Si MOS.

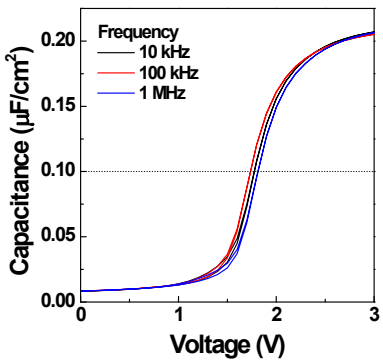


**Fig. 4.** Measured C-V of $SiO_2$/4H-SiC MOS at 10 kHz, 100 kHz, and 1 MHz.

system. The gate voltage cycled between 3 V and 0 V in 0.1-V steps. The capacitive equivalent thickness was 16.8 nm using the accumulation capacitance at 100 kHz. The measured voltage hysteresis values at $10^{-7}$ F/cm$^2$ were 3.7, 0.3, and 1.6 mV under 10 kHz, 100 kHz, and 1 MHz, respectively. Notably, the voltage hysteresis was less than 1 mV at 100 kHz for a gate-oxide deposition temperature of <200°C; this was attributed to the suppression of carbon cluster formation. As such, $SiO_2$/4H-SiC fabricated under low-temperature annealing conditions is a good candidate for a gate oxide in $SiO_2$/Si MOS capacitors.

It is widely known that $V_{FB}$ indicates zero band bending and no space charge; however, experimental values of $V_{FB}$ have not typically been identical to theoretical $V_{FB}$ values due to effective oxide charges from dangling bonds or defects. The $V_{FB}$ shift is the difference between the theoretical and experimental $V_{FB}$ values. The theoretical $V_{FB}$ value was calculated using the metal work function ($\varphi_m$), energy band-gap ($E_g$), affinity ($\chi$), and the difference between the Fermi level and the intrinsic Fermi level ($\varphi_{fn}$), as shown in the following equation [15]:

$$Theoretical\,V_{FB} = \varnothing_m - \left( \chi + \frac{E_g}{2} - \varnothing_{fn} \right) \quad (1)$$

The experimental $V_{FB}$ value was extracted from flat band capacitance ($C_{FB}$) measurements [16]; an extracted $C_{FB}$ value of $2.059\times10^{-11}$ F was obtained from the $C$–$V$ characteristics at 100 kHz. The theoretical and experimental $V_{FB}$ values were 0.624 and 1.644 V, respectively; therefore, the $V_{FB}$ shift was 1.020 V in the positive direction. The value of $Q_{eff}$ can be determined using the following equation [16]:

$$Q_{eff} = C_{ox}\left(theoretical\,V_{FB} - experimental\,V_{FB}\right) \quad (2)$$

where $C_{ox}$ is the oxide capacitance at accumulation. $Q_{eff}$ was $-1.300\times10^{12}$ /cm$^2$ from the $C$–$V$ characteristics at 100 kHz. A negative value for $Q_{eff}$ means that the trapped charges at the oxide and interface states are electrons; these states are acceptor-like and can capture an electron to become negatively charged [12]. Carbon clusters at the $SiO_2$/4H-SiC interface and near-interfacial states in $SiO_2$ may be the origin of the high $Q_{eff}$ value [10]. It has been reported that near-interfacial states have a slow response.

Another method for extracting $V_{FB}$, using the Mott–Schottky equation, was attempted [17-19]. The $x$-axis intercept from the $1/C^2$-gate voltage curve provides the experimental $V_{FB}$ value [19]. From the Mott–Schottky equation, values of $V_{FB}$ and $Q_{eff}$ of 1.576 V and $-1.213\times10^{12}$ /cm$^2$, respectively, were obtained, from identical $C$–$V$ characteristics at 100 kHz. The difference

**Table 1.** Extracted parameters of $SiO_2$/Si and $SiO_2$/4H-SiC MOS

| | $SiO_2$/Si MOS | $SiO_2$/4H-SiC MOS |
|---|---|---|
| Theoretical $V_{FB}$ | 0.168 V | 0.624 V |
| Measured $V_{FB}$ | -0.349 V | 1.644 V |
| $C_{FB}$ | $2.338\times10^{-11}$ F | $2.059\times10^{-11}$ F |
| $Q_{eff}$ | $7.236\times10^{11}$ /cm$^2$ | $-1.300\times10^{12}$ /cm$^2$ |

between the extracted $V_{FB}$ values using the two methods was small.

Table 1 shows a summary of $V_{FB}$, $C_{FB}$, and $Q_{eff}$ values for both the $SiO_2$/Si and $SiO_2$/4H-SiC MOS systems. The value of $Q_{eff}$ was higher than the reported value ($10^{11}$ /cm$^2$) [20], because $SiO_2$ deposited at a low temperature has more structural defects compared with a thermally oxidized system. Notwithstanding, using the same deposition method for the gate oxide, $Q_{eff}$ for the $SiO_2$/4H-SiC MOS was higher than that for the $SiO_2$/Si MOS.

The threshold voltage ($V_{TN}$) is an important parameter for designing 4H-SiC MOSFETs; $V_{TN}$ for an *n*-type semiconductor is given by

$$V_{TN} = \frac{\left|Q'_{SD(max)}\right|}{C_{ox}} + V_{FB} - 2\phi_{fn} \tag{3}$$

where $Q'_{SD(max)}$ is the magnitude of the maximum space charge density per unit area of depletion region [15]. The theoretical and experimental $V_{TN}$ values for the 4H-SiC MOS were −2.364 and 1.431 V, respectively; this difference also arises from the distinction between theoretical and experimental $V_{FB}$ values.

The extracted $Q_{eff}$ value of the $SiO_2$/4H-SiC MOS was comparable to or higher than reported values because the $SiO_2$ deposition temperature was less than that used in the literature [11, 12, 21]. Furthermore, no post-deposition annealing was used during the fabrication procedure. The stable *C–V* characteristics and low-voltage hysteresis reported here are significant. We expect that an optimized processing treatment will further decrease the effective oxide charges of 4H-SiC MOSs.

The gate leakage of a 4H-SiC MOS system is critical because this can increase off-state power loss and cause reliability problems during switching operation. Fig. 5 shows the measured gate leakage current of the $SiO_2$/4H-SiC MOS. The fabricated device exhibited breakdown at

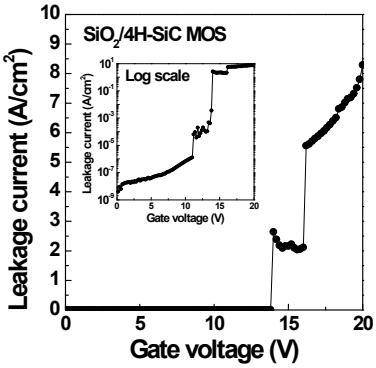


**Fig. 5.** Measured gate leakage current of $SiO_2$/4H-SiC MOS.

13.8 V with suppressed leakage current. The gate breakdown field of $SiO_2$/4H-SiC was 8.178 MV/cm; this value is comparable to that reported in literature [21], however, still smaller than the gate breakdown field of $SiO_2$/Si of 8.820 MV/cm. This can be explained by the higher $Q_{eff}$ of $SiO_2$/4H-SiC compared with that of $SiO_2$/Si, as shown in Table 1. The high-density near-interface states in the $SiO_2$ near the conduction band edge of 4H-SiC are responsible for the gate leakage current [10].

## IV. CONCLUSIONS

The results of this study suggest that low-temperature $SiO_2$ deposition shows superior 4H-SiC MOS characteristics without post-deposition annealing. The proposed device can suppress carbon clusters without any high-temperature processing. The $SiO_2$/4H-SiC MOS capacitor achieved low voltage hysteresis of less than 1 mV from the *C–V* characteristics at 100 kHz. The $V_{FB}$ shift and $Q_{eff}$ were 1.020 V and $-1.300\times10^{12}$ /cm$^2$, respectively. The $SiO_2$/Si MOS capacitor was also fabricated using an identical process for comparison. The $Q_{eff}$ value of the $SiO_2$/4H-SiC MOS was higher than that of the $SiO_2$/Si MOS. The gate breakdown fields of the $SiO_2$/Si and $SiO_2$/4H-SiC MOS systems were 8.820 and 8.178 MV/cm, respectively. Optimized treatment is expected to improve the *C–V* characteristics and gate leakage current of the 4H-SiC MOS system.

## ACKNOWLEDGMENTS

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