JOURNAL OF SEMICONDUCTOR TECHNOLOGY AND SCIENCE, VOL.17, NO.2, APRIL, 2017
https://doi.org/10.5573/JSTS.2017.17.2.199
ISSN(Print) 1598-1657
ISSN(Online) 2233-4866

# Mutually-Actuated-Nano-Electromechanical (MA-NEM) Memory Switches for Scalability Improvement

**Ho Moon Lee and Woo Young Choi**

*Abstract*—**Mutually-actuated-nano-electromechanical (MA-NEM) memory switches are proposed for scalability improvement. While conventional NEM memory switches have fixed electrode lines, the proposed MA-NEM memory switches have mutually-actuated cantilever-like electrode lines. Thus, MA-NEM memory switches show smaller deformations of beams in switching. This unique feature of MA-NEM memory switches allows aggressive reduction of the beam length while maintaining nonvolatile property. Also, the scalability of MA-NEM memory switches is confirmed by using finite-element (FE) simulations. MA-NEM memory switches can be promising solutions for reconfigurable logic (RL) circuits.**

*Index Terms*—**Reconfigurable logic, nano-electro-mechanical switch, scalability, CMOS-NEM hybrid circuit, nonvolatility**

## I. INTRODUCTION

Reconfigurable logic (RL) systems such as field-programmable gate arrays (FPGAs) have attracted much attention due to their short time-to-market, design flexibility and re-usability [1-3]. However, in the case of complementary-metal-oxide-semiconductor (CMOS)-only RL systems, it is difficult to minimize the power consumption and chip area [4, 5]. In order to address these problems, RL systems replacing MOS field-effect transistors (FETs) in routing blocks (RBs) by nano-electromechanical (NEM) memory switches have been researched intensively [6-8]. CMOS-NEM hybrid RL systems can achieve low power consumption and high data signal transfer speed with large chip density thanks to the zero leakage current, three-dimensional (3-D) integration feasibility and nonvolatility of NEM memory switches [6-12].

Conventional cantilever-type NEM-memory-based RL circuits have been proposed and fabricated in our previous work [6]. A cantilever-type NEM memory switch has a movable beam attached to the bit line (BL) and two fixed electrode lines as shown in Fig. 1(a). Although the fabricated cantilever-type NEM memory switches show 1-V pull-in voltage ($V_p$) and 2-V switching voltage ($V_s$), they occupy large area due to long cantilever beam (~ 2900 nm) to achieve the nonvolatile property [6, 13]. Thus, for high-density RL circuits, novel nonvolatile NEM memory structures are needed. In this manuscript, mutually-actuated (MA)-NEM memory switches are proposed as shown in Fig. 1(e). The cantilever-like and movable electrode lines (L1 and L2) distinguish the MA-NEM memory switches from conventional cantilever-type NEM ones. It should be noted that as beam length ($L$) decreases, $V_p$ of NEM devices increases because spring constant ($k$) is proportional to $L^{-3}$ [14]. However, owing to pull-in point shift of the MA-NEM structures, MA-NEM memory switches can achieve shorter $L$ without increasing of $V_p$ compared with cantilever-type memory switches.

In the next section, the difference of pull-in mechanism between cantilever-type and MA-NEM memory switches will be compared. In Section 2, $V_s$,

Manuscript received Aug. 24, 2016; accepted Oct. 9, 2016
A part of this work was presented in Asia-Pacific Workshop on Fundamentals and Applications of Advanced Semiconductor Devices, Hakodate in Japan, Jul. 2016.
Department of Electronic Engineering, Sogang University, 35 Baekbeom-ro (Sinsu-dong), Mapo-gu, Seoul 04107, Korea
E-mail : wchoi@sogang.ac.kr

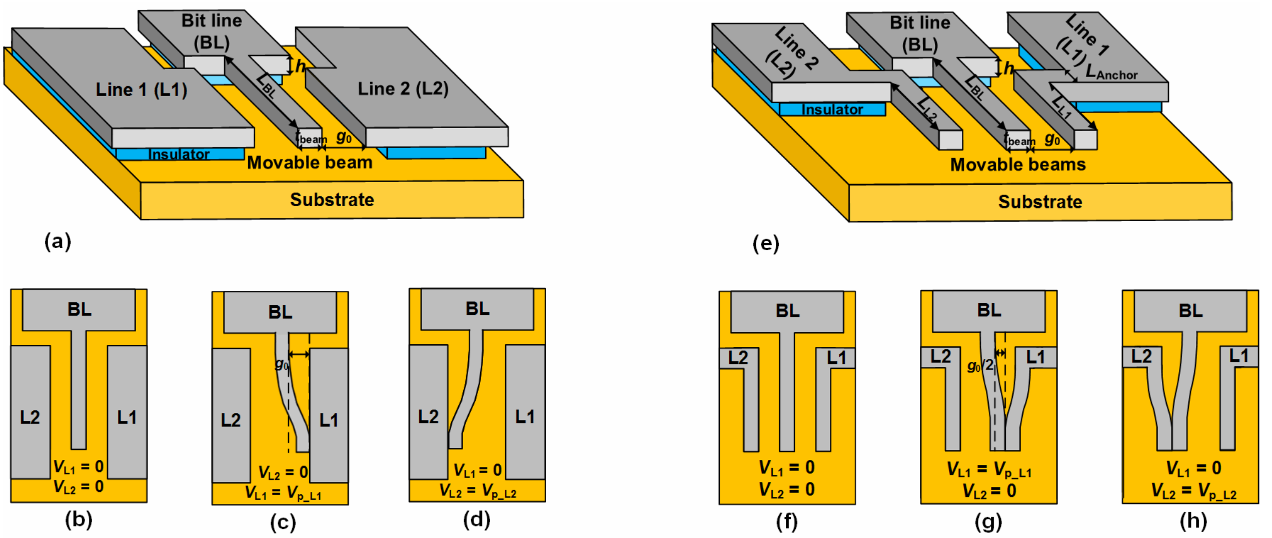


**Fig. 1**. (a) Schematic of the conventional cantilever-type NEM memory switch. Its top view in (b) initial state, (c) state 1 and (d) state 2, (e) Schematic of the proposed MA-NEM memory switch. Its top view in (f) initial state, (g) state 1 and (h) state 2. 0 V is applied to BL for all cases.

release voltage ($V_r$) and $V_p$, of cantilever-type and MA-NEM memory switches will be compared by using finite-element (FE) simulation. In Section 3, the scalability of each NEM memory structure will be discussed.

## II. Pull-in Mechanism

As a brief description of operation mechanism, $V_p$ of simple-parallel-plate model is given by [14]

$$V_p = \sqrt{\frac{2k(g_0 - x_{p\_BL} - x_{p\_L1})^2 x_{p\_BL}}{\varepsilon_0 A}} \qquad (1)$$

where $\varepsilon_0$ is the vacuum permittivity, $A$ is the area of a parallel plate, $x_{p\_BL}$ and $x_{p\_L1}$ are the pull-in point of BL and L1 respectively. $x_{p\_L1}$ of cantilever-type devices should be zero due to the fixed L1 and L2. On the other hand, $x_{p\_L1}$ of MA-NEM devices is equal to $x_{p\_BL}$ because the physical dimensions of movable lines are the same. Now, $V_p$ reduction can be explained as follows: Fig. 1(b) and (f) show the initial states of the cantilever-type and MA-NEM cell, respectively. When positive voltage is applied to L1 ($V_{L1}$>0) of the cantilever-type NEM device, the movable BL is pulled onto the fixed L1 due to the electrostatic force. When the BL reaches $x_{p\_BL}$, which is given by $g_0/3$ for the cantilever-type NEM device [14], the BL is attached to L1 as shown in Fig. 1(c). On the other hand, mutually-actuated movable BL and L1 of MA-NEM memory switches attract each other when $V_{L1}$>0. Also, the pull-in of MA-NEM memory switches occurs when both $x_{p\_BL}$ and $x_{p\_L1}$ are $g_0/6$. Thus, the proposed MA-NEM memory switches can achieve $\times(0.5)^{1/2}$ lower $V_p$ than conventional cantilever-type NEM devices. The switching between BL and L2 is the same as that between BL and L1 as shown in Fig. 1(d) and (h). Surface adhesion force needs to be considered in switching process between state 1 and state 2 [6].

## III. Operation Analysis

FE-simulation is performed for the accurate comparison of operation voltages between conventional cantilever-type NEM and the proposed MA-NEM memory switches. A commercial FE simulator is used: ANSYS. Table 1 summarizes simulation parameters. Copper, which is used for CMOS back-end-of-line (BEOL) process, is assumed for line materials. The electrode lines of NEM devices are assumed to have a symmetric structure. Thus, the physical dimensions of movable electrode lines are set to be identical with those of the BL beam.

Fig. 2 shows FE-simulated voltages *vs.* beam maximum deformation. Simulated $V_p$ of the cantilever-type NEM device ($V_{p\_cantilever}$) and that of the MA-NEM ($V_{p\_MA\text{-}NEM}$) device are extracted to be 2.91 V and 2.05 V,

**Table 1.** Used device parameters

| | |
|---|---|
| Young's modulus of material ($E$) | 110 Gpa |
| Poisson ratio | 0.34 |
| Thickness of three beams ($t_{beam}$) | 65 nm |
| Initial gap ($g_0$) | 65 nm |
| Length of beams ($L_{BL} = L_{L1} = L_{L2}$) | 2420 nm |
| Length of electrode anchors ($L_{Anchor}$) | 0 nm |
| Height of metal lines ($h$) | 180 nm |
| RMS surface roughness | 3 nm [16] |
| Surface adhesion force per unit area ($P$) | 0.03 μN/μm$^2$ [17] |

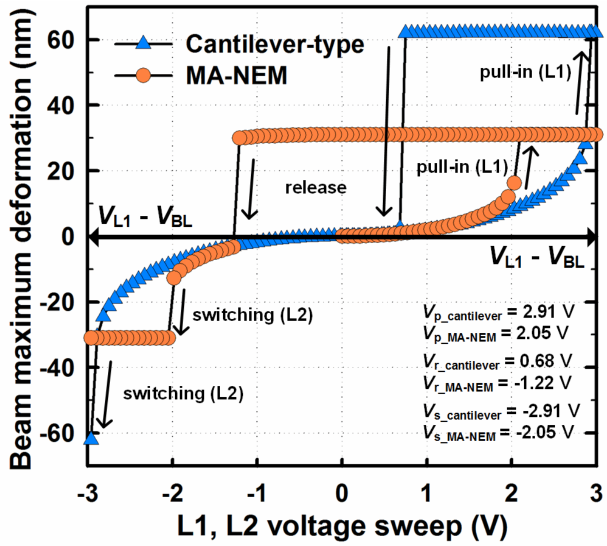


**Fig. 2.** Comparison of the beam maximum deformation versus voltages in steady state for cantilever-type NEM and that for the MA-NEM memory switch.

respectively. Thus, their ratio ($V_{p\_MA\text{-}NEM}/V_{p\_cantilever}$) is ~0.70, which is close to $(0.5)^{1/2}$. On the other hand, $V_r$ of cantilever-type ($V_{r\_cantilever}$) and MA-NEM devices ($V_{r\_MA\text{-}NEM}$) are 0.68 V and -1.22 V, respectively. It should be noted that if NEM memory devices maintain state 1 without applied voltage, $V_r$ is determined by the restoring force ($F_r$), electrostatic force ($F_e$) and surface adhesion force ($F_{ad}$) which are given by [14]

$$F_r = \frac{2Et_{beam}^3 h}{3L_{BL}^3} x_{BL} \quad (2a)$$

$$F_e = \frac{\varepsilon_0 h L_{BL} V_{L2}^2}{2x_{L2}^2} \quad (2b)$$

$$F_{ad} = P\alpha h L_{BL} \quad (2c)$$

where $x_{L2}$ is the distance between BL and L2. Note that $x_{L2}$ of the cantilever-type NEM device is $2g_0$ while that of the MA-NEM memory switch is $3g_0/2$. $V_{L2}$ is the applied

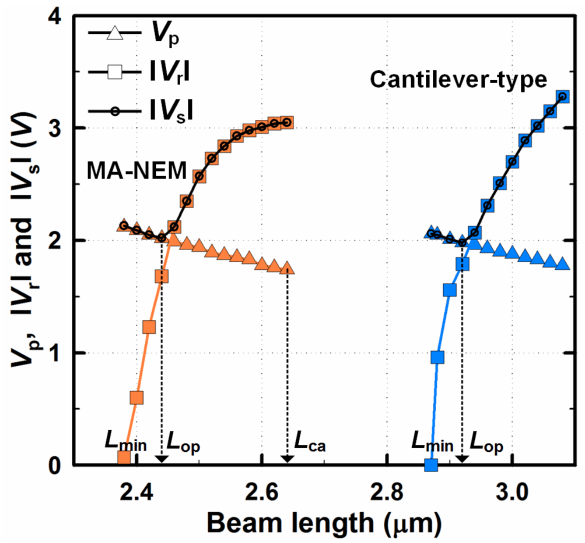


**Fig. 3.** Simulated $V_p$, $|V_r|$ and $|V_s|$ versus length scaling for the MA-NEM and that for cantilever-type NEM memory switch.

voltage to L2 line. α in (2c) is the contact ratio of BL beam and it is assumed to be 0.3 for simple discussion [15]. Other notations are summarized in Table 1. NEM memory switches can maintain nonvolatile property as long as $F_{ad}$ is equal to $F_r$ while $F_e$ is zero. Thus, increasing $L_{BL}$, which is undesirable in terms of density, is the most effective way of achieving nonvolatile NEM memory switches. According to the Hook's law, $F_r$ is a multiplication of spring constant and deformation of BL beam ($x_{BL}$). (2a) shows $F_r$ of the cantilever beam is proportional to $x_{BL}/(L_{BL})^3$. When cantilever-type NEM memory switches stay in state 1 or state 2, $x_{BL}$ of the BL beam becomes $g_0$, as shown in Fig. 1(c) and (d). However, $x_{BL}$ of the MA-NEM memory switches is $g_0/2$ as shown in Fig. 1(f) and (g). Thus, MA-NEM memory switches can achieve $(0.5)^{(1/4)}$ times smaller $L_{BL}$ than cantilever-type NEM memory switches without losing nonvolatility. Fig. 2 shows that cantilever-type memory switches have volatile property while MA-NEM memory switches have nonvolatile property at the same physical dimensions of beams. $V_s$ of the cantilever-type NEM memory switches ($V_{s\_cantilever}$) and that of the MA-NEM memory switches ($V_{s\_MA\text{-}NEM}$) between BL and L2 are -2.91 V and -2.05 V, respectively. Note that $|V_{s\_cantilever}|$ and $|V_{s\_MA\text{-}NEM}|$ are the same as $|V_{p\_cantilever}|$ and $|V_{p\_MA\text{-}NEM}|$, respectively. In fact, $|V_s|$ of NEM devices is determined by *max* ($|V_p|$, $|V_r|$), which is highly related to the physical dimensions of beams. It will be discussed in the next section.

## IV. LENGTH SCALABILITY

For high density, $L_{BL}$ should be reduced. Fig. 3 shows $L$ (= $L_{BL}$ = $L_{L1}$ = $L_{L2}$) reduction of cantilever-type and MA-NEM memory switches that operate less than CMOS breakdown voltage considering CMOS-NEM hybrid circuit. In this work, CMOS breakdown voltage is assumed to be 3.3 V [18]. From Fig. 3, some meaningful parameters can be defined: $L_{min}$, $L_{op}$ and $L_{ca}$. First, $L_{min}$ means the minimum $L$ of the NEM devices maintaining nonvolatility. Fig. 3 shows that $L_{min}$ of MA-NEM memory switches can be 15-% smaller than that of cantilever-type NEM memory switches. Second, $L_{op}$ represents the optimized $L$ achieving minimum $|V_s|$. Likewise, MA-NEM memory switches can achieve smaller $L_{op}$ than cantilever-type NEM memory switches. When $L$ is reduced below $L_{op}$, $|V_s|$ increases because it follows $V_p$ which is proportional to $L_{BL}^{-2}$ as mentioned (1) and (2a). Oppositely, when $L$ becomes larger than $L_{op}$, $|V_s|$ increases because it follows $|V_r|$. Moreover, as $L$ increases, $F_r$ decreases rapidly due to the $L^{-3}$ dependency in (2a) while $F_e$ and $F_{ad}$ increase linearly according to (2b) and (2c). Thus, $F_{ad}$ and $F_e$ become dominant to describe switching operations of NEM memory switches. If $F_r$ becomes zero, in the case of cantilever-type NEM memory switches, $|V_r|$ will be saturated because the $L$ dependency of $F_{ad}$ and $F_e$ are canceled out. On the other hand, in the case of MA-NEM memory switches, all the lines stick together and fail to operate when $F_e + F_r$ is smaller than $F_{ad}$. $L_{ca}$ means the catastrophic length of MA-NEM memory switches. Thus, the length of MA-NEM memory switches should be determined between $L_{min}$ and $L_{ca}$.

## V. CONCLUSIONS

Novel MA-NEM memory switches are proposed and simulated for scalability improvement. It turns out that MA-NEM memory switches can achieve smaller $L_{BL}$ with nonvolatile property than conventional cantilever-type NEM memory switches. Also, by reducing $L$, minimum $|V_s|$ can be obtained at $L_{op}$. Therefore, the proposed MA-NEM memory switch can be a promising solution to highly integrated RL circuits.

## ACKNOWLEDGMENTS

This work was supported in part by the NRF of Korea funded by the MSIP under Grant NRF-2015R1A2A2 A01003565 (Mid-Career Researcher Program), NRF-2015M3A7B7046617 (Fundamental Technology Program), NRF-2016M3A7B4909668 (Nano·Material Technology Development Program) and in part by the MOTIE/KSRC under Grant 10044842 (Future Semiconductor Device Technology Development Program).

## REFERENCES

[1] C. Dong, C. Chen, S. Mitra and D. Chen, “Architecture and performance evaluation of 3D CMOS-NEM FPGA,” SLIP’11 Proceedings of the System Level Interconnect Prediction Workshop, pp.2–9, NJ, USA, Jun. 2011

[2] H. Scott, “The roles of FPGAs in reprogrammable systems.” Proceedings of the IEEE, vol.86, no.4, pp. 615–638, Apr. 1998.

[3] D. E. Van den Bout, J. N. Morris, D. Thomae, S. Labrozzi, S. Wingo and P. Hallman, “Anyboard : An FPGA-based, reconfigurable system,” IEEE Design & Test, pp.21–30, CA, USA, July. 1992.

[4] S. Chong, B. Lee, J Provine, “Integration of nanoelectromechanical (NEM) relays with silicon CMOS with functional CMOS-NEM circuit.” Proceedings of the System Level Interconnect Prediction Workshop. IEEE Press, pp.30.5.1–30.5.4 Washington DC, USA, Dec. 2011

[5] S. Sun and P. G. Y. Tsui, “Limitation of CMOS supply-voltage scaling by MOSFET threshold-voltage variation.” IEEE Journal of Solid-State Circuits, vol.30, no.8, pp. 947–949, Aug. 2002.

[6] Y. J. Kim and W.Y. Choi, “Nonvolatile nanoelectromechanical memory switches for low-power and high-speed field-programmable gate arrays,” IEEE Trans. Electron Devices, vol.62, no.2, pp.673–679, 2015.

[7] W. Y. Choi and Y. J. Kim, “Three-Dimensional Integration of Complementary Metal-Oxide-Semiconductor (CMOS)-Nano-Electromechanical (NEM) Hybrid Reconfigurable Circuits," IEEE Electron Device Letters, vol.36, no.9, pp. 887–889, Sep. 2015.

[8] S. Chong, B. Lee, K. B. Parizi, J. Provine, S. Mitra, R. T. Howe and H.-S. P. Wong, "Integration of nanoelectromechanical (NEM) relays with silicon CMOS with functional CMOS-NEM circuit," Electron Devices Meeting (IEDM), 2011 IEEE International, pp.701–704, DC, USA, Dec. 2011

[9] K. Kimihiko, V. Stojanovic and T.J.K. Liu, "Non-Volatile Nano-Electro-Mechanical Memory for Energy-Efficient Data Searching." IEEE Electron Device Letters, vol.37, no.1, pp. 31–34, Dec. 2015.

[10] P. Singh, G. L. Chua, Y. S. Liang, K. G. Jayaraman, A. T. Do and T. T. Kim, "Anchor-free NEMS non-volatile memory cell for harsh environment data storage." Journal of Micromechanics and Microengineering, vol.24, no.11, p. 115007, Oct. 2014.

[11] P. Vincent, G. L. Chua, R. Vaddi, J. M. Tsai and T. T. Kim, "The shuttle nanoelectromechanical nonvolatile memory." IEEE Electron Device Society, vol.23, no.4, pp. 1137–1143, Jan. 2012.

[12] B. W. Soon, E. J. Ng, Y. Qian, N. Singh, M. J. Tsai and C. Lee, "A bi-stable nanoelectromechanical non-volatile memory based on van der Waals force." Applied Physics Letters, vol.103, no.5, p. 053122, Feb. 2013.

[13] M. P. Boer and T. A. Michalske, "Accurate method for determining adhesion of cantilever beams." Journal of Applied physics, vol.82, no.2, pp. 817–827, July. 1999.

[14] G. M. Rebeiz, RF MEMS: Theory, design, and technology, 1st ed., Wiley, New York, 2003.

[15] J. A. Knapp, and M. P. Boer, "Mechanics of Microcantilever Beams Subject to Combined Electrostatic and Adhesive Forces," J. Microelectromech. Syst., vol.11, no.6, pp.754–764, 2002.

[16] J. Yaung, L. Hutin, J. Jeon, and T. J. K. Liu, "Adhesive force characterization for MEM logic relays with sub-micron contacting regions," J. Microelectromech. Syst., vol.23, no.1, pp.198–203, 2014.

[17] D. Lee, V. Pott, H. Kam, R. Natanael, and T. J. K. Liu, "AFM chracteriztion of adhesion force in micro-relays," Micro Electro Mechanical Systems (MEMS), 2010 IEEE 23rd International Conference on, pp.232–235, Wanchai, Hong Kong, Jan, 2010

[18] G. Boselli, V. Reddy and C. Duvvury, "Latch-up in 65nm CMOS technology: a scaling perspective." Reliability Physics Symposium, 2005. Proceedings. 43rd Annual, Dallas, USA, pp.137–144, Apr. 2005.

**Ho Moon Lee** was born in Seoul, in 1990. He received the B.S. degree in 2016 from Sogang University, Seoul, Korea. He is currently working toward the M.S. degree in the Department of Electronic Engineering, Sogang University, Seoul, Korea. His current research interests include nanoelectromechanical (NEM) relays/memory cell.

**Woo Young Choi** received the B.S., M.S. and Ph. D. degrees in the School of Electrical Engineering from Seoul National University, Seoul, Korea in 2000, 2002 and 2006, respectively. From 2006 to 2008, he was with the Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, USA as a post-doctor. Since 2008, he has been a member of the faculty of Sogang University (Seoul, Korea), where he is currently an Associate Professor with the Department of Electronic Engineering. He has authored or coauthored over 180 papers in international journals and conference proceedings and holds 35 Korean patents. His current research interests include fabrication, modeling, characterization and measurement of CMOS/CMOS-compatible semiconductor devices and nanoelectro-mechanical (NEM) relays/memory cell.