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Optimization of Double Gate Vertical Channel Tunneling Field Effect Transistor (DVTFET) with Dielectric Sidewall

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Abstract—**In this paper, we propose a novel double gate vertical channel tunneling field effect transistor (DVTFET) with a dielectric sidewall and optimization characteristics. The dielectric sidewall is applied to the gate region to reduced ambipolar voltage (V_{amb}) and double gate structure is applied to improve on-current (I_{ON}) and subthreshold swing (SS). We discussed the fin width (W_S), body doping concentration, sidewall width (W_{side}), drain and gate underlap distance (X_d), source doping distance (X_S) and pocket doping length (X_P) of DVTFET. Each of device performance is investigated with various device parameter variations. To maximize device performance, we apply the optimum values obtained in the above discussion of a optimization simulation. The optimum results are steep SS of 32.6 mV/dec, high I_{ON} of 1.2×10^{-3} A/μ m and low V_{amb} of -2.0 V.**

Index Terms—**Tunneling fieldeffect transistor, double gate, dielectric sidewall, vertical channel, semiconductor optimization**

I. INTRODUCTION

In recent years, tunnel field-effect transistor (TFET) has attracted substantial attentions for low-power applications to overcome the limitations of nanoscale complementary metal-oxide-semiconductor (CMOS) devices [1, 2]. The TFET possesses a distinct operation mechanism, known as band to band tunneling (BTBT), enables TFETs to achieve steep subthreshold swing (SS) [3, 4]. Moreover, TFETs have been considered as the most promising candidates for low power applications because of their compatibility with CMOS technology [5]. However, improvements in low on-current (I_{ON}) and ambipolar characteristics (V_{amb}) (i.e. ambipolar characteristics are evaluated with ambipolar voltage V_{amb} at V_d = 1 V and I_d = 10^{-7} A/μm.) are significant challenges in the TFET development [6-8]. In our previous works, a novel dielectric sidewall structure is proposed to reduce the V_{amb} of vertical channel tunneling field effect transistor (VTFET) [9]. However, improvement in I_{ON} and SS could not be achieved, due to the use of a single gate. Therefore, double gate with high-k dielectric structure can be applied for improvement in I_{ON}, while taking advantage of the reduced SS also [7, 10]. In this paper, we propose a double gate VTFET structure with dielectric sidewall and optimization methods. Comparing with conventional VTFET, double gate vertical channel tunneling field effect transistor (DVTFET) has additional device parameters including fin width. Extensive study of TFET with dielectric sidewall is investigated with device simulation for optimization of device performance

II. SIMULATION STRUCTURE

Fig. 1 shows schematic diagram of double gate TFET with dielectric sidewall. Basically the suggested device

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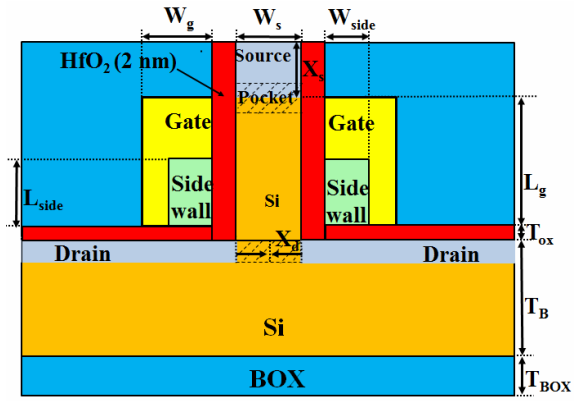


Fig. 1. Schematic of double gate TFET with dielectric sidewall and device parameters.

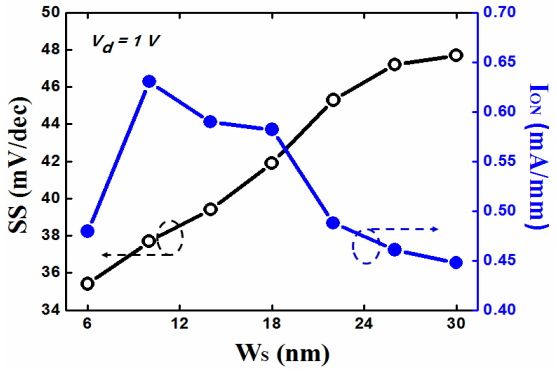
Table 1. List of device parameters in simulation structure

Parameter	Default Value
Source width (W_s)	10 nm
Gate width (W_g)	10 nm
Gate length (L_g)	100 nm
Sidewall width (W_{side})	3 nm
Sidewall length (L_{side})	35 nm
Dielectric thickness (T_{ox})	2 nm
Body thickness (T_B)	70 nm
BOX thickness (T_{BOX})	20 nm
Source doping distance (X_S)	38 nm
Drain-gate underlap (X_d)	0 nm
Pocket doping length (X_P)	0 nm
Source doping concentration(N_S)	10^{20} cm^{-3}
Drain doping concentration (N_D)	10^{20} cm^{-3}
Body doping concentration (N_B)	10^{17} cm^{-3}

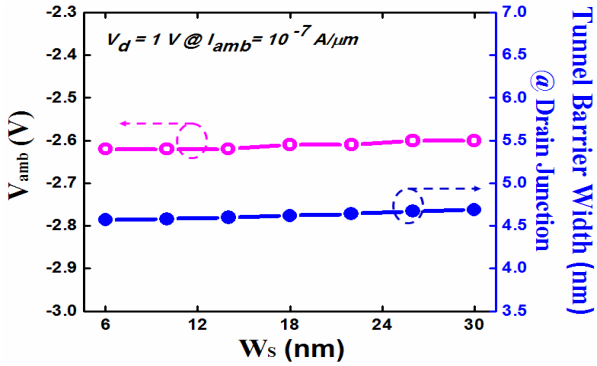
has a vertical p-channel and a Si_3N_4 dielectric sidewalls layer in the gate region besides HfO_2 gate dielectric. Moreover, we applied n-type pocket doping below the source in the subsequent optimization simulation [15]. The parameters used in our simulations are listed in Table 1. All DVTFETs simulated here use a n-type polysilicon gate work function of 4.17 eV. Device performance has been investigated with SILVACO ATLAS simulator [11]. Tunneling current simulations were performed with nonlocal band-to-band tunneling, band gap narrowing, reverse bias band to band tunneling and quantum tunneling direction models as same in the previous work [9].

III. Simulation and Discussion

Fig. 2(a) shows SS and I_{ON} characteristics with source



(a)



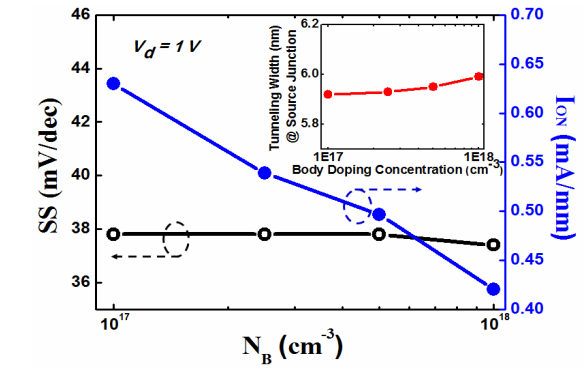
(b)

Fig. 2. W_S scaling characteristics (V_d = 1 V) (a) SS and I_{ON} characteristics, (b) V_{amb} and W_{tunnel} at drain junction.

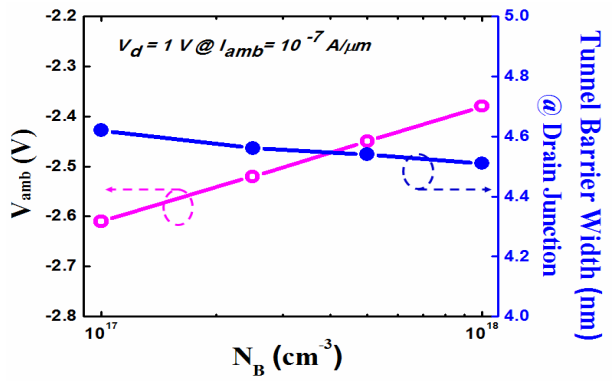
width (W_S) scaling down. In this work, W_S means fin width for double gate structure. SS is improved with W_S reduction due to the enhancement of gate controllability. When W_S is reduced below 10 nm, possible cross section area for current flow reduces decreasing I_{ON} [7]. Since the V_{amb} of TFET is mainly determined by gate electric field in drain junction. Reduction in W_S has a negligible effect on V_{amb} as shown in Fig. 2(b). V_{amb} is also studied by tunneling barrier measurements in drain junction.

When the body doping concentration (N_B) is changed from 10^{17} cm^{-3} to 10^{18} cm^{-3}, SS is not changed while I_{ON} significantly decreases as shown in Fig. 3(a). Since the W_{tunnel} is increased at source junction, I_{ON} is slightly reduced by N_B decrease as shown in Fig. 3(a) inset. V_{amb} is also reduced with N_B decrease as shown in Fig. 3(b). Considering these results, optimized N_B is 10^{17} cm^{-3} in this parameter range.

SS and I_{ON} characteristics with sidewall width (W_{side}) variation as shown in Fig. 4(a). Since the SS is determined by capacitance between the gate and channel in source region, SS has a fixed value with W_{side}



(a)

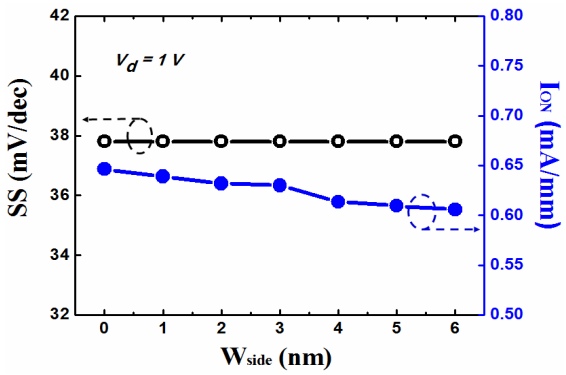


(b)

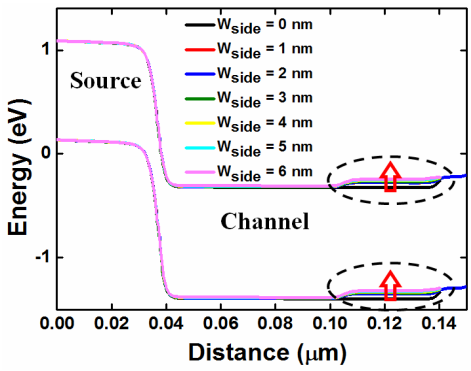
Fig. 3. Optimization with N_B concentration variation (a) SS and I_{ON} characteristics, W_{tunnel} at source junction (inset), (b) V_{amb} and W_{tunnel} at drain junction.

variation [9]. I_{ON} is decreased due to the increase of energy band valley at the channel region as shown in Fig. 4(b). In the drain region, the gate controllability is decreased with reduction of capacitance between the gate and channel which in turns decrease the V_{amb} as shown in Fig. 4(c).

As shown in Fig. 5(a), I_{ON} is increased and SS is not changed with drain underlap (X_d) increase. This result is explained by change of the tunneling direction near by drain junction and channel length reduction. In this case, I_{ON} is determined by the channel resistance not by the p-n tunnel barrier [13]. In addition, channel cross section area of current flow is increased with X_d as shown in Fig. 5(b). The electron density in the channel is proportional to drain and gate underlap length. Since the capacitance between the gate and channel is not changed, SS has a fixed value. When the drain underlap from the sidewall dielectric is increased, the gate controllability is decreased at drain junction. Tunneling width (W_{tunnel}) is increased and V_{amb} is reduced as shown in Fig. 5(c).



(a)



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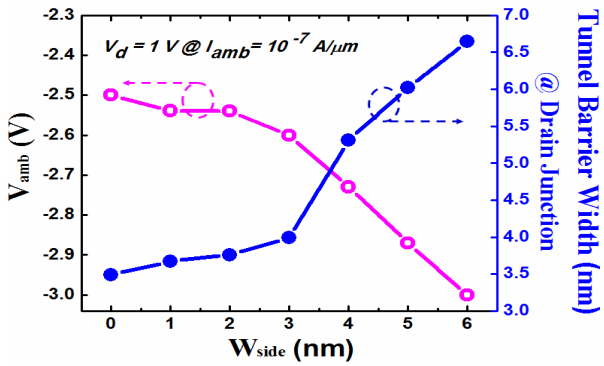


(c)

Fig. 4. Optimization with W_{side} variation (a) SS and I_{ON} characteristics, (b) energy band at source junction, (c) V_{amb} and W_{tunnel} at drain junction.

In this DVTFET structure, the initial position of the source doping distance is 38 nm from the top surface as shown in Fig. 6(a). (i. e. X_s is 38 nm). When the X_s is changed from X_s = 35 nm to X_s = 41 nm, variation of SS and I_{ON} are shown in Fig. 6(a). From the result in Fig. 6(a), I_{ON} and SS has optimum point at X_s = 37 nm. A – A' region is location in source region as shown in Fig. 6(b) inset and Fig. 6(b) indicates carrier concentration in A-A' region. When X_S is 37 nm, the electron

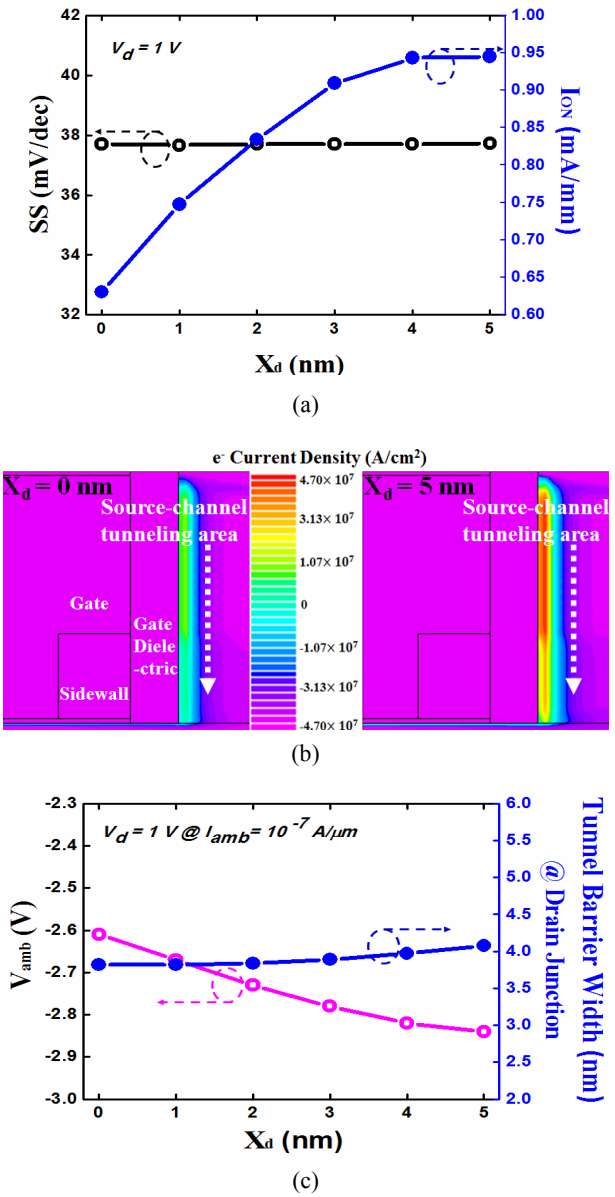


Fig. 5. Optimization with X_d variation (a) SS and I_{ON} characteristics, (b) the electron current density of X_d = 0 nm and X_d = 5 nm, (c) V_{amb} and W_{tunnel} at source junction.

concentration has maximum value within the tunneling region as shown in Fig. 6(b) [14]. Variation of source doping distance at source junction induces no effect on drain junction region as shown in Fig. 6(c).

In order to obtain a high I_{ON}, a heavily n-type doped pocket is applied below the source region. The source pocket structures have been introduced to have a steeper SS and higher I_{ON} comparing with the conventional p-i-n TFETs structure [15]. The n-type pocket can reduce the W_{tunnel} by increasing the electric field across the tunneling junction [16]. The simulation results were

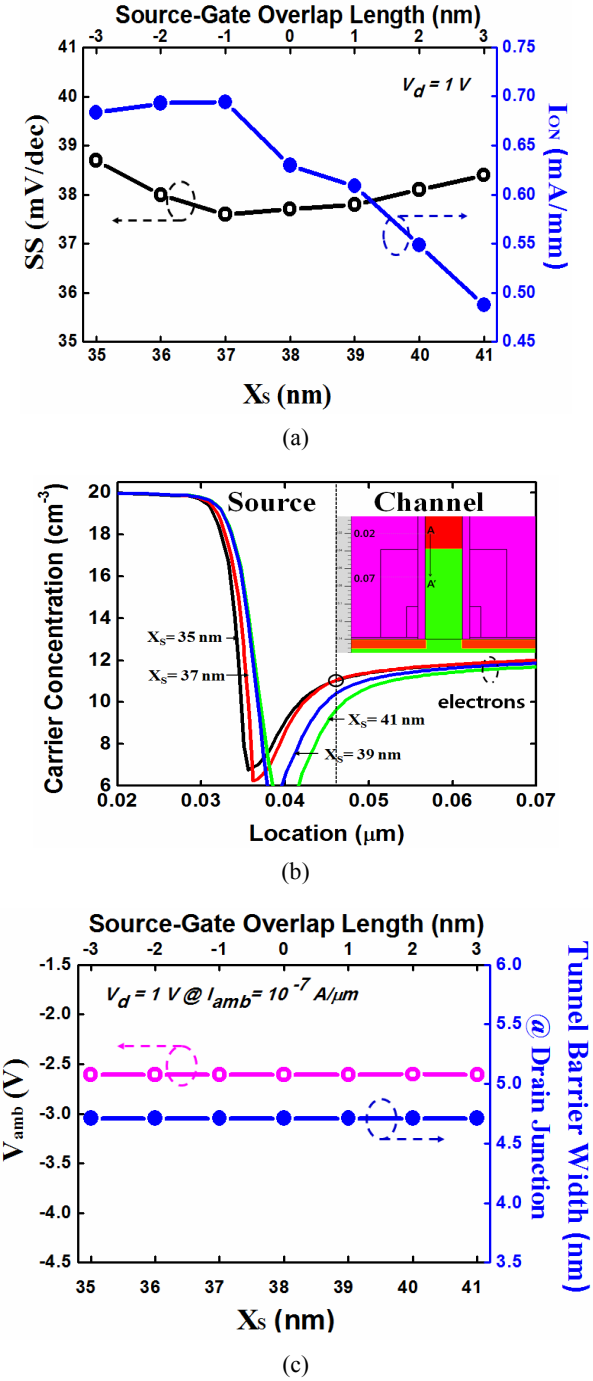
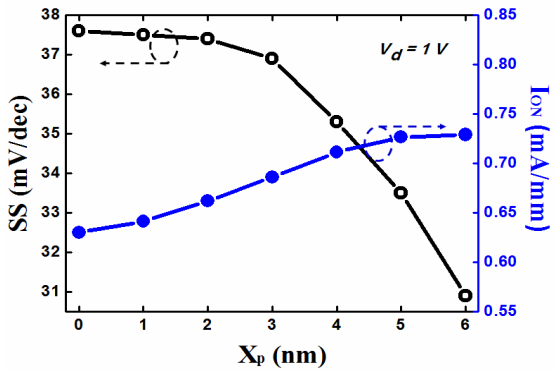


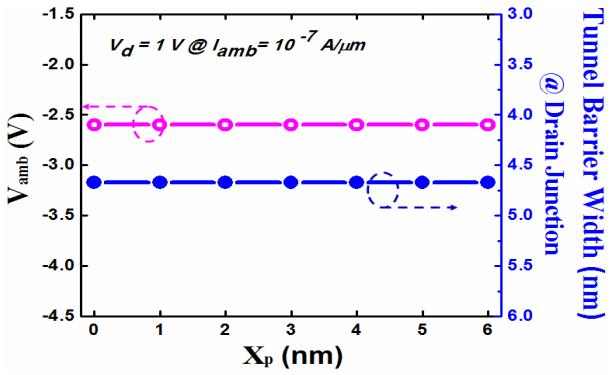
Fig. 6. Optimization with X_s variation (a) SS and I_{ON} characteristics, (b) carrier concentration of source and channel tunneling region, (c) V_{amb} and W_{tunnel} at source junction.

presented in Fig. 7(a). The Fig. 7(b) shows that adding a source pocket has no effect on V_{amb} at the drain junction.

Herein, we performed a comprehensive optimization with previous optimization results. Fig. 8 shows comparison of simulation results for default and optimized values. The optimized values of the simulation



(a)



(b)

Fig. 7. Optimization with X_P variation (a) SS and I_{ON} characteristics, (b) V_{amb} and W_{tunnel} at source junction.

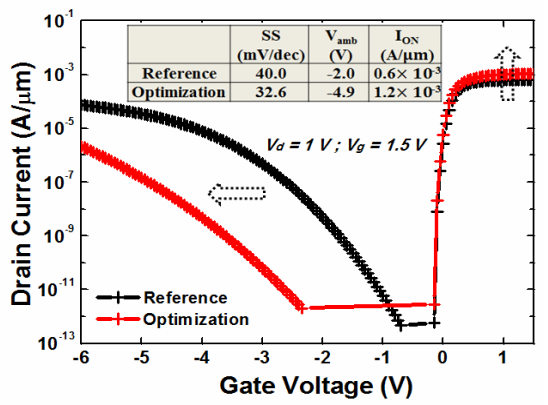


Fig. 8. Transfer characteristics in optimized and default DVTFET.

are sidewall width (W_{side}) is 6 nm, source pocket doping depth (X_S) is 6 nm and doping concentration (N_D) is 10^{19} cm^{-3}, source-gate overlap (X_S) is 37 nm, drain-gate underlap (X_d) is 5 nm respectively. Improvement of performance is summarized in inset table of Fig. 8.

V. Conclusions

In this paper, we proposed the DVTFET with a Si_3N_4 dielectric sidewall and optimizedfor performance improvement. We analyze the influence of device parameters such as fin width, size of dielectric sidewall and pocket doping on the I_{ON}, SS and V_{amb} of DVTFETs. I_{ON} is modulated by W_S, X_d, X_S, X_P and body doping concentration. SS is modulated by W_S, X_d, X_S and X_P. Finally, V_{amb} is modulated by W_{side}, X_d and body doping concentration. The results for optimized structure shows a low SS of 32.6 mV/dec, which means 18.5% reduction as compared with reference structure. I_{ON} is increased from 0.6×10^{-3}A/μm to 1.2×10^{-3} A/μm and V_{amb} is reduced from -2.0 V to -4.9 V. We demonstrated optimization of DVTFET with dielectric sidewall which is attractive device for low power consumption logic applications.

Acknowledgments

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