JOURNAL OF SEMICONDUCTOR TECHNOLOGY AND SCIENCE, VOL.17, NO.2, APRIL, 2017
https://doi.org/10.5573/JSTS.2017.17.2.167

ISSN(Print) 1598-1657
ISSN(Online) 2233-4866

Characterization of the Vertical Position of the Trapped Charge in Charge-trap Flash Memory

Seunghyun Kim[1], Dae Woong Kwon[1], Sang-Ho Lee[1], Sang-Ku Park[1], Youngmin Kim[2], Hyungmin Kim[3], Young Goan Kim[3], Seongjae Cho[2], and Byung-Gook Park[1,*]

***Abstract*—In this paper, the characterization of the vertical position of trapped charges in the charge-trap flash (CTF) memory is performed in the novel CTF memory cell with gate-all-around structure using technology computer-aided design (TCAD) simulation. In the CTF memories, injected charges are not stored in the conductive poly-crystalline silicon layer in the trapping layer such as silicon nitride. Thus, a reliable technique for exactly locating the trapped charges is required for making up an accurate macro-models for CTF memory cells. When a programming operation is performed initially, the injected charges are trapped near the interface between tunneling oxide and trapping nitride layers. However, as the program voltage gets higher and a larger threshold voltage shift is resulted, additional charges are trapped near the blocking oxide interface. Intrinsic properties of nitride including trap density and effective capture cross-sectional area substantially affect the position of charge centroid. By exactly locating the charge centroid from the charge distribution in programmed cells under various operation conditions, the relation between charge centroid and program operation condition is closely investigated.**

***Index Terms*—Charge-trap flash memory, TCAD, macro modeling, silicon nitride, charge centroid, charge distribution**

Manuscript received Jul. 26, 2016; accepted Dec. 11, 2016
[1] Department of Electrical and Computer Engineering with Inter-university Semiconductor Research Center (ISRC), Seoul National University, 1 Gwanak-ro, Gwanak-gu, Seoul 08826, Korea
[2] Department of Electronics Engineering, Gachon University, 1342 Seongnamdaero, Seongnam, Gyeonggi-do 13120, Korea
[3] Novachips, Gyeonggi-do 13511, Korea
E-mail : bgpark@snu.ac.kr

I. INTRODUCTION

Charge-trap flash (CTF) is replacing the floating-gate (FG) flash memory for high-density integration and low-power operation. In the CTF memory cells, the injected charges are not stored in a polycrystalline silicon (poly-Si) conductive layer but in the trapping layer such as silicon nitride (Si_3N_4). The distribution of trapped charges affects the memory operation of individual cells and needs to be considered in constructing the accurate macro models of CTF memory cells. Although several experiment results have been reported in the previous literature [1-5], the relation between charge distribution and device operation has not been clearly studied yet. In this study, we trace the locations of the trapped charges in the CTF memory cell by device simulations and experimental results in cooperation.

II. SIMULATION AND EXPERIMENTS

For device simulation, a gate-all-around (GAA) channel CTF memory cell is designed by a commercial TCAD tool [6]. In order to consider more realistic circumstances than dealing with a single cell, three memory cells are connected in series between one string select line (SSL) and one ground select line (GSL), which make up a short NAND flash bitline (BL) as shown in Fig. 1(a) and (b). Fig. 1(a) and (b) show the circuit symbol of the simple NAND string with three wordlines (WLs) and the simulated structure,

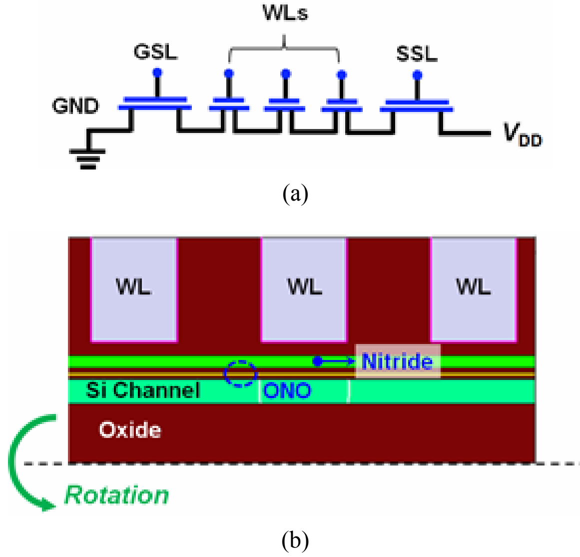


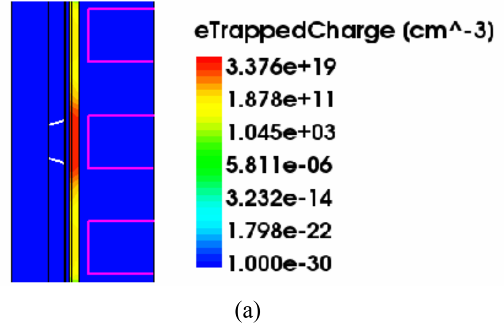
Fig. 1. NAND string used in the simulation (a) Circuit symbol, (b) Simulated structure and materials.

respectively. In the device simulation, the array structure in Fig. 1(b) is rotated about the axis along the bottom (dotted line in the figure) so that the channel is made to be very thin Si shell on the oxide core. Based on the simulated structure, the GAA-channel CTF memory cells have been fabricated. The oxide-nitride-oxide-nitride-oxide (ONONO) dielectric layers have thicknesses of 2/2/2/6/6 nm, from bottom to top. The bottom ONO stack is designed for bandgap engineering (BE) to boost the program and erase (P/E) operation speeds [7, 8]. The diameter of the nanowire channel is 40 nm. Ion implantation was not performed for source and drain (S/D) junctions so that the virtual S/D are formed by the gate-to-channel fringing electric field instead [9-11].

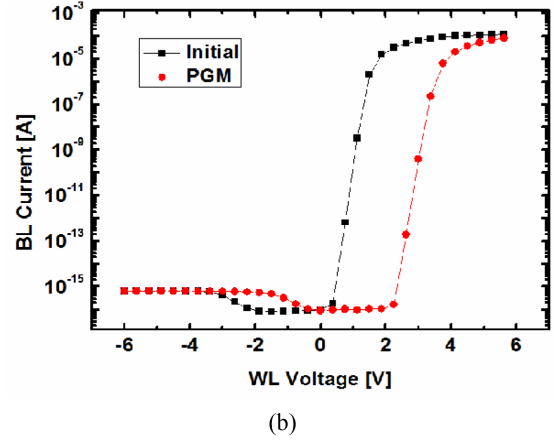
III. Results and Discussion

In order to locate the charge centroid from the relation with charge distribution, the SONONOS CTF memory cells were simulated as shown in Fig. 2(a). Fig. 2(b) shows the transfer curves of the memory cell at the center of the string in Fig. 2(a) before and after the program operation. The charge centroid is calculated from the charge distribution inside the programmed cell by mathematical extraction through Eqs. (1, 2).

$$Q = \int_0^{T_n} Q(x)\, dx \qquad (1)$$



(a)



(b)

Fig. 2. Program operation on the cell at the center (a) Density of electrons trapped in the charge trapping layer, (b) Transfer curves of the GAA BE SONOS flash memory cell before and after program.

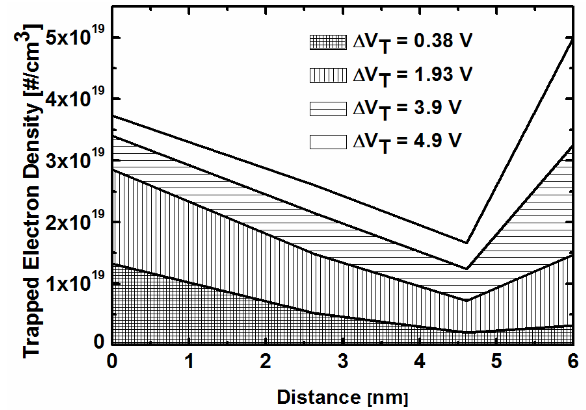


Fig. 3. Distributions of the trapped charges in the vertical direction inside nitride trapping layer obtained at different program times.

$$x_{\text{centroid}} = \frac{1}{Q}\int_0^{T_n} xQ(x)\, dx \qquad (2)$$

Here, T_n is the thickness of nitride trapping layer, $Q(x)$ is the trapped charge density per unit volume, as a function of vertical distance x. Q is the density of trapped

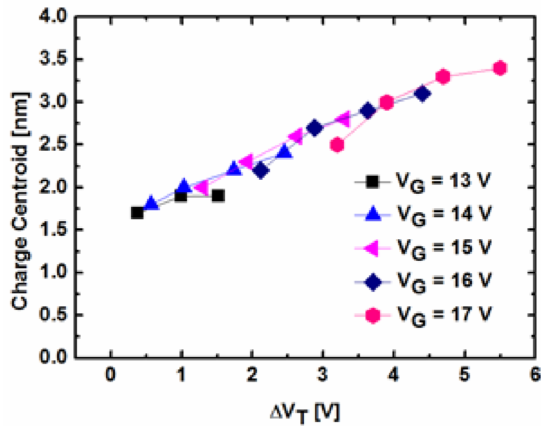
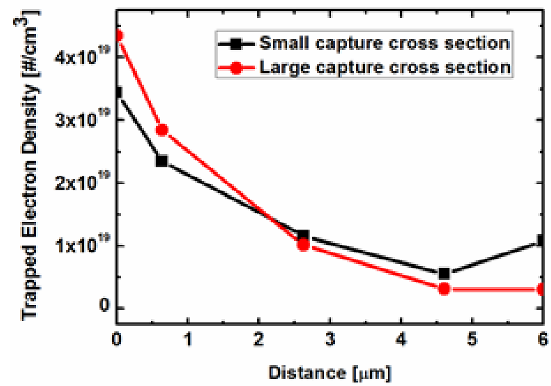


Fig. 4. Location of centroid of the trapped electrons in the nitride layer as a function of ΔV_T at different V_{PGM}'s.

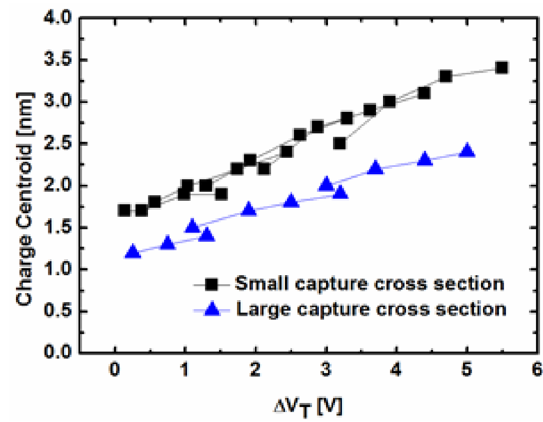
charges per unit area throughout the entire Si_3N_4 layer.

Fig. 3 demonstrates the distributions of the trapped charges inside the nitride trapping layer depending on program time. The program voltage (V_{PGM}) was 16 V and the pulse durations were 10 µs, 100 µs, 1 ms, and 10 ms. As the pulse gets longer, the threshold voltage shift (ΔV_T) becomes larger. The total length of 6 nm in the figure corresponds to the thickness of nitride trapping layer. The left-side boundary is the interface between tunneling oxide and nitride charge trap layer and the right-side one is that between nitride and the blocking oxide.

Fig. 4 depicts the location of charge centroid as a function of ΔV_T at different V_{PGM}'s. As shown in the figure, the charge centroid migrates from the bottom oxide side to the top oxide side. It is notable that the location of charge centroid depends only on ΔV_T and is not affected by V_{PGM}. In other words, the same ΔV_T obtained from different program voltages leads to the same location, which agrees with the previous results [12-14]. However, $x_{centroid}$ is substantially affected by the intrinsic properties of the trapping nitride layer. When the capture cross-sectional area is large, the injected charges are trapped near the tunnel oxide, which means that the effective capacitance becomes small. On the other hand, in case of small capture cross-sectional area, the programmed charges are located near the blocking oxide, farther from the channel, since the trapping probability gets smaller. The dependence of distribution of trapped charges on capture cross-sectional area is shown in Fig. 5(a). From the $x_{centroid}$'s extracted from the distributions in Fig. 5(a) by Eqs. (1, 2) are depicted in Fig. 5(b).



(a)



(b)

Fig. 5. Effects of capture cross-sectional area (a) Distributions of programmed charges as a function of distance, (b) $x_{centroid}$ as a function of ΔV_T at different capture cross sections (small area: 5×10^{-18} cm^2, large area: 1×10^{-15} cm^2).

Fig. 6 depicts the charge centroid as a function of ΔV_T. As the trap density is low (black square line), the programmed charges are distributed relatively farther from the tunneling oxide interface. On the other hand, in case of high trap density, the distribution is pulled toward the tunneling oxide interface. It should be more probable for the electrons to be trapped near the tunneling oxide interface before travelling across the nitride layer and reaching the nitride/blocking oxide interface as the trap density becomes higher.

In case of low trap density, the trap sites near the tunneling oxide/nitride interface are more readily occupied by the program electrons, and additional charges are not likely to have a high probability to occupy the energy states of the nitride traps. Instead, the surplus program electrons are drifted to the deeper nitride region. Consequently, $x_{centroid}$ shows an abrupt shift. Fig. 7 shows this process schematically where J_{trap} is trapping

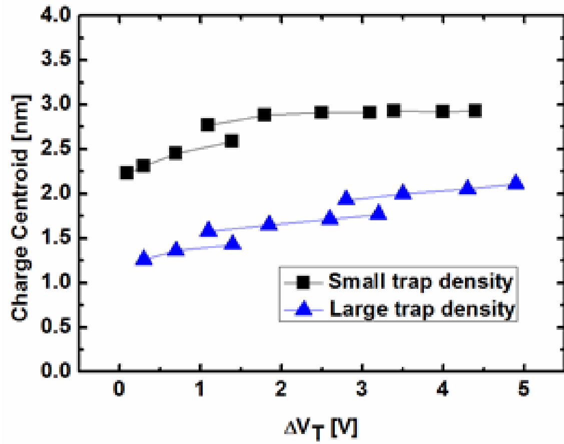


Fig. 6. Location of centroid of the trapped electrons in the nitride layer as a function of ΔV_T at different trap densities (low trap density: 3×10^{19} cm^{-3}, high trap density: 8×10^{19} cm^{-3}).

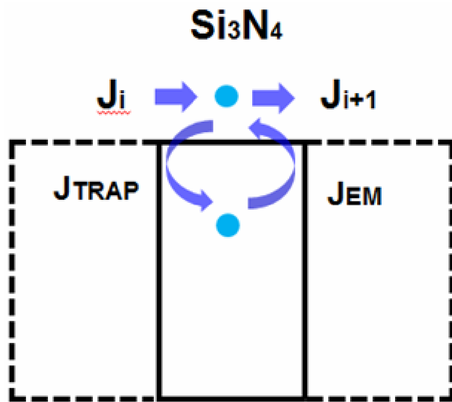


Fig. 7. Schematic representation of the injected charges in the nitride layer.

current density, J_{em} is emission current density, J_i is electron current density incoming to the ith nitride unit volume, and J_{i+1} is electron current density outgoing from the nitride unit volume. In short, under low-trap-density condition, J_{i+1} becomes larger compared with the case of high-trap-density condition and the distribution of trapped electrons becomes wider and changes faster.

V. Conclusions

In this work, we closely investigated the relation among charge distribution, charge centroid, and program operation conditions. On the initial stage of the program, charge centroid is located between tunneling oxide and the center of nitride charge trap layer. The charge centroid moves toward the blocking oxide since a considerable number of additional program charges are trapped farther from the tunneling ONO-nitride interface as the program voltage gets higher. Also, it has been confirmed that charge centroid has higher dependence on program voltage than program time. Thus, longer charge centroid shift comes with the larger threshold voltage shift resulted from higher program voltage rather than longer program time. Further, it has been proven that effective capture cross-sectional area and trap density play an important role in determining the charge centroid. Both properties can be controlled by process conditions even though the base materials are the same. Capture cross-sectional area and trap density act in the same manner that higher values are more effective in distributing the trapped charges closer to the tunneling oxide/nitride interface. The accurate charge centroid model will make a better way to design processing conditions and operating schemes for precise allocation of the threshold voltages for multi-level/triple-level/X-level cell operations.

Acknowledgments

This work was supported by the Brain Korea 21 Plus Project in 2015 and Samsung Electronics Corp. This work was also supported by Business for Cooperative R&D between Industry, Academy, and Research Institute funded by Korean Small and Medium Business Administration in 2015 (No. C0300518).

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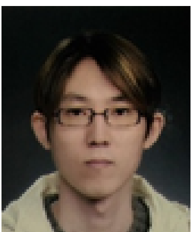
Seunghyun Kim received the B.S. degrees in 2010 from Seoul National University (SNU) Seoul, Korea, where he is currently working toward the Ph.D. degree in electrical engineering. His research interest is characterization of nonvolatile memory device.

Dae Woong Kwon was born in Seoul, Korea, in 1979. He received the B.S. degrees in 2005 from KwangWoon University, Seoul, Korea. he is currently working toward the M.S degree in electrical engineering in Seoul National University (SNU), Seoul, Korea. He has designed the Nand Flash memory Process Structure from 2005 at Samsung Electronics, Yongin , Korea. His current research interests include XIZO Channel material amorphous TFT Electrical , Optical Stress Model.

Sang-Ho Lee was born in Cheonan, Korea, in 1986. He received the B.S. degree in 2012 from Seoul National University (SNU), Seoul, Korea, where he is currently working toward the Ph.D. degree in electrical engineering. His current research interests include nonvolatile memory device fabrication, characterization, measurement. Mr. Lee is currently a Student Member of the Institute of Electronics Engineers of Korea (IEEK).

Sangku Park was born in Chung-ju, Korea, in 1981. He received the B.S. in 2008 and from Hanyang University, Seoul, Korea in electrical engineering. From 2008, he has been working in Samsung Electronics Co. Ltd. and currently studying toward the MS degree in the School of Electrical Engineering (SoEE), SNU.

Youngmin Kim received the B.S. degree from the Department of Electronics Engineering, Gachon University, Seongnam, Korea, in Feb. 2016, where he currently pursuing the M.S. degree. His research interests include emerging memory devices, nanoscale CMOS devices, and fabrication technology. He is a Student Member of the Institute of Electronics and Information Engineering (IEIE) and a Graduate Student Member of the Institute of Electrical and Electronics Engineers (IEEE).



Hyungmin Kim received the B.S. and the M.S. degrees in electrical engineering from Seoul National University Seoul, Korea, in 2010 and 2003, respectively. He worked at the Flash Memory Division, Samsung Electronics, for 5 years, where he developed many generations of Samsung 1st Fusion Flash Memory, OneNAND. Then, he has worked at Novachips as an SSD System Architect and RTL Designer for 7 years. He is now a Principal Research Engineer in Novachips.

Young Goan Kim received the B.S. degree in electrical engineering from Pusan University, Korea. He has 20 years of relevant industry experience including positions at LG, Mtek, Samsung, and Indilinx, where he developed Barefoot as a System Architect, RTL Designer, and Team Leader. He has developed more than 20 designs and succeeded in 7 mass products with MPEG, DSP, MP3, ECC, Compress, NAND HW & FW, eMMC, Blutooth, ARM-based embedded designs, CD/DVD/HDDVD/Blue-ray, SSD, and HLNAND. He is currently the President/CTO of Novachips.

Seongjae Cho received the B.S. and the Ph.D. degrees in electrical engineering from Seoul National University, Seoul, Korea, in 2004 and 2010, respectively. He worked at as an Exchange Researcher at the National Institute of Advanced Science and Technology (AIST) in Tsukuba, Japan, in 2009. Also, he worked as a Postdoctoral Researcher at Seoul National University in 2010 and at Stanford University, CA, USA, from 2010 to 2013. Currently, he is an Assistant Professor at the Department of Electronics Engineering, Gachon University, Seongnam, Korea. His research interests include emerging memory technologies, nanoscale CMOS devices, optical devices, and electrical-optical integrated circuits. He is a Life Member of IEIE and a Member of IEEE Electron Devices Society (EDS) and Photonics Society.

Byung-Gook Park received his B.S. and M.S. degrees in electronic engineering from Seoul National University in 1982 and 1984, respectively, and the Ph.D. degree in electrical engineering from Stanford University, Stanford, CA, in 1990. From 1990 to 1993, he was with AT&T Bell Laboratories, where he contributed to the development of 0.1-μm CMOS and its characterization. From 1993 to 1994, he was with Texas Instruments, developing 0.25-μm CMOS. In 1994, he joined Seoul National University as an Assistant Professor in the School of Electrical Engineering (SoEE), where he is currently a Professor. He led the Inter-university Semiconductor Research Center (ISRC), Seoul National University, as the Director from June 2008 to June 2010. His current research interests include the design and fabrication of nanoscale CMOS, Si quantum devices, emerging memory technologies, and neuromorphic systems. He has authored and co-authored more than 950 research papers in journals and conferences. Prof. Park has served as a committee member on several international conferences including Microprocesses and Nanotechnology, International Electron Devices Meeting (IEDM), Conference on Solid State Devices and Materials (SSDM), and IEEE Silicon Nanoelectronics Workshop (SNW) and served as an Editor of IEEE Electron Device Letters. He received Best Teacher Award from SoEE of Seoul National University in 1997, Doyeon Award from Creative Research from ISRC in 2003, Haedong Paper Award from the Institute of Electronic Engineers of Korea (IEEK) in 2005, and Educational Award from College of Engineering, Seoul National University, in 2006. Also, he received Haedong Academic Research Award from IEEK in 2008.