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Effect of Annealing Temperature on the Electrical Performance of SiZnSnO Thin Film Transistors Fabricated by Radio Frequency Magnetron Sputtering

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Amorphous oxide thin film transistors (TFTs) were fabricated with 0.5 wt% silicon doped zinc tin oxide (a-0.5SZTO) thin film deposited by radio frequency (RF) magnetron sputtering. In order to investigate the effect of annealing treatment on the electrical properties of TFTs, a-0.5SZTO thin films were annealed at three different temperatures (300°C, 500°C, and 700°C) for 2 hours in a air atmosphere. The structural and electrical properties of a-0.5SZTO TFTs were measured using X-ray diffraction and a semiconductor analyzer. As annealing temperature increased from 300°C to 500°C, no peak was observed. This provided crystalline properties indicating that the amorphous phase was observed up to 500°C. The electrical properties of a-0.5SZTO TFTs, such as the field effect mobility (μ_{FE}) of 24.31 cm^2/Vs, on current (I_{ON}) of 2.38×10^{-4} A, and subthreshold swing (S.S) of 0.59 V/decade improved with the thermal annealing treatment. This improvement was mainly due to the increased carrier concentration and decreased structural defects by rearranged atoms. However, when a-0.5SZTO TFTs were annealed at 700°C, a crystalline peak was observed. As a result, electrical properties degraded. μ_{FE} was 0.06 cm^2/Vs, I_{ON} was 5.27×10^{-7} A, and S.S was 2.09 V/decade. This degradation of electrical properties was mainly due to increased interfacial and bulk trap densities of forming grain boundaries caused by the annealing treatment.

Keywords: Thin film transistor, Annealing temperature, Oxide semiconductor, SiZnSnO, X-ray diffraction spectroscopy

1. INTRODUCTION

Conventional display panels are driven by thin film transistors (TFTs) mostly using silicon (Si) based active channel layers such as polycrystalline silicon (poly-Si) or amorphous silicon (a-Si). However, the mobility of a-Si TFTs is too low for use in high resolution displays. Poly-Si TFTs have several problems, including low uniformity and high fabrication cost. For these reasons, many materials have been investigated. Among them, amorphous oxide semiconductor (AOS) TFTs have received great attention as one of the most promising candidates for backplane device application in next generation displays. This is due to their high mobility, uniformity and transparency. Currently, indium-gallium-zinc-oxide (IGZO) is one of the most used TFT channel materials [1-3]. However, the indium (In) in IGZO has several problems, including toxicity and high cost. Therefore, non-toxic and inexpensive semiconductor materials, such as zinc tin oxide (ZTO), have been explored.

However, ZTO has a propensity to readily generate many oxygen vacancies, causing poor stability and defect states. To improve device performance, research has been done on various process controls (such as oxygen partial pressure [4,5], sputtering power [6], the composition of each element [7-10], the contact material for source and drain (S/D) metals [11,12], and the annealing conditions [13,14]). Among these, annealing process is an effective way to improve electrical properties caused by decremental defects. Most AOSs TFTs are annealed to improve electrical properties and device stability after deposition at room temperature. Therefore, it is very important to optimize the annealing temperature [13].

In this study, we show how the annealing temperature of 0.5 wt%

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silicon doped zinc tin oxide (a-0.5SZTO) thin film transistors (TFTs) changes the electrical properties and structures.

2. EXPERIMENTS

The a-0.5SZTO (Zn:Sn=65:35) channel layers were deposited by RF magnetron at room temperature on a SiO_2 (200 nm)/p-type Si substrate with the bottom gate structure. The sputtering conditions were Ar:O_2 flow ratio of 30:1, RF power of 50 W, and process pressure of 3 mTorr. After deposition, the films were annealed at various temperatures for 2 hours. Annealing temperatures ranging from 300°C to 700°C were used in air atmosphere at the intervals of 200°C. Channel and electrode patterning was performed by a photolithography process. The width and length of the active channel layer were 250 μm and 50 μm, respectively. The Ti (10 nm)/Al (50 nm) source/drain electrodes were deposited using an e-beam and thermal evaporation, respectively, and followed by the lift off processes.

Figure 1 shows a schematic diagram of the a-0.5SZTO TFT structure with the bottom gate and top contact electrode. The structural properties of a-0.5SZTO thin films were confirmed by X-ray diffraction (XRD, D8 Discover with GADDS, Bruker Co). The electrical properties of a-0.5SZTO TFTs were measured by using a semiconductor analyzer (EL 423, ELECS Co.).

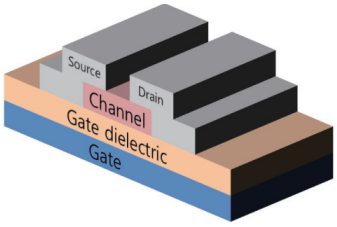

Fig. 1. Schematic diagram of a-0.5SZTO TFTs.

3. RESULTS AND DISCUSSION

Figure 2 shows XRD patterns of a-0.5SZTO thin films on Si substrate with different annealing temperatures, ranging from 300°C to 700°C. The sharp peaks at 22° and 33° are the signal of Si substrate. As the annealing temperature increased from 300°C to 500°C, no peak was observed. This indicated that the amorphous phase was maintained up to 500°C. However, when a-0.5SZTO thin films were annealed at 700°C, ZnO(100), ZnO(101) crystalline peaks were observed.

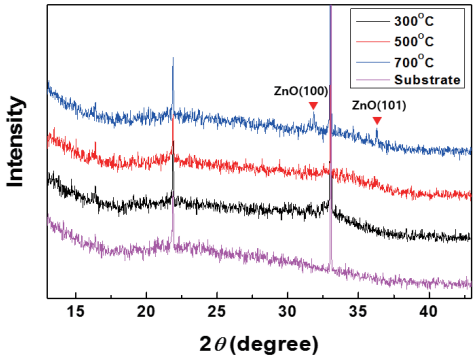

Fig. 2. XRD patterns of the a-0.5SZTO thin films annealed at 300°C, 500°C and 700°C.

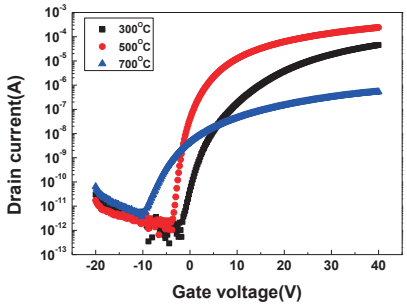

Fig. 3. Transfer curves of the fabricated a-0.5SZTO TFTs annealed at 300°C, 500°C, and 700°C.

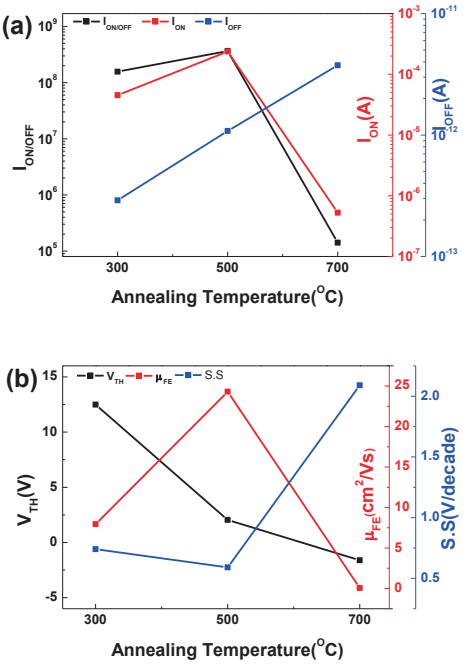

Fig. 4. Electrical properties of the a-0.5SZTO TFTs with different annealing temperatures, $I_{ON/OFF}$, I_{ON} and I_{OFF} shown as in (a), and V_{TH}, μ_{FE} and S.S shown as in (b).

Figure 3 shows transfer curves of 300°C, 500°C and 700°C. All a-0.5SZTO TFTs were measured at a drain voltage (V_{DS}) of 5.1 V. Gate voltage (V_{GS}) was swept from -20 V to 40 V. The electrical properties measured can be calculated as follows. The μ_{FE} is extracted using the following equation (1)

$$\mu_{FE}=\frac{Lg_m}{WC_iV_{DS}} \quad (1)$$

Where V_{DS} is the drain voltage, g_m is the transconductance, C_i is the gate dielectric capacitance, W and L are channel width and length [15]. The subthreshold swing (S.S) is extracted using the following equation (2)

$$S.S=\frac{\partial V_{GS}}{\partial \log I_{DS}} \quad (2)$$

Where V_{GS} is the gate voltage and I_{DS} is the drain current [16]. The electrical properties, such as V_{TH}, on/off current ratio ($I_{ON/OFF}$), I_{ON}, I_{OFF}, μ_{FE} and S.S are shown in Fig. 4.

As annealing temperature increased from 300°C to 500°C, the V_{TH} shifted toward the negative direction from 12.48 V to 2.04 V, the I_{OFF} increased from 2.90×10^{-13} A to 6.50×10^{-13} A, and the I_{ON}

increased from 4.54×10^{-5} A to 2.38×10^{-4} A. Also, the μ_{FE} and S.S improved. The μ_{FE} was 24.31 cm^2/Vs, and the S.S was 0.59 V/decade. These improved electrical properties can be explained by the decrease in trap state. High annealing temperatures decrease the structural defects of the a-0.5SZTO active layer. The electrons can more easily transport in the a-0.5SZTO channel layer due to fewer trap states from structural defects [17,18]. Consequently, optimized annealing temperature improves electrical properties by decreasing trap density (such as V_{TH}, I_{OFF}, I_{ON}, μ_{FE} and S.S). However, the 700°C annealed a-0.5SZTO thin film exhibited a poor electrical properties (I_{ON} was 5.27×10^{-7} A, μ_{FE} was 0.06 cm^2/Vs and S.S was 2.09 V/decade). This degradation was due to the crystallization channel as shown in Fig. 2. This channel has grain boundaries that deteriorate the electrical properties. The grain boundaries with poor crystallinity cause forming a double schottky potential barrier, trapping free carriers, and increasing trap density in channel layer [19]. As a result, the optimized annealing temperature was 500°C. The electrical properties of the device annealed at 700°C were worse than those of the device annealed at 500°C.

4. CONCLUSIONS

In this study, we investigated the effect of annealing temperature on the electrical and structural properties of 0.5SZTO TFT fabricated by RF sputtering to verify the mechanism of crystal structure dependency of a-SZTO on the electrical properties of a-SZTO TFT. We observed the crystalline structure by XRD patterns depending on the annealing temperature. When a-0.5SZTO film was annealed at 700°C, it was clearly observed that the a-0.5SZTO film structure changed from amorphous to polycrystalline. The electrical properties of the sample annealed at 500°C showed enhanced performance. However, when the annealing temperature increased from 500°C to 700°C, I_{ON} decreased from 2.38×10^{-4} A to 5.27×10^{-7} A, mobility decreased from 24.31 cm^2/Vs to 0.06 cm^2/Vs, and S.S decreased from 0.59 V/decade to 2.09 V/decade. This degradation of the electrical properties is mainly due to the increased trap density by grain boundaries. We derived the relationship between the controlled crystal structure by changing the annealing temperature and the electrical performance of the TFTs. This clearly indicates that optimized annealing temperature can improve the electrical properties of a-0.5SZTO TFTs.

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