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Influence of Channel Thickness Variation on Temperature and Bias Induced Stress Instability of Amorphous SiInZnO Thin Film Transistors

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TFTs (thin film transistors) were fabricated using a-SIZO (amorphous silicon-indium-zinc-oxide) channel by RF (radio frequency) magnetron sputtering at room temperature. We report the influence of various channel thickness on the electrical performances of a-SIZO TFTs and their stability, using TS (temperature stress) and NBTS (negative bias temperature stress). Channel thickness was controlled by changing the deposition time. As the channel thickness increased, the threshold voltage (V_{TH}) of a-SIZO changed to the negative direction, from 1.3 to -2.4 V. This is mainly due to the increase of carrier concentration. During TS and NBTS, the threshold voltage shift (ΔV_{TH}) increased steadily, with increasing channel thickness. These results can be explained by the total trap density (N_T) increase due to the increase of bulk trap density (N_{Bulk}) in a-SIZO channel layer.

Keywords: Amorphous SiInZnO, Instability, Negative bias temperature stress, Activation energy

1. INTRODUCTION

TAOS (transparent amorphous oxide semiconductors) based TFTs (thin film transistors) are promising candidates as the next generation materials for backplane devices of active matrix displays, to replace conventional amorphous silicon (a-Si) due to their superior electrical properties, such as high mobility of >10 cm^2/V s, good uniformity, and good subthreshold swing. In addition, TAOS TFTs are transparent in visible light because of their large band gap (>3.3 eV). Moreover, TAOS materials are suitable for flexible displays, such as rollable and foldable, providing low cost process like roll to roll. Mobility is an important electrical parameter in TAOS; however, it greatly depends on the channel materials, gate insulators, applied voltage, and TFT structures. The leading TAOS materials are indium-zinc-oxide (a-IZO) based materials, due to their excellent electrical properties, foremost among them being amorphous indium-gallium-zinc-oxide (a-IGZO) [1-3]. However, since gallium is very expensive and rare, gallium-free materials like ZTO (zin-tin-oxide) [4], HIZO (hafnium-indium-zinc-oxide) [5], SZTO (silicon-zinc-tin-oxide) [6], and a-SIZO (amorphous silicon-indium-zinc-oxide) are rapidly studied. Recently, Lee et al. reported that a-SIZO TFT has high field effect mobility and low temperature process below 150°C [7]. This material can contribute to flexible display due to low manufacturing temperature. Moreover, high manufacturing temperatures over 250°C, such as post-annealing and passivation process, are critical options to use flexible substrates. However, the electrical stability of TAOS TFTs for flexible electronic devices is a serious problem under BS (bias stress), TS (temperature stress), and IS (illumination stress). Electrical stability is still studied in terms of manufacturing temperature, doping the carrier generation suppressor materials, such as Zr, Hf, Si and Al, the contact between gate insulator and channel interface, and the control of channel thickness. The channel thickness is an important parameter in TFT.

In this paper, a-SIZO TFTs with different channel thickness, using RF (radio frequency) magnetron sputtering at below 150°C, have been fabricated. The stability of a-SIZO TFTs was measured by TS and NBTS. The influence of the channel thickness on the electrical performances of a-SZTO TFTs were also investigated by analyzing activation energy falling late.

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2. EXPERIMENTS

The a-SIZO channels were deposited by RF magnetron sputtering on substrate (SiO_2 (200 nm)/p-type Si). The target of a-SIZO used was 1 wt. % Si-incorporated SIZO (In_2O_3:ZnO ratio = 3:1), magnetron sputtering power density of 30 W, process pressure of 4 mTorr, and Ar flow ratio of 30 sccm at room temperature. The various thicknesses for a-SIZO films were controlled by changing the deposition time. All films were annealed at 150°C for 2 hrs in a thermal furnace with air ambience. Channel and source/drain electrodes were patterned by the conventional photolithography and wet-etching processes. The Ti (10 nm)/Al (50 nm) source/drain electrodes were fabricated using ebeam and thermal evaporator, respectively, followed by lift-off process. The patterned channel width and length were 250 μm and 50 μm, respectively.

Figure 1 shows a schematic diagram of the a-SZTO TFT. The electrical performance and the electrical stability were measured in the dark, using a semiconductor parameter analyzer (EL 423, ELECS Co.) and vacuum probe station (HP4145B, Hewlett-Packard Co.). The a-SIZO channel thickness was measured to be about 12, 24, and 36 nm by -step (Alpha-step D-100, KLA Tencor Co.).

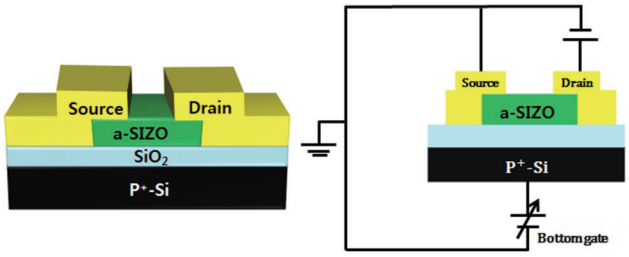

Fig. 1. Schematic diagram of the fabricated a-1SIZO TFT structure.

3. RESULTS AND DISCUSSION

Figure 2(a) shows the drain current (I_{DS})-gate voltage (V_{GS}) characteristics of a-SIZO TFTs with drain voltage (V_{DS}) of 5.1 V and gate voltage from -20 V to 40 V. Their electrical performance, such as field effect mobility (μ_{FE}), threshold voltage (V_{TH}), on-off current ratio ($I_{ON/OFF}$), and subthreshold slope (S.S), are summarized in Table 1. As the channel thickness increases, the μ_{FE} (9.5 to 19.4 cm^2/V s) and ION/OFF (8.5×10^8 to 1.3×10^9) increased correspondingly, and the transfer curve of the a-SIZO TFTs shifted to negative due to the increase of carrier concentration. The μ_{FE} was calculated by equation (1) [8] :

$$\mu_{FE} = \frac{L g_m}{W V_{DS} C_{OX}} \quad (1)$$

where g_m is the trans-conductance, C_{OX} is the oxide capacitance of the gate insulator, and W and L are channel width and length, respectively. Also, it is observed that the S.S value increased significantly. This change can be attributed to the change of the total trap density (N_T).

Figure 2(b) shows the total trap density of a-SIZO TFTs with various channel thickness. We calculated of N_T value from the S.S by using equation (2) [9] :

$$N_T = N_{IT} + N_{Bulk} = \left\{ \frac{S.S \log(e)}{kT/q} - 1 \right\} \frac{C_i}{q} \quad (2)$$

where N_{IT} is the interfacial trap density, N_{Bulk} is the bulk trap density, T is the absolute temperature, k is the Boltzmann constant, q is the electronic charge, and Ci is the capacitance of the gate insulator. According to equation (2), as channel thickness increased, the N_T values rapidly rise from 5.2×10^{11} to 1.0×10^{12} cm^{-2}. a-SIZO TFTs have same gate insulator/channel interface since the channel thickness is controlled only by deposition time, and hence the N_T values are dependent on the N_{Bulk} values. In general, the S.S value was affected by NIT, which in turn was affected by channel thickness in thin films.

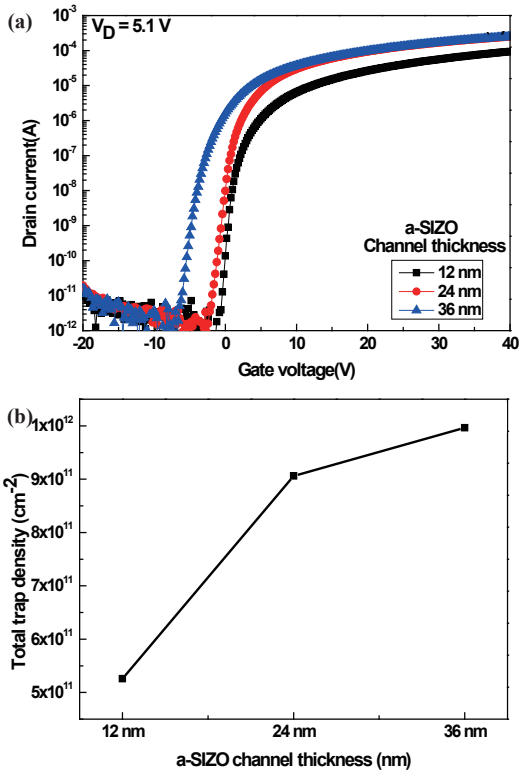

Fig. 2. Transfer curve (a) and total trap density (b) of a-SIZO TFTs with various channel thickness.

Table 1. Summary of the electrical properties of a-SIZO TFTs with various channel thickness.

Channel thickness (nm)	V_{TH} (V)	$I_{On/Off}$ ratio	μ_{FE} (cm^2/Vs)	S.S (V/decade)
12	1.3	8.5×10^8	9.5	0.39
24	0.8	1.2×10^9	19.1	0.56
36	-2.4	1.3×10^9	19.4	0.61

Figure 3 and Figure 4 shows the evolution of transfer curves of a-SIZO TFTs with various channel thickness under temperature stress and their activation energy (E_A), from 298 to 333 K. The V_{TH} is clearly observed to be negatively shifted. The ΔV_{TH} of a-SIZO TFTs under temperature stress is related with the increase in thermally excited electrons. As the temperature increased, the captured electrons are emitted from trap sites by thermal energy. The values of ΔV_{TH} of a-SIZO TFTs were measured at 1.21, 1.35, and 2.29 V, as channel thickness increased at intervals of 12 nm, from 12, 24 to 36 nm, respectively. As mentioned, 12 nm of channel thickness has less trap sites, and therefore few electrons were emitted from the trap site. We estimated the E_a depends on the change of gate voltages in the forbidden band gap by fitting the temperature stress for different channel thicknesses. The E_a was investigated by using equation (3) [10] :

$$I_D = I_{D0} \cdot \exp\left(-\frac{E_a}{kT}\right) \quad (3)$$

where I_{D0} is the prefactor, k is Boltzmann constant, T is the absolute

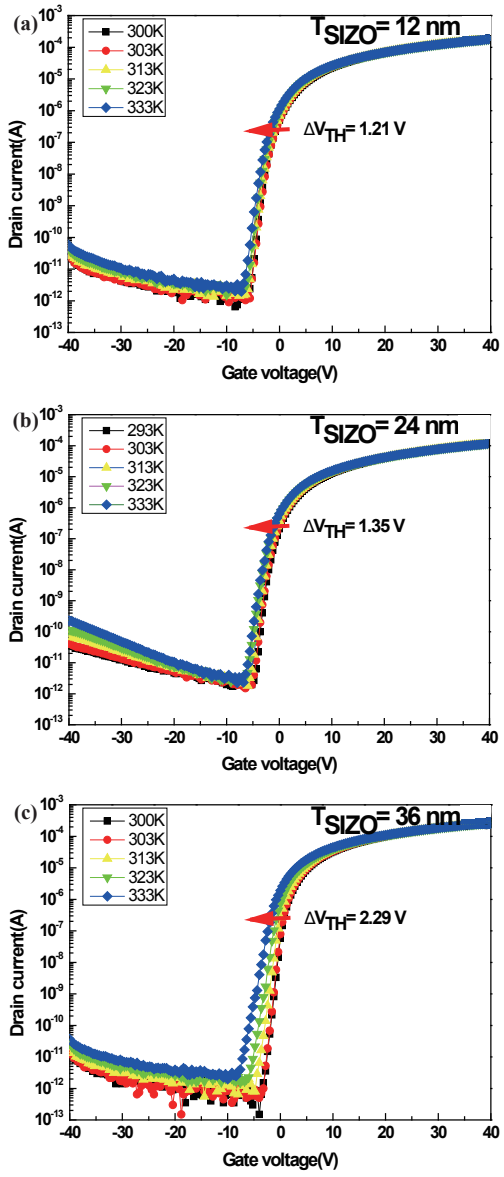

Fig. 3. Change of the transfer characteristics with various channel thickness of a-SIZO TFTs under TS from, room temperature to 333 K. (a) 12 nm, (b) 24 nm, and (c) 36 nm.

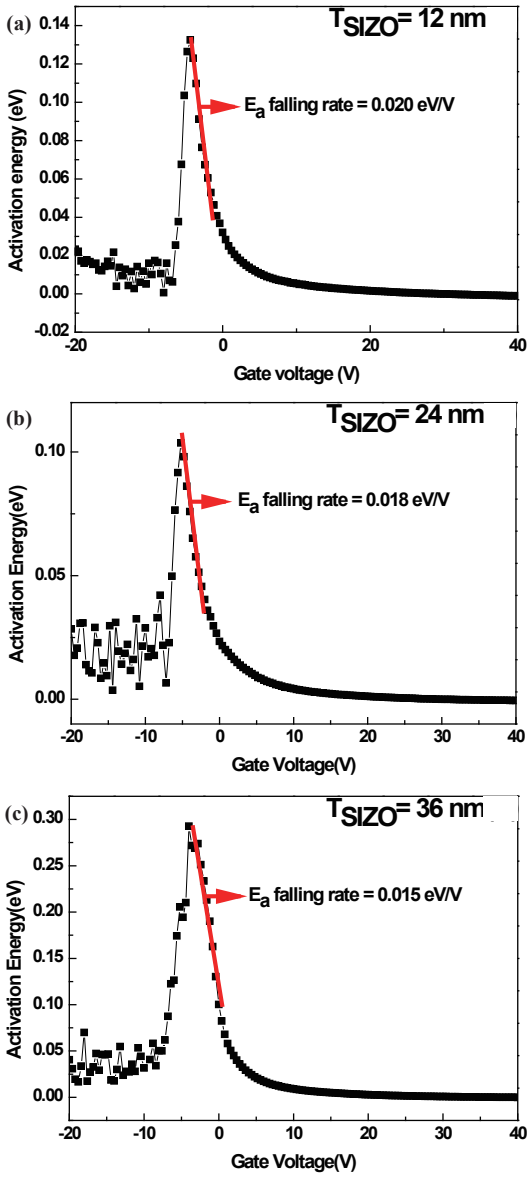

Fig. 4. The activation energy of a-SIZO TFTs (a) 12 nm, (b) 24 nm, and (c) 36 nm.

temperature, and E_a is activation energy. The estimated E_a falling rates were 0.020, 0.018, and 0.015 eV/V for 12 nm, 24 nm, and 36 nm a-SIZO TFTs, respectively. In general, the fast falling rate means the probability increased that the free electrons were not obstructed from source to drain electrodes, and the falling rate is closely related with the charge trapping time [11]. This indicates that the ΔV_{TH} increases and Ea falling rates decrease, depending on N_T. In previous researches, the Ea falling rate in the subthreshold region is inversely proportional to N_T, while E_a is closely related to a trap site density of channel layer [12]. As the channel thickness increased from 12 to 36 nm, the Ea falling rate decreased from 0.020 to 0.015 eV/V. These trends were exactly inversely proportional to N_T in a-SIZO TFTs [13].

Figure 5 shows the change of the transfer curve of a-SIZO TFTs with various channel thickness under negative bias temperature stress (NBTS). The a-SIZO TFTs were measured at V_{GS} = -20 V, V_{DS} = 0.1 V, and temperature (T) = 60°C for 7,200 sec. First measurement was conducted right after the fabrication. Second measurement was at T = 60°C, followed by measurements after 300 sec, 600 sec, 1,200 sec, 1,800 sec, 3,600 sec, and 7,200 sec, sequentially.

For device of 12 nm thickness a-SIZO TFT, a negative V_{TH} shift of 15.22 V was observed with increasing stress time. As increasing channel thickness, the ΔV_{TH} of a-SIZO TFTs gradually increased from 15.22 to 19.13 V. Under negative gate bias, the VTH shifted toward negative direction because of the hole carriers trapping model near the gate insulator/channel layer interface. In general, the commonly accepted mechanism of NBTS in AOS TFTs include: (i) hole trapping in a gate insulator or/and gate insulator/channel interface [14], (ii) thermally exciting electrons are emitted from trap sites [15], (iii) defect creation in the channel materials [16], and (iv) ambient effects, including the desorption of oxygen and/or water molecules [17]. In this study, the mechanism of ambient effects can be ruled out since all a-SIZO TFTs were measured in a vacuum probe station. Also, the mechanism of defect creation in the channel materials can be excluded because all the a-SIZO TFTs did not show large degradation of electrical properties, such as μ_{FE}, S.S values, and $I_{ON/OFF}$. Therefore, for all a-SIZO TFTs, it should be considered that the thermally exciting electrons and hole trapping model were dominant mechanism of the negative direction shift of V_{TH} under NBTS in this study. As channel thickness increased, a-SIZO TFTs showed increasing ΔV_{TH} values. These results were

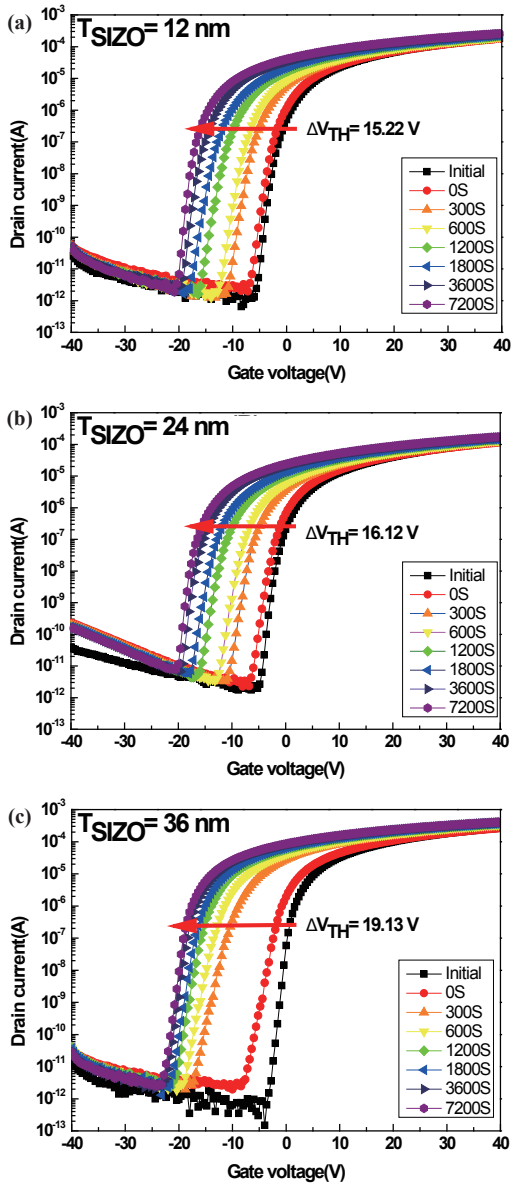

Fig. 5. Change of the transfer characteristics with the various channel thickness of a-SIZO TFTs, under NBTS for 7,200s. (a) 12 nm, (b) 24 nm, and (c) 36 nm.

caused by the thermally exciting electrons emitted from trap sites and the hole trapping in a gate insulator and/or interface. a-SIZO TFTs of channel thickness 24 and 36 nm have more trap sites in channel than 12 nm, hence the thicker channels emitted more free electrons, and showed greater V_{TH} shift.

4. CONCLUSIONS

In conclusion, we report the channel thickness dependency of a-SIZO TFT under temperature and bias induced stress. As channel thickness increases, a-SIZO TFTs show an improvement of electrical properties such as μ_{FE}, $I_{ON/OFF}$, depending on increasing of carrier concentration. The S.S values and N_T values increase. That is mean thicker SIZO has more defect in bulk. These results are derived from the degradation of VTH under TS and NBTS. In this study, a-SIZO TFT (24 nm) has good electrical properties (μ_{FE} (12.8 cm^2/V s) and $I_{ON/OFF}$ (1.2×10^9)) and better electrical stability (ΔV_{TH} = 19.1 V) than 36 nm (ΔV_{TH} = 19.13 V) thickness of a-SIZO channel under NBTS. Thus, the a-SIZO channel thickness should be considered, to provide better stability and electrical properties when we fabricate a-SIZO TFTs.

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