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Review Article

Understanding radiation effects in SRAM-based field programmable gate arrays for implementing instrumentation and control systems of nuclear power plants

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ABSTRACT

Field programmable gate arrays (FPGAs) are getting more attention in safety-related and safety-critical application development of nuclear power plant instrumentation and control systems. The high logic density and advancements in architectural features make static random access memory (SRAM)-based FPGAs suitable for complex design implementations. Devices deployed in the nuclear environment face radiation particle strike that causes transient and permanent failures. The major reasons for failures are total ionization dose effects, displacement damage dose effects, and single event effects. Different from the case of space applications, soft errors are the major concern in terrestrial applications. In this article, a review of radiation effects on FPGAs is presented, especially soft errors in SRAM-based FPGAs. Single event upset (SEU) shows a high probability of error in the dependable application development in FPGAs. This survey covers the main sources of radiation and its effects on FPGAs, with emphasis on SEUs as well as on the measurement of radiation upset sensitivity and irradiation experimental results at various facilities. This article also presents a comparison between the major SEU mitigation techniques in the configuration memory and user logics of SRAM-based FPGAs.

1. Introduction

Field programmable gate arrays (FPGAs) are already a well-known technology in applications such as aerospace, automotive, medical, and high-performance computing and data storage. However, FPGAs are not much used in the area of nuclear power plant (NPP) instrumentation and control (I&C) systems. The International Atomic Energy Agency recommends the use of FPGAs instead of analog- and microprocessor-based systems [1] in future and existing nuclear I&C systems to improve reliability and also to overcome fast obsolescence. As of now, there are only a few reactors in the world that use FPGA-based systems for their I&C, as shown in Table 1 [2]; among those, most systems are implemented using antifuse FPGAs. However, SRAM-based FPGAs have the benefit of the most up-to-date fabrication process, on par with complementary metal–oxide–semiconductor (CMOS) process technology; they also offer much higher integration and logic capacity as well when compared with flash- or antifuse-based FPGAs [3,4]. Along with the mentioned advantages, SRAM-based FPGAs can be reconfigured an infinite number of times without any degradation in their performance. These features make SRAM-based FPGAs more suitable for complex design implementation. As a result of the implementation of the defense in depth concept in I&C architecture, use cases of the programmable logic device–based designs are varied in their applications and importance. For example, programmable logic device–based designs are used to develop instrumentation for shutdown systems (design assurance level: high) and instrumentation for simple data acquisition systems (design assurance level: moderate to low). SRAM-based FPGAs are primarily targeted for designs in which the assurance level required is moderate to low. The typical cross-section data [5] for SRAM-based FPGAs suggest that the failure rate expressed as failure in times (FITs) due to irradiation in installed locations is much less than the overall target failure rate of the system, i.e., the selected device is not the weakest link in the structure and can be safely used. SRAM-based FPGAs provide the added advantage of configuration readback, which

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Table 1
FPGA-based I&C Systems in NPPs.

Nuclear reactor/company	Type & status	FPGA-based systems
Prototype Fast Breeder Reactor, India	Fast breeder reactor , under construction	Reactor core central sub assembly temperature monitoring system, Primary sodium pump reactivity meter, VME (Versa Module Europa) bus–based CPU card, analog I/O cards, and digital I/O cards
CANDU (CANadian Deuterium Uranium) Reactor	Pressurized heavy water reactor, operational	System implemented the logic for shutdown system No.1
Lungmen Nuclear Power Plant, Taiwan	Boiling water reactor, unfinished	Reactor protection system
Wolf Creek Generating Station, USA	Pressurized water reactor, operational	Main steam and feed-water isolation system
The Ukrainian RPC (Research and Production Company) Radiy for Ukrainian and Bulgarian NPPs	—	Reactor trip system, reactor power control and limitation system, power equipment for rods control system, and regulation and monitoring control and protection system for research reactors.
Rolls-Royce and Electricite de France	Pressurized water reactor	Rod control systems

FPGA, field programmable gate array; I&C, instrumentation and control; NPP, nuclear power plant.

enables system-level diagnostics to reprogram the FPGA in case of an error, a feature that is missing in antifuse- and flash-based FPGAs. Flash- and antifuse-based FPGAs find maximum applications in safety systems, where they are made as simple as possible to enhance the reliability. Capabilities of SRAM-based FPGAs for complex computations and dynamic and partial reconfiguration at runtime [6] are not much required for these systems. However, core temperature-monitoring systems in fast reactors which are tasked with core supervision for early detection of core anomalies, such as plugging of fuel subassemblies and errors in core loading, are a notable exception [7]. These require substantial input/output (I/O) handling capability and processing power and are usually implemented using a microprocessor-based system. SRAM-based FPGAs with large logic processing capacities are ideal candidates for hardware implementation of this system and hence require a detailed study. Although SRAM-based FPGAs have numerous advantages, they are vulnerable to radiation effects either due to transient or cumulative radiation exposure [8].

The design that needs to be implemented in FPGAs is converted into bitstreams and downloaded into the device. The bitstreams are stored in the configuration memory, which holds the functionality and the routing of the design mapped into the FPGAs. The configuration memory, which constitutes an array of SRAM memory cells, along with the configuration access ports and control logic, forms the configuration layer. The user logic, user memory, and I/O resources form the application layer. The current state of the functionality is stored in the user memory [9,10]. The configuration memory is organized as an array of frames; each bit is stored in the static RAM cells as shown in Fig. 1. These configuration memory cells implement the lookup tables (LUTs), control multiplexers, and other control elements. A LUT stores its truth table in the configuration memory cells, which implement the combinational logic function. The interconnection structure includes a programmable interconnection point, mostly a pass transistor that is controlled by the value stored in the configuration memory cell [11]. The selection line values of the multiplexers and other programmable elements are also stored in the configuration memory cells. The registers [flip-flops (FFs) and latches] and on-chip memory (Block RAM (BRAM)) bits hold the current state of the circuit [12]. Among the elements of the configuration memory, the configuration memory bits are very prone to radiation effects; the bits dedicated to routing resources are more vulnerable than the bits dedicated to logic resources [13]. In the application layer, BRAM is highly susceptible and registers and I/O resources are medium to low susceptible to radiation effects [14].

This article is organized as follows: Section 2 talks about the major sources of radiation effects and also how particle radiation interacts with matter in various ways. In Section 3, the radiation effects in metal-oxide-semiconductor (MOS) structures, especially SRAM-based FPGAs, with emphasis on single event upsets (SEUs), are discussed. The measurement of radiation upset sensitivity and the effects of various irradiation experiments on SRAM-FPGAs are explained in Section 4. The main SEU mitigation techniques for configuration memory and user logics, which are compared based on their mitigation efficiency, are depicted in Section 5. Concluding remarks are given in Section 6.

2. Sources of radiation effects

FPGAs can be affected by gamma photons and also heavy particles like neutrons, alpha particles, etc. When electronic devices are exposed to gamma ray photons, the energy of the photons gets deposited in the devices, mainly by ionization process. The energy required to form an electron–hole pair is called the ionization dose. However, the cumulative energy absorbed by the circuit during the whole exposure is determined as total ionization dose (TID) [15]. The ionization process can take place directly by gamma photons themselves or indirectly by secondary recoil particles. The major damaging effects due to gamma photons are basically single event effects (SEEs) and TID effects caused by increased conductivity and trapped charges in the electronic devices. Neutron interaction with matter is dominated by collisions, with nuclei leading to either scattering or absorption. In elastic scattering, a neutron collides with a nucleus and scatters in different directions. The energy lost by the neutron is gained by the target nucleus. In inelastic scattering, the neutron

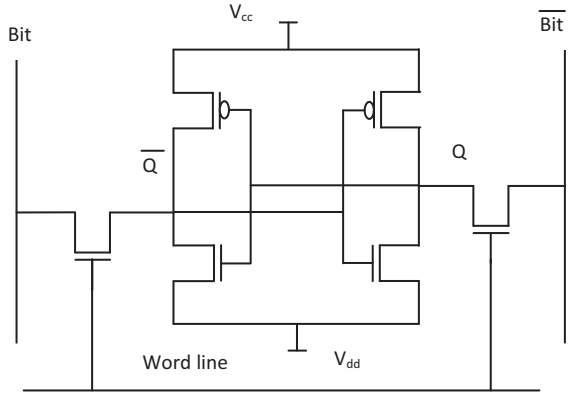

Fig. 1. Basic SRAM cell.

strikes a nucleus, forming a compound nucleus, and the deexcitation process of the nucleus produces gamma radiation.

The neutron absorption reaction includes radiative capture and nuclear fission. A neutron can be captured by nuclei through one of the following nuclear reactions: (n, p), (n, α), or (n, γ). Elastic scattering is more probable for high-energy neutrons and the capture effect is more likely for low-energy ones. The secondary particles generated by the neutron interaction can cause ionization in the targeted material. For example, an alpha particle generated in such a way has very high linear energy and transfer and deposits its whole energy, ionizing the material. Neutrons generally cause displacement damage dose (DDD) and SEEs in targeted devices. The types of particle interactions and the primary and secondary effects they cause are illustrated in Table 2 [16–19].

3. Radiation effects in SRAM-based FPGA

3.1. TID effects

TID effects are dependent on the dose rate, the type of radiation applied, and the internal electric field including space charge effects [20], device geometry [21,22], operating temperature, time after irradiation (annealing or rebound), [23,24] and so on. The ionization radiation effects are responsible for building up of the charge in the SiO_2 and Si/SiO_2 interface. These trapped charges affect the electronic parameters of the MOS transistor, with the threshold voltage (V_{th}) being the most important parameter [25]. The other parameters are a decrease of transconductance, an increase of leakage current, reduction of drain-source breakdown voltage, a deterioration of noise parameters, and reduction in surface mobility [26,27].

n-type metal-oxide-semiconductor (NMOS) transistors are more vulnerable to radiation and cause threshold voltage shift more easily than p-type metal-oxide-semiconductor (PMOS) transistors. The positive threshold voltage can either decrease or increase in NMOS transistors, as shown in Fig. 2 [28]. Initially, the charge sheet moves toward the interface due to positive gate bias voltage; a decrease in threshold voltage happens when the oxide trapped charge (Qot) effect dominates. The threshold value can move to a positive side when the charge deposition increases. The threshold voltage shift in the PMOS transistor is as shown in Fig. 3 [29]. PMOS transistors, due to the presence of holes as charge carriers, are slower and carry less current than NMOS transistors, which has electrons as carriers [30]. Given a constant area of influence of a radiation event, the percentage of area affected of the NMOS is two to three times that of PMOS, and hence, PMOS is more tolerant. In modern processes, short channel effects, such as saturation velocity, reduce this ratio to a much lower value [31]. In this context, an isolated NMOS will be more vulnerable than a PMOS. In another perspective, the change in threshold voltage of MOS devices depends on the electric field in the silicon dioxide [32]. Therefore, the biasing voltage has a significant influence on generated and trapped charge. The threshold voltage shift can be expressed as the sum of two voltage changes caused by the increase of the charge in silica (Q_{ot}) and two interface trapped charges (Q_{it}) [33]. The effect of the trapped charge and the interface state formation are additive in PMOS devices, but for the source of the differential in NMOS devices likely lies in the difference in worst-case logic bias conditions for PMOS and NMOS transistors [34]. The position of the built-up charge strongly depends on the gate bias voltage, and thus, the smaller the distance between the gate terminal and the charge sheet, the less additional electric field is observed and the less the threshold voltage is shifted. The distance is greater for the PMOS transistor because of negative biasing; thus, PMOS is more radiation resistant than NMOS [15]. Charges trapped in MOS oxide will shift the threshold voltage negatively in NMOS, leading to unacceptable drain-source leakage current. In PMOS, the opposite occurs, increasing the threshold and reducing the leakage [35].

3.2. DDD effects

The DDD quantizes the displacement damage to the semiconductor lattice due to the impact of energetic particles. If the transferred energy is higher than the displacement energy, a lattice atom will be removed from its original position in the lattice and a defect will be created [20]. A cascade of disruptions in the silicon lattice is possible with higher energy particle exposure. The main types of displacement defects are vacancy, divacancy, interstitial, Schottky and Frenkel as shown in Fig. 4 [18].

The displacement damage changes the arrangement of the atoms in the crystal lattice, creating lasting damage and increasing the number of recombination centers, depleting the minority carriers, and worsening the electronic properties of the affected semiconductor junctions.

3.3. Single event effects

A SEE is caused by a single energetic particle, which generates an electrical charge in a material depending on the amount of energy the ionizing particle transfers to the material; this process is also known as linear energy transfer (LET) [36]. LET is expressed in $MeV\mu m^{-1}$; it can also be measured in $MeVcm^2g^{-1}$ when it is normalized to the specific mass of the absorbing material [37]. Critical LET, or the LET threshold (LET_{th}), is the maximum LET value deposited by a high-energy particle travelling through a semiconductor device for which failure is not yet observed. When the created electron–hole pairs are expressed as a charge, the minimum charge necessary to create SEE is called the critical charge [38]. The SEEs can be classified as soft errors and hard errors [39], as illustrated in Fig. 5. Hard errors, being nonrecoverable, can permanently damage the hardware in the same way as in the case of a burnout resulting from a short circuit. A soft error is a change in the signal or a data bit flip and can occur in logic modules, I/Os, routing resources, and block random access memory (RAMs)—virtually any part of the FPGA. When a soft error occurs, the device

Table 2
Types of particle interaction.

Radiation type	Energy range	Type of interaction	Primary effects	Secondary effects
Photons	<0.1 MeV	Photoelectric effect	Ionizing phenomena	Displacement damage
	0.3–3 MeV	Compton effect		
	> 1.024 MeV	Pair production		
Neutrons	~0.025eV	Slow diffusion and capture by nuclei	Displacement damage	Ionizing phenomena
	< 10 MeV	Elastic scattering, capture, and nuclear excitation		
	>10 MeV	Elastic, inelastic scattering, various nuclear reactions, and secondary charged reaction products		
Alpha particles	Typical 4–8 MeV	Coulomb attraction	Ionization phenomena	–

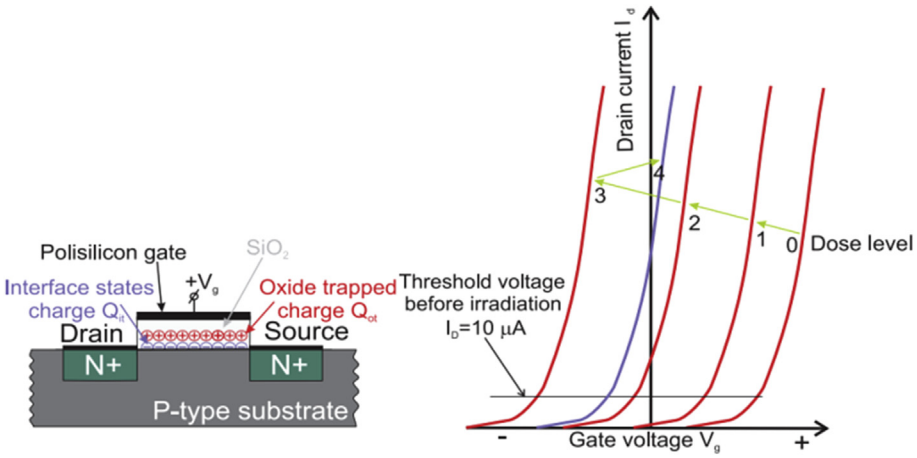

Fig. 2. Oxide and oxide-silicon trapped charge in NMOS transistor together with I_D–V_G curves reflecting shifts in threshold voltage [28].

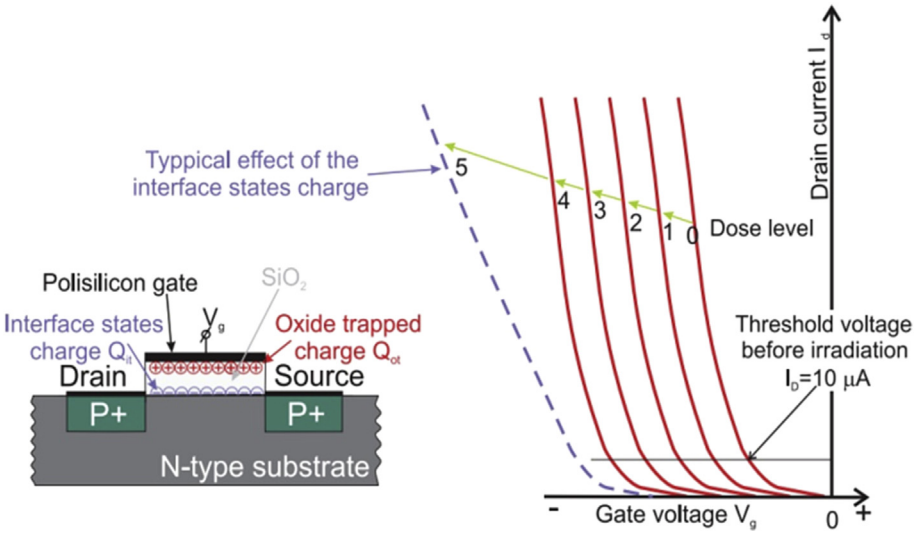

Fig. 3. Oxide and oxide-silicon trapped charge in PMOS transistor together with I_D–V_G curves reflecting shifts in the threshold voltage [29].

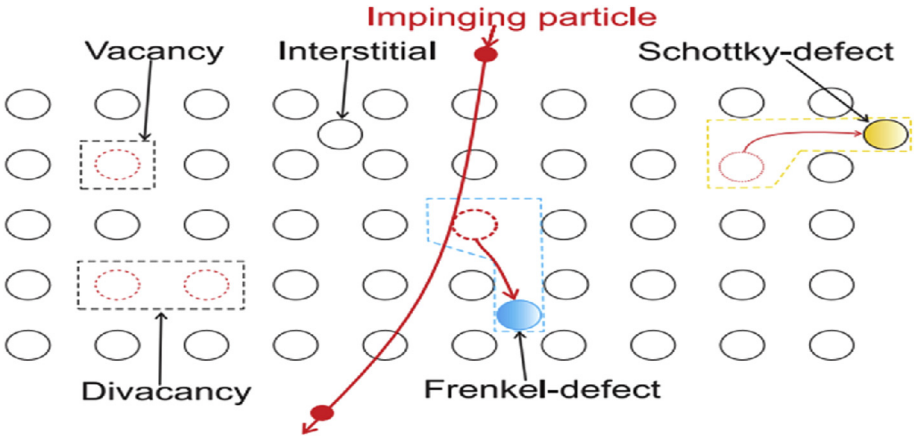

Fig. 4. Displacement damage defects [18].

may still function correctly or may exhibit partial functionality [40]. Unlike hard errors, soft errors can be detected and corrected through special design techniques without having to power-cycle the device.

3.3.1. *Soft errors*

The capacitance and voltage levels of logic circuits have a significant role in the generation of soft errors; the higher these parameter values are, the less probability there is of a soft error

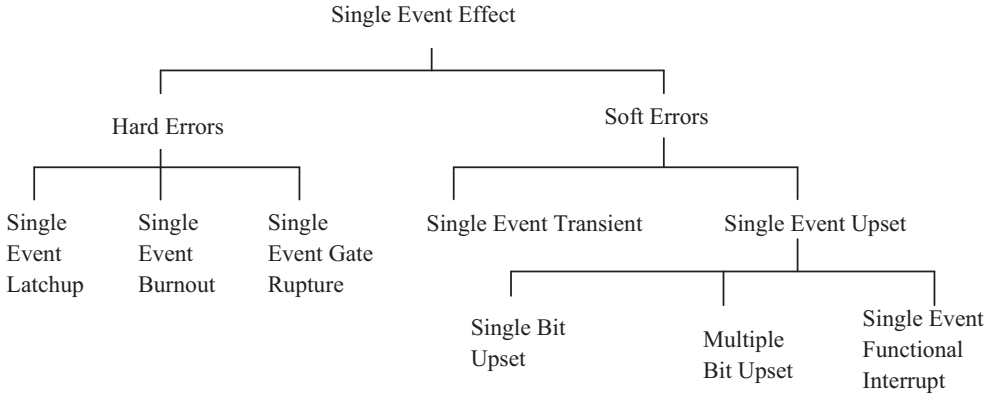

Fig. 5. Classification of single event effects.

generation. The critical charge value varies for each node in the FPGAs. The capacitance of the internal nodes of SRAM cells is very low compared to that of FFs; therefore, it requires less charge deposition to alter the value stored in the SRAM cells. Soft errors are mainly classified into two types: they are single event transients (SETs) or SEUs.

The basic mechanism of soft error generation is illustrated in Fig. 6 [41]. When the charged particles pass through the device material, they generate electron–hole pairs. The most susceptible parts are generally reverse-biased p-n junctions. The charge carriers are collected by the electric field and drift to the nearby node, where a current/voltage transient is created. The majority of the charge is collected by rapid drift process, and this is followed by a diffusion process, as shown in Fig. 7 [41]. A funnel-shaped extension of the depletion region enhances the drift collection; therefore, more charges can be effectively collected at the node [42,43].

3.3.1.1. Single event transient. A SET is a current or voltage spike generated due to particle strikes. SET could be a glitch in the circuit or it may get captured in FFs or other memory elements and can cause a functional error in the operation of the device [44]. SETs are not always harmful to the device and may be transitory in nature. The probability of transient pulse capture is increased by high clock speeds [45]. As SET captures are asynchronous, it is impossible to predict them by static timing analysis. The generation of a transient pulse and its capture are shown in Fig. 8.

3.3.1.2. Single event upset. SEU is a soft error caused by a transient signal induced by a single energetic particle strike when the collected charge is greater than the critical charge required to cause

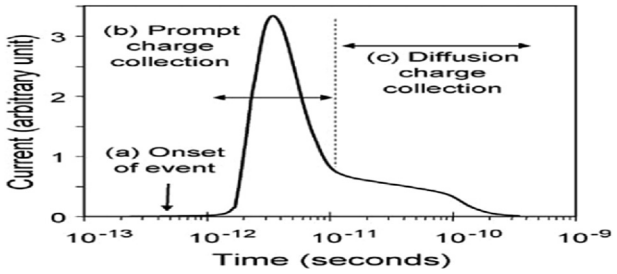

Fig. 7. Current pulse generated due to radiation effect [41].

a change in state of a memory cell, register, latch, or FF. For 0.5 μm technology, the critical charge required to cause an SEU is roughly in the range of femto coulombs. The SEU sensitivity is measured by cross-section and is expressed in cm^2/bits or cm^2/device. The most

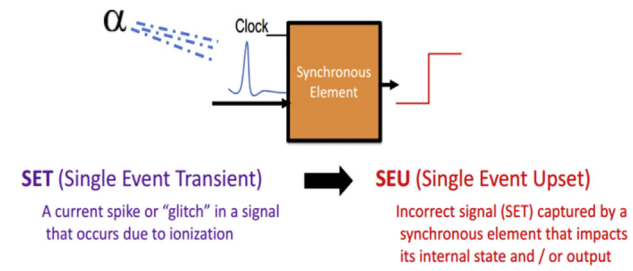

Fig. 8. SET captured in a synchronous element [12]. SET, single event transient.

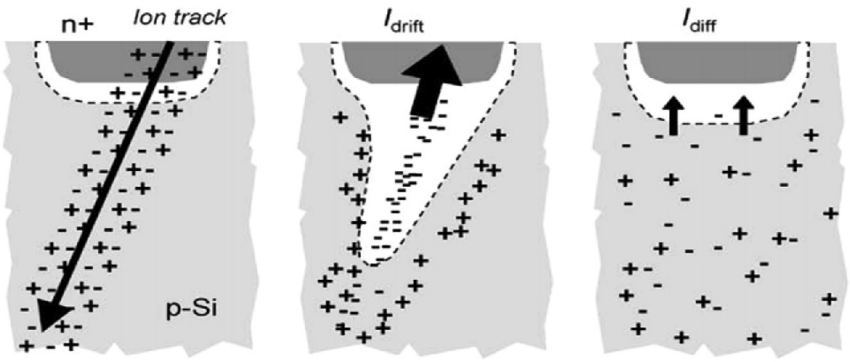

Fig. 6. Charge generation and collection phase in a reverse-biased junction [41].

sensitive regions in SRAM cells are the reverse-biased drain junctions of a transistor biased in the off state [46,47].

SEU generation is dependent on lots of factors such as the LET, particle strike location, charge collection and recovery process, etc.; from a technology standpoint, it depends on the restoring transistor current drive and minority carrier lifetimes in the substrate [48–51]. A bit flip in an SRAM cell is illustrated in Fig. 9 [52].

3.3.1.3. Single bit and multiple bit upsets. A single particle strike can affect either single or multiple memory cells based according to whether it is a single bit upset or multiple bits upset, respectively. A single particle strike can pass through multiple adjacent cells and can cause multiple bit upsets. There are three major principles for multiple bit upset origination: (a) a particle impact angle that allows the particle to pass through more cells; (b) a diameter of the cylinder in which the charge is deposited, that crosses more memory cells such that SEUs may occur there; (c) memory cells that are upset by the products of spallation reactions from the primary particle in the chip [53].

3.3.1.4. Single event functional interrupt. Single event functional interrupt (SEFI) causes the interruption of normal operation of the affected device [54]. SEFI is a special case of SEU in which SEU either occurs in control logic or control over the logic, and the device functionality are lost. SEFI in SRAM-based FPGAs is due to upsets in particular circuits that involve power-on-reset, failures in the joint test action group (JTAG) or select-map communications port, loss of configuration capability, or others [55,56].

3.3.2. Hard errors

3.3.2.1. Single event latchup. Single event latchup (SEL) occurs when the energy released by a particle strike can activate the parasitic thyristor (PNPN structure) embedded in the CMOS architecture [57,58]. When activated, this structure presents positive feedback, causing the involved transistor to start to drain high current [59]. Depending on the resistance, the latchup can be a) fatal when the current density exceeds safe current limits or b) temporal (soft) when a latchup generates heat that further increases current consumption. However, after the power cycle, the device recovers [51]. The SEL typically requires power cycling of the device (when the latchup occurs between the supply voltage and ground) but can also occur within signals where the latchup can be stopped by the change of values.

3.3.2.2. Single event burnout. Even when there is no P-N-P-N structure, an ion strike can turn on a real bipolar junction transistor (BJT) or a parasitic BJT structure in a (usually) n-channel metal-oxide-semiconductor field-effect transistor (MOSFET). The resulting second breakdown causes a high-current state and can cause thermal failure of the device. Due to particle strike, the substrate right under the source region gets forward biased, and the drain-source voltage is higher than the breakdown voltage of the parasitic structures. The resulting high current and overheating may then destroy the device. MOSFETs, BJTs, and some CMOS structures are very susceptible to single event burnouts [60,61].

3.3.2.3. Single event gate rupture. A local breakdown happens in the insulating layer of SiO_2, causing local overheating and destruction of the gate region [62]. Single event gate rupture only affects transistors when they are in their nonconducting states ($V_{GS} \leq 0V$ for n-channel devices or $V_{GS} \geq 0V$ for p channel devices). In the case of single event gate rupture, holes from the ion strike pileup under the gate, thus increasing the electric field across the MOSFET gate oxide to its dielectric breakdown point. The resulting flow of the current causes thermal failure of the gate oxide. These events represent localized breakdowns in the oxide and also can result in latent damage [63].

4. Measurement of radiation upset sensitivity

Before deploying FPGA-based systems in NPP I&C systems, the sensitivity of the device needs to be measured. For this purpose, the device has to be exposed to radiation sources and the consequences have to be analyzed. The main objectives of irradiation experiments on SRAM-FPGAs are listed in [64], they are:

a. Measure SEU sensitivity of configuration memory and block RAM cells (with and without mitigation techniques).
b. Measure SEU sensitivity of input/output blocks (IOBs).
c. Measure SEFI modes (power on reset, SelectMAP, IOB, etc.)
d. Measure the TID effects.

SEE evaluation can be mainly classified into three areas; they are: 1) static: during irradiation the FPGA design is tested in unclocked state, and configuration memory upsets and SEFI failure modes are measured [65]; 2) dynamic: the FPGA design is tested in clocked state and this mainly helps to measure the SETs and also measure SEFIs and IOB upsets; process requires observation to measure the upsets during transient signal propagation [65]; 3) mitigation: after implementing the error mitigation techniques, the FPGA design is evaluated for upsets. The radiation test needs to be conducted mainly to determine faults in the logic resources (LUT error, multiplexer (MUX) error, and FF error) [66] and routing resources (short error, open error, open/short error) [67]. A basic block diagram of the irradiation experimental setup is shown in Fig. 10 [68].

4.1. Measurement of SEUs and TID effects in SRAM-based FPGAs

In the static test, the configuration memory is initialized with a known pattern. Then, during radiation exposure, the FPGA memory

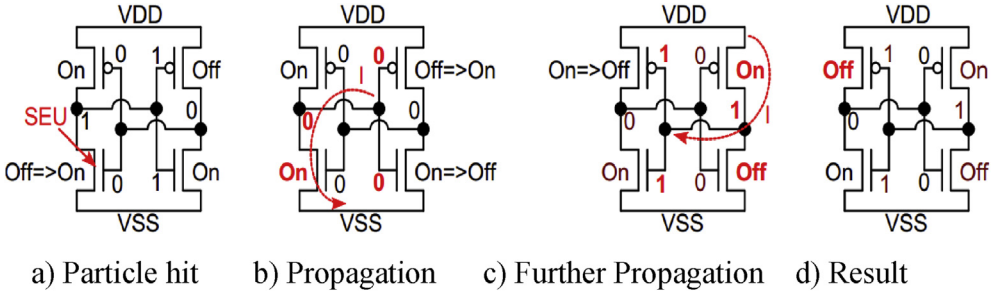

Fig. 9. (A) Particle hits a transistor in off state. (B) Charge is collected by the collector of the left NMOS and creates current I, which discharges gate of the right transistor. (C) Right transistor toggles and enables current to charge gates of left transistors. (D) Left PMOS switches off and the circuit reaches a stable condition [52]. SEU, single event upset.

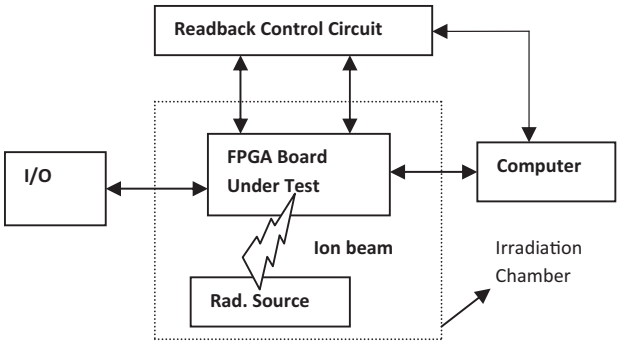

Fig. 10. Irradiation experimental setup [68]. FPGA, field programmable gate arrays; RAD., radiation.

is periodically readback and compared with the expected pattern. The main parameter to determine is the probability that the particle flips a single bit, which is known as a cross-section (σ) and is measured in cm^2/bit or cm^2/device. The device cross-section is defined as the ratio between the number of SEUs (N_{seu}) and the fluence of the hitting particles (ø) given in Equation 1. Fluence is the total number of particles that impinge upon a unit surface area for a given time interval in particles/cm^2. Based on the cross-section value, the sensitivity of the FPGAs to a specific radiation source can be quantified.

$$Crosssection, \sigma = \frac{Nseu}{ø} \quad (1)$$

The expected failure rate of FPGAs can be expressed as FIT. One FIT equals one failure per billion (10^9) hours and is statistically projected from the results of the accelerated test procedures, given in Equation 2. The mean time between functional failures (MTBFF) can be calculated as shown in Equation 3 [69].

$$FIT = Cross\ section \times Particle\ flux \times 10^6 \times 10^9 \quad (2)$$

$$MTBFF = SEUPI \times [1/(Bits \times Cross\ section \times Particle\ flux)] \quad (3)$$

The estimation of the single event upset probability impact (SEUPI) factor is explained in [70]; the particle flux is defined as the rate at which particles impinge upon a unit surface area and is given in particles/cm^2/s. Dynamic tests are conducted in clocked operation mode; the results from the static test can be used as a comparison or a baseline for these tests [65].

TID effects can be evaluated by measuring the propagation delay of different paths of an implemented circuit before and after the device is exposed to radiation. Other parameters that are also the indicators of TID effects are duty cycle response, power supply current, and temperature [71]. There are two main kinds of experiments available. The first is to measure the propagation delay between the input and output; the measurement path includes the I/O logic and the internal logic. The inputs are given from a function generator and delay is measured by comparing the outputs using an oscilloscope or a logic analyzer [71,72]. The second method measures the delay between internal elements, which provides more accuracy [73].

4.2. Irradiation experiments and available results

The total ionization limit for the majority of space applications is 300 Krad (Si) and the LET limit for SEU in both configuration memory and user FF and registers is 37 MeV-cm^2/mg [74]. Total dose testing has demonstrated a tolerance in the range of 80–100 Krad (Si); the testing was done at both high and low dose rates using ^{60}Co sources [75]. The value of immunity to SEL is determined at an LET of 125 MeV-cm^2/mg [76]. The feature size of the process technology also has a role in the tolerance level. The devices with thickness of 0.35 μm can tolerate TID in a range of 0.5–3 KGy (Si) (i.e., 50 Krad to 300 Krad) [77] and devices with thickness of 0.25 μm and 0.18 μm are able to operate at up to dozens of KGy (Si) [78]. The radiation dose limits mentioned above can also be applicable to NPP I&C systems in the normal operating conditions. However, during severe accident conditions, the radiation dose level changes drastically. Severe accident (SA) conditions in boiling water reactors and pressurized water reactors are classified into the following: (1) SA1 is the condition in which the reactor core is damaged, but the core fuel remains inside; (2) SA2 is the condition in which reactor pressure vessel/reactor vessel failure has occurred, and the core has relocated to outside the reactor pressure vessel/reactor vessel; (3) SA3a is the condition in which a primary containment vessel/containment vessel failure has occurred, but water has been successfully injected within 24 h after the safety control rod actuation mechanism (SCRAM), and 4) SA3b: is the condition in which a primary containment vessel/containment vessel failure has occurred and efforts to inject water before 24 h after the scram have failed, but after 24 h have passed successful injection of water occurs [79]. The radiation dose levels during accidental conditions in boiling water reactors and pressurized water reactors are given in Table 3 [79].

There have been lots of experiments conducted at various facilities to measure the sensitivity of radiation upsets in SRAM-FPGAs, mainly for space applications. The results are analyzed mainly based on the source, cross-section, and upsets generated; overall results are illustrated in Table 4.

5. SEU mitigation techniques

The majority of the memory bits in SRAM-based FPGAs are configuration bits. Therefore, the susceptibility of the configuration memory to SEUs is much greater than that of the user memory. Among the configuration bits, the routing resources are critical, in contrast to the bits dedicated to logic resources. The major SEU mitigation techniques available for the configuration memory are depicted in Table 5 [85]. The current state values of the application

Table 3
Radiation levels in BWR and PWR at severe accident conditions.

Plant/environment condition	SA1	SA2	SA3a	SA3b
BWR (radiation dose)	500 Mrad/6months (plant) 30 Mrad/6months (environment outside CV)	500 Mrad/6months (plant) 30 Mrad/6months (environment outside CV)	500 Mrad/6months (plant) 200 Mrad/6months (environment outside CV)	500 Mrad/6months (plant) 200 Mrad/6months (environment outside CV)
PWR (radiation dose)	Below the conventional PAM's environmental conditions	200 Mrad/year (an annular space is 500 Mrad/year)	200 Mrad/year (an annular space is 500 Mrad/year)	200 Mrad/year (an annular space is 500 Mrad/year)

BWR, boiling water reactor; CV, containment vessel; PAM's, post accident monitoring PWR, pressurized water reactor; SA, severe accident.

Table 4
Analysis of irradiation experimental results.

Facility	Source	Device under test	Neutron cross-section (cm^2)	Time of irradiation (hr)	Mean flux (n. cm^{-2}. s^{-1})	Energy (MeV)	FIT/Mb (Config. RAM)	Upsets
IEAv facility, Brazil [80]	^{241}Am-Be	Spartan 6 FPGA (45 nm)	1.45×10^{-15}	261	7.87×10^{3}	Up to 10.5	—	0.38/hr Mean bitstream upsets
ISIS, CCLRC Rutherford Appleton Laboratory [81]	Spallation process	Spartan 6 FPGA (45 nm)	1.37×10^{-14}	2	3.43×10^{4}	10 and above	—	16.45/hr Mean bitstream upsets
LANSCE-UG116 [82]		Spartan 6 FPGA (45 nm)	1.00×10^{-14}	—	—	—	177 (soft error rate per event)	—
LANSCE-UG116 [82]		Spartan 6 FPGA (45 nm)	2.2×10^{-14}	—	—	—	370 (soft error rate per event)	—
LANSCE [83]		Virtex 5 FPGA, (65 nm)	2.29×10^{-9}	97	9×10^{5}	10	—	958 funct.
The Swedberg Lab., Sweden [84]	7Li (p,n) 7Be	XC4010XL (0.35 μm)	4.4×10^{-15}	9	9.3×10^{3}	100	—	5 SEUs

FPGA, field programmable gate array; SEU, single event upset.

Table 5
SEU mitigation techniques for configuration memory.

Mitigation techniques	Mitigation efficiency
Single error correction and double error detection Hamming code with partial reconfiguration [88].	Medium
Scrubbing: post configuration write in the configuration memory; it could be implemented as external, internal as well as software-based and hardware-based [5,89,90].	High
TMR coupled with scrubbing, TMR masks the memory bits during the scrubbing delay thus provides better reliability [91].	High
Use of asymmetric SRAM cells like ASRAM and refreshing SRAM which prevents the bit flips from 0 to 1 and 1 to 0 due to particle strike [92,93].	High
Decoder-based switch box architecture which reduces the number of SRAM cells required to program the switch box [94].	High
Utilizing unused programmable switches to create alternative paths for mitigating open errors in routing resources and replacement of some of the programmable switches in the switch module with a hardwired net for mitigating short errors [95].	Medium
A new switch box architecture which reduces the number of programmable switches in the switch box increases the reliability [96].	High
In place decomposition: it performs logic decomposition and converging within the original logic block which makes the circuit more robust against SEUs [97].	Medium
In place reconfiguration is a resynthesis algorithm does logic transformation while preserving the function and topology of the LUT based logic network [98].	Medium
In-place x-filling: these algorithms take into account of SEUs in LUT configuration bits and interconnect configuration bits [86].	High

LUT, lookup table; SEU, single event upset; TMR, triple module redundancy.

implemented in FPGAs will be in flip-flops and on-chip memories. The combinational logics will be implemented in LUTs, multiplexers and carry logics. The sequential logics will be used in latches and FFs. The control parts of most FPGA-based designs are built using finite state machines, which are implemented mostly in LUTs and FFs. Any bit-flips due to SEE in finite state machines can adversely affect the performance and reliability of the overall system. The techniques used for mitigating SEUs in combinational and sequential circuits implemented in FPGAs are illustrated in Table 6.

The mitigation efficiency of each technique is quantified as low/medium/high based on its benefits, drawbacks, complexity of implementation, and error mitigation capability. Among the scrubbing techniques, external scrubbing gives better reliability even if it requires a radiation hardened auxiliary device. In internal scrubbing, it is better to have triple module redundancy (TMR) coupled with scrubbing; TMR masks the memory bits during the scrubbing delay and provides better reliability. In terms of routing resources, asymmetric SRAM and refreshing SRAM cells give better reliability against bridging errors. The switch module architecture, which utilizes unused switches, provides alternative paths between switch terminals and works efficiently against open errors in routing resources. The replacement of some of the programmable switches with a hardwired net is suitable for short errors. Among the mitigation techniques for logic resources, in-place x-filling has very good reliability because it improves the overall system reliability by mitigating SEUs in the LUTs and interconnects resources [86].

TMR applied to the FFs and logic outputs provides better SEU mitigation efficiency in the user layer. Depending on the scenario, there are three main kinds of TMRs that can be used. They are block TMR, which triplicates combinational logic and FFs; local TMR, which triplicates only the sequential elements, i.e., the FFs; and distributed TMR, which triplicates the entire design except for the global routes. The distributed TMR corrects most of the SEUs [87]. The sequential circuit reliability can be improved by adding a redundant state to states with higher probabilities of occurrence. TMR coupled with error correction codes can improve the SEU mitigation efficiency in a better way by providing additional protection to the memory elements also.

6. Conclusion

For implementation of NPP I&C systems in SRAM-based FPGAs, radiation effects are a major concern. This article has provided an understanding of the sources of radiation and its effects on SRAM-based FPGAs. The mitigation techniques discussed are mainly for SEUs. With the consideration of non-recoverable errors, the authors suggest adopting a combination of the different techniques explained above, along with circuit- or layout-level modifications, improvement in device or manufacturing process techniques or various shielding methods depending on the radiation environment and the level of hardness required for dependable operation of the system implemented in SRAM-based FPGAs.

Table 6
SEU mitigation techniques for user layer.

Mitigation techniques	Mitigation efficiency
Mapping of FSM into synchronous embedded memory block: it enhances the runtime reliability without a significant increase in power consumption [99].	Medium
Duplication with self-checking: duplicating the FSM and inserting a logic block able to detect the error in one of the machines. It is able to auto recover an error provoked by SEU.	High
Triple modular redundancy: three copies of FSM operating in tandem with majority voters placed at the flip-flops and logic output [87,100].	
DWC and CED: a new technique for upset detection and voting that combines DWC with CED based on time redundancy for the user's combinational logic in FPGAs [101].	Medium
Automatic recovery of Single bit errors using Hamming Code [102].	Medium
SEC code (minimum Hamming distance equal to 3) is used with different architectures: single independent decoder block (architecture SID), distributed error correction (architecture DEC), UPset oriented SID (UPS) and upset-oriented DEC (UPD) [103].	Medium
CED for FSMs implemented using embedded memory blocks of FPGAs: the scheme is proven to detect each permanent or transient fault associated with a single input or output of any component of the circuit that results in its incorrect state or output [104].	Medium
Increase the sequential circuit reliability by adding redundant equivalent states to the states with a high probability of occurrence [105].	High
Mapping of FSMs into SEMBs for power and area minimization. Memory array contents are programmed with encoded state bits, the address is formed by combining present state and the input, memory content is next state, and the output [106].	Medium
TMR architecture, duplex architecture, explicit error correction architecture, modified EEC and implicit error correction [107].	High
A design methodology for realizing total self-checking VLSI systems derived from a VHDL description. Innovative state assignment algorithm (based on heuristic), state encoding (based on a constant hamming distance between the present and next state codes). Sequential data-path and output encoding (Berger codes) and SC checkers design have been addressed introducing new techniques [108].	High
Temporal Data Sampling: this stage helps to store data samples at different time intervals. The data samples from “sample release stage” are compared with each other. Data is considered “fault free” if no disagreement is found [109].	Medium
Redundancy addition and removal [110].	Medium
Selective voltage scaling (SVS): the same amount of charge disturbance produces a smaller (less harmful) SET at gates with high supply voltage than at gates with low supply voltage. Assign a higher supply voltage selectively to gates that have large error impact and contribute most to the overall SER, and leave the remaining gates with the nominal supply voltage [111].	Medium
Clock skew scheduling (CSS): The CSS-based approach adjusts the arrival times of clock signals to memory elements (latches or flip-flops) such that the probability of capturing unwanted transient pulses is significantly decreased, as a result of more latching-window masking [112].	Medium
A general method for the synthesis of sequential circuits using embedded memory blocks: it is based on the serial decomposition concept and relies on decomposing the memory block into two blocks; a combinational address modifier and a smaller memory block [113].	Low
BIST is a design technique that allows a circuit to test itself. It is a set of structured test techniques for combinational and sequential logic, memories, multipliers and other embedded logic blocks. BIST controller coordinates the operations of different blocks of the BIST [114].	Medium
ECC and TMR [115].	High
Nonconcurring error detection, identification and correction by appropriately choosing the state encodings and the redundant dynamics of a redundant implementation of the given FSM [116].	Low

BIST, built-in self-test; CED, concurrent error detection; DWC, duplication with comparison; ECC, error correction code; FPGA, field programmable gate array; FSM, finite state machine; SC, self-checking; SEC, single error correction; SEMB, synchronous embedded memory block; SER, soft error rate; SET, single event transient; SEU, single event upset; TMR, triple module redundancy; VHDL, very high speed integrated circuit hardware description language; VLSI, very large scale integration.

As there is no availability of information on past experiences of FPGAs in NPP I&C systems, it is a challenge to design a dependable system using SRAM-based FPGAs in nuclear power plants. The standard international electrotechnical commission (IEC) 62566 provides guidance for FPGA-based solutions for NPP I&C systems, but this standard has not been adopted by most regulatory boards. FPGAs are becoming more complex, with embedded hard microprocessors, digital signal processors, etc.; therefore, extra protection of these modules is also necessary. The major challenge is the quantification of the upset sensitivity of SRAM-based FPGAs; this is still an unresolved problem. Experiments conducted at various facilities have provided different results. Also, available mitigation techniques for the configuration layer and the user layer are not fully efficient. As radiation hardened devices are usually produced in small quantities, there is no guarantee that devices or similar parts will be accessible in the near future. So, it is better to use much cheaper commercially available electronic devices and make them radiation tolerant. Future work involves irradiation experiments on SRAM-based FPGAs to measure the upset sensitivity of the devices, and the function implemented, as well as to measure the feasibility and efficiency of upset mitigation techniques in the NPP environment. This will give information on the preventive measures to be taken before deploying an FPGA-based system in a NPP environment at various operating stages (shutdown, normal operation, and accident conditions). Generally, except sensors, electronics are kept outside the reactor containment building, so future work will be based on how near the reactor the FPGA-based systems can be deployed. This will improve the efficiency of the data acquisition and improve the speed of operation.

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