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Investigation of Junction-less Tunneling Field Effect Transistor (JL-TFET) with Floating Gate

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Abstract—**This work presents a novel structure for junction-less tunneling field effect transistor (JL-TFET) with a floating gate over the source region. Introduction of floating gate instead of fixed metal gate removes the limitation of fabrication process suitability. The proposed device is based on a heavily n-type-doped Si-channel junction-less field effect transistor (JLFET). A floating gate over source region and a control-gate with optimized metal work-function over channel region is used to make device work like a tunnel field effect transistor (TFET). The proposed device has exhibited excellent ID-VGS characteristics, ION/IOFF ratio, a point subthreshold slope (SS), and average SS for optimized device parameters. Electron charge stored in floating gate, isolation oxide layer and body doping concentration are optimized. The proposed JL-TFET can be a promising candidate for switching performances.**

Index Terms—**Tunneling field effect transistor, junction-less field effect transistor, band to band tunneling, floating gate, high-k dielectric**

I. INTRODUCTION

The scaling down of conventional metal oxide semiconductor field effect transistor (MOSFET) beyond 1x nm node has become extremely challenging [1]. The most fundamental limitations in scaling down of conventional MOSFETs are, difficulty in fabrication of metallurgical p-n junctions at source-channel and drain channel interfaces, large doping-concentration gradient and ultra-sharp doping profile and subthreshold slope (SS) at room temperature [2]. The SS of conventional MOSFETs is limited to 60 mV per decade at room temperature [3]. Due to the limitations of scaling down beyond the 1x nm node, various devices have been proposed to replace the conventional MOSFETs for low power applications. The most representative devices are ultra-thin body (UTB) devices, tunneling field effect transistors (TFET), junction-less field effect transistors (JLFET) and multi-gate MOSFETs (gate all around FETs and FinFETs) [4-7]. Recently a new TFET structure named junction-less tunnel field effect transistor (JL-TFET) was proposed which combined together the advantages of both JLFET and TFET [8]. The device was a double gate transistor with heavily n-type doped (1×10^{19} cm^{-3}) silicon channel, extended into source and drain region without any metallurgical junctions. The two gates, control gate over channel region and fixed gate over source region with different work functions were used to provide better controllability over channel and imply work function engineering [9]. The metal work function selection is very important for the selection of metal gate material. If proper metal work function is not selected it leads to degradation of short channel and off characteristics which in turn leads to poor transistor performance [9, 10]. Accurate metal work function is also essential for the alignment of the energy bands between metal and gate dielectric [9, 10]. Even if an appropriate work function is achieved, device fabrication process for integration of two types of metal gates in a device is very challenging [9, 10]. The main problem of the structure was to find a metal gate with

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proper work function for fabrication process suitability.

In this work, a new structure for junction-less tunneling field effect transistor (JL-TFET) with a floating gate is proposed. The effect of floating body has been investigated and applied in the proposed device. A floating body can be used effectively as a storage node in MOS devices [11]. The stored electron charges in the floating body ensures a fully depleted region and can have more holes than doping concentration in the region below it [11]. The energy band can be changed by electron charges in the floating gate and it converts N^+-N^+-N^+ region to N^+-I-P^+ regions and device operates like a conventional TFET. The limitation of finding a metal with proper work function for fabrication process suitability of fixed gate has been removed and replaced by a conventional floating gate in this device. The device performance and characteristics are investigated with commercialized device simulations.

II. Device Structure and Operation

Fig. 1 shows the proposed double-gate junction-less tunnel field effect transistor (JL-TFET) with a floating gate structure. The control-gate (CG) and floating-gate (FG) are isolated from each other by an oxide layer. The lengths and thickness of different layers used in simulation are also defined in Fig. 1. The simulated JL-TFET has a 20 nm heavily n-type (1×10^{19} /cm^3) Si-channel, with source/drain extension lengths of 20 nm. Silicon film thickness is 5 nm, gate oxide thickness is 2 nm, isolation oxide layer is 5 nm and polysilicon FG thickness is 2 nm respectively. To provide better controllability over the channel, the double gate technology is applied to this structure.

All simulations are carried out using Sentaurus TCAD simulator. The nonlocal band to band tunneling (BTBT) model is used in simulation to check the tunneling in lateral direction and predict the performance of TFET [5]. Due to high doping concentration, band-gap narrowing (BGN) model is enabled [12]. Considering interface trap effect and presence of high impurity atom in the channel, Shockley-read-hall (SRH) model is also included.

The optimized work-function of CG and electron charge in the FG are used to make the layer beneath them intrinsic and p-type respectively. To make the layer beneath CG intrinsic, the metal work function has been

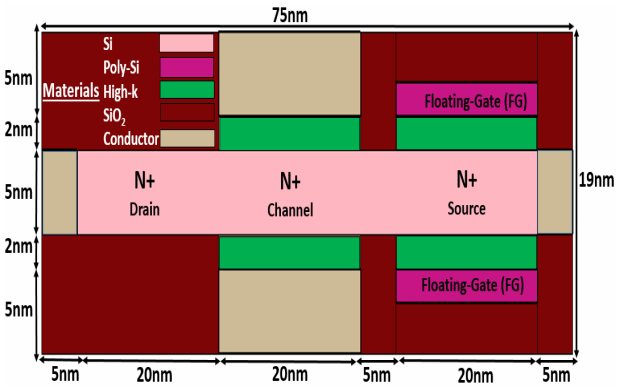


Fig. 1. Schematic diagram of proposed double gate JL-TFET with a floating gate structure. The dimensions and materials used for the device simulation are also mentioned in the figure.

varied from 4.33 eV to 5.1 eV to find the optimized work function. For the proposed JL-TFET, the CG work function is optimized at 4.65 eV. The basic idea here is to convert (N^+-N^+-N^+) drain, channel, source of JLFET into a (N^+-I-P^+) structure without any physical doping as in previous work [8].

III. Results and Discussions

The off-state energy band diagram is shown in Fig. 2(a). The device in the off state looks like an N^+-I-P^+ doped structure and there is a very negligible probability of the tunneling of electron due to the large tunneling barrier in between the source and channel. Thus N^+-I-P^+ diode leakage causes an off-state current flow. When positive voltage is applied on the CG, the device is turned on. Fig. 2(b) shows the energy band diagram of the device in on-state. Applying a positive voltage on CG accumulates electrons in the layer beneath this gate and it becomes an n-type region. As a result the tunneling barrier between the source and channel of the device is narrowed. In a TFET device the on-current (I_{ON}) exponentially increases with narrowed tunneling barrier width [5]. From Fig. 2(b), we can expect that the tunneling barrier is significantly narrowed with CG voltage increase.

Fig. 3(a) shows the off-state and on-state energy band diagrams of the device for different electron charge densities in the FG. The electron charge density in a conventional FG ranges from -1×10^{-15} C/μm^2 to -1×10^{-14} C/μm^2. Thus the electron charge density in the FG for proposed device is varied from -5×10^{-16} C/μm^2 to -8×10^{-14}

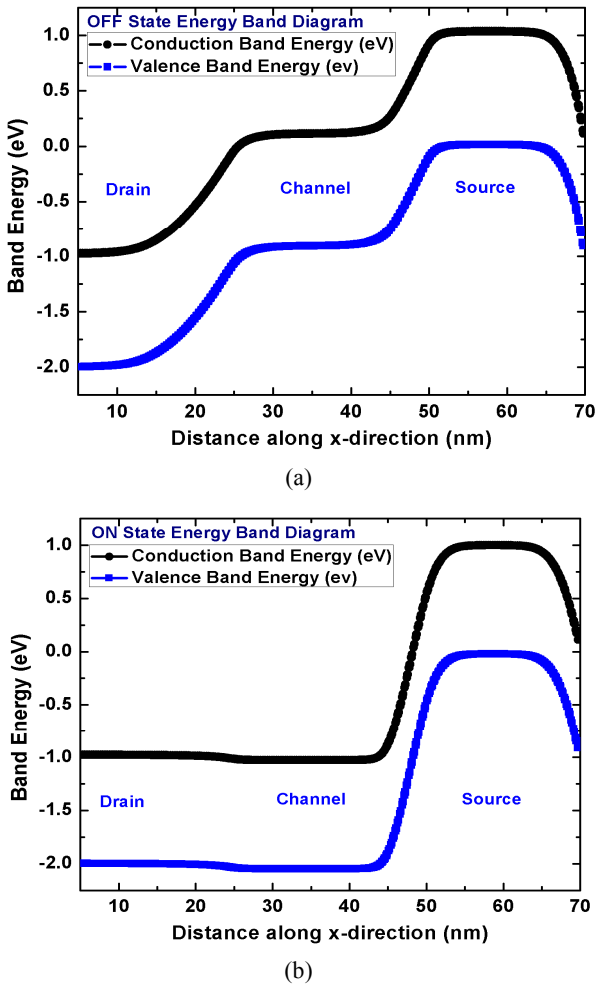


Fig. 2. Energy band diagrams of proposed JL-TFET with a floating gate (a) OFF-state (VDS=1.0 V, VGS=0 V), (b) ON-state (VDS=1.0 V, VGS=2.0 V) energy band diagram.

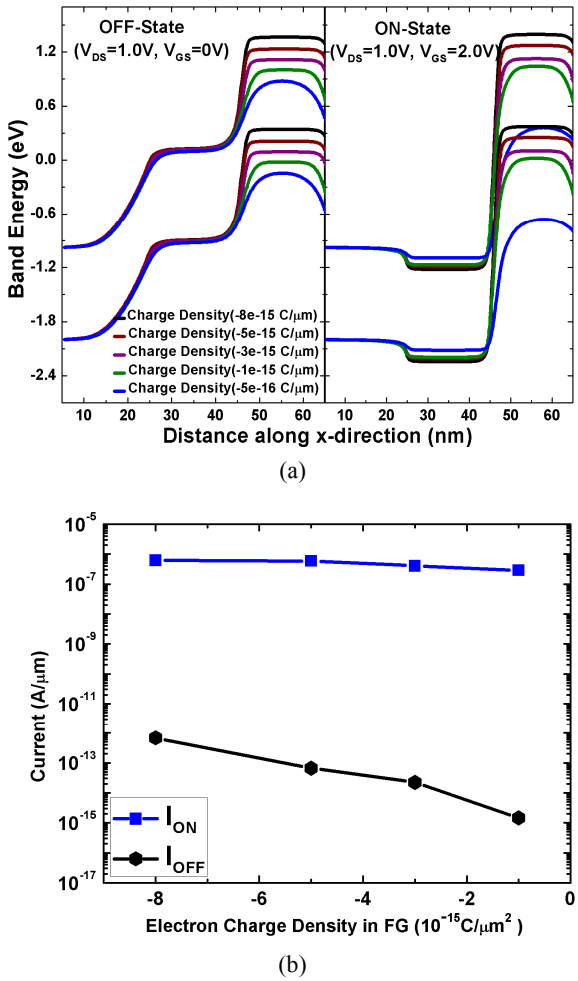


Fig. 3. (a) OFF-state and ON-State energy band diagrams, (b) ON-current and OFF-current of proposed JL-TFET for different trapped electron charge densities in the floating gate.

C/μm^2 to check the effect on the band diagram. From Fig. 3(a) it is evident that increasing the value of electron charge density narrows the tunneling barrier between the source and channel region and increases the probability of tunneling. From the energy bands in the Fig. 3(a) it is also clear that the smaller values of trapped charge density (-5×10^{-16} C/μm^2) has smaller effect on the region below and the probability of tunneling is negligible. The tunneling barrier is drastically narrowed with increase in the values of electron charge density (-5×10^{-15} C/μm^2, -8×10^{-15} C/μm^2), as shown in Fig. 3(a). Hence there is a probability of a leakage current. It is very important to optimize the value of charge density keeping a high probability of tunneling in on-state and a very low I_{OFF} in off-state of the device.

The I_{ON} and I_{OFF} in the proposed device with different electron charge densities in FG are shown in Fig. 3(b). The I_{ON} of the device is calculated with a fixed overdrive voltage (V_{OV} = 0.3 V) for each sample. From Fig. 3(b), the I_{ON} of the device is slightly lowered for smaller values. For charge densities lower than -1×10^{-15} C/μm^2 there is no I_{ON} as there is a very negligible probability of tunneling. The I_{ON} is slightly improved for higher values of charge densities but a very high I_{OFF} is also induced which is critical in power consumption. The optimized charge density of -1×10^{-15} C/μm^2 is selected for the simulations of the proposed device in this work.

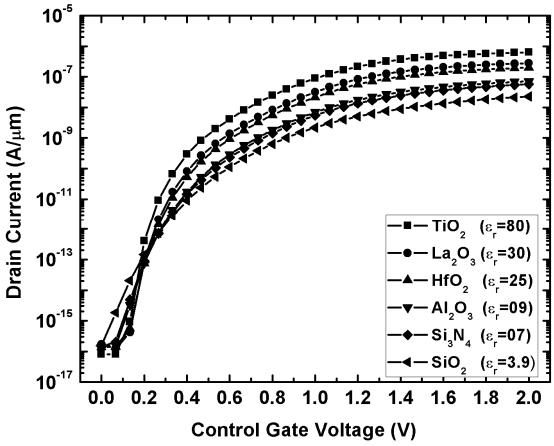
The I_{ON}, I_{ON}/I_{OFF} ratio and SS for TFET's improves by the use of high-k dielectric materials [5, 13]. Although use of high-k dielectric materials is advantageous, it can also lead to defects at the interface of dielectric material and semiconductor. Due to this reason effect of the interface defects is also taken into account. Different gate dielectric materials are considered and their dielectric

constants are taken from previous article [14]. The gate dielectric materials used in this work are, TiO_2 (ε_r = 80), La_2O_3 (ε_r = 30), HfO_2 (ε_r = 25), Al_2O_3 (ε_r = 9), Si_3N_4 (ε_r = 7) and SiO_2 (ε_r = 3.9).

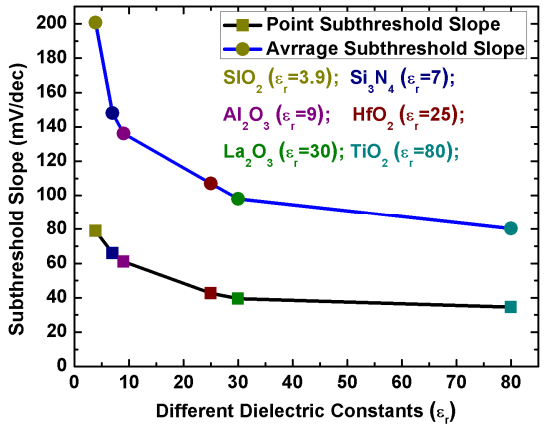
Fig. 4 shows I_{DS}-V_{GS} characteristics, SS and I_{ON}/I_{OFF} ratio for the proposed device with different gate dielectric materials. The physical thickness of gate oxide is kept fixed at 2 nm and different dielectric materials with dielectric constant values ranging from 3.9 to 80 are used. The high-k dielectric material with higher dielectric constant value provides better gate coupling which in turn improves SS and I_{ON}/I_{OFF} ratio. As shown in Fig. 4(a), TiO_2 (ε_r = 80) material with highest dielectric constant has a highest I_{ON} of~6.2×10^{-7} A/μm. All of the high-k dielectric materials also showed a very low I_{OFF} of almost 1×10^{-17} A/μm. The point SS and average SS are shown in Fig. 4(b) and I_{ON}/I_{OFF} ratio is shown in Fig. 4(c) with different gate high-k dielectric materials. Extraction method of the point SS and average SS are same with the previous work [5, 6]. High-k dielectric material TiO_2 (ε_r = 80) with high dielectric constant value has point SS~35 mV/decade, average SS~80 mV/decade and I_{ON}/I_{OFF} of~ 7.8×10^{9} A/μm. Improved point SS and I_{ON}/I_{OFF} ratio for high-k material with lower dielectric constant values (La_2O_3 (ε_r = 30), HfO_2 (ε_r = 25) and Al_2O_3 (ε_r = 9) is observed in the simulation results. The proposed device has shown almost similar values with the device in previous work with similar physical dimensions. Device performance parameters can be optimized according to different physical dimensions of the device.

The FG and CG are separated and isolated from each other by an oxide layer. The inset in the Fig. 5 defines the isolation oxide layer. The thickness of this layer have impact on performance of the device. The thickness of the isolation layer is varied from 2 nm to 8nm to check the impact on performance of the device.TiO_2 material is used as high-k gate dielectric material and the thickness of gate dielectric is kept at 2 nm. Fig. 5 shows the I_D-V_{GS} characteristics of the proposed device with variation in isolation layer thickness. As the thickness of the layer is reduced, an improved I_{ON} and SS is observed. The reduction in thickness of isolation layer has reduced the tunneling barrier between the source and channel which in turn improves I_{ON}.

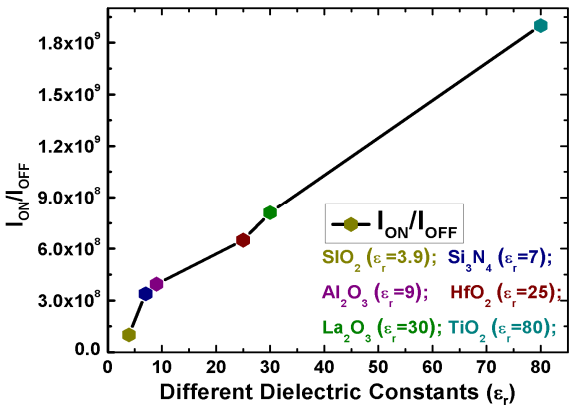
The proposed device has no metallurgical junctions, thus the device doping profile is easy to fabricate. The



(a)



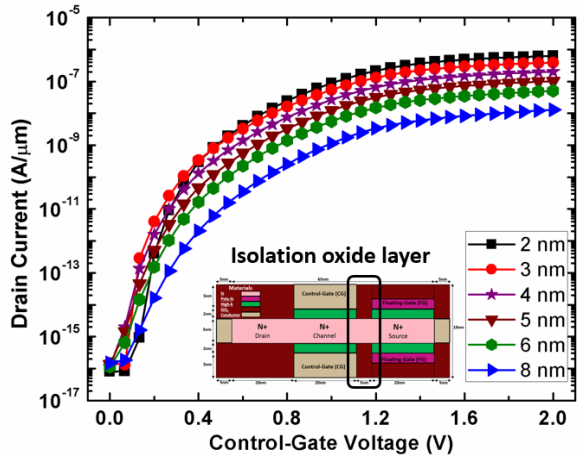
(b)



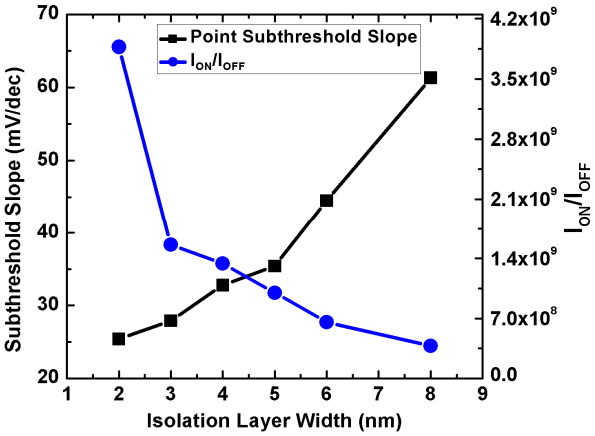
(c)

Fig. 4. (a) I_D-V_{GS} characteristic, (b) point and average SS, (c) I_{ON}/I_{OFF} ratio of proposed JL-TFET with different high-k gate dielectric materials.

doping concentration is varied to check the impact on the device performance and to find an optimized value, keeping other parameters fixed. I_{DS}-V_{GS} characteristics of the proposed device with variation in doping concen-



(a)



(b)

Fig. 5. (a) I_D-V_{GS} characteristics, (b) Point SS and I_{ON}/I_{OFF} ratio of proposed JL-TFET with variation in isolation layer thickness between control gate and floating gate, using TiO_2 as gate dielectric.

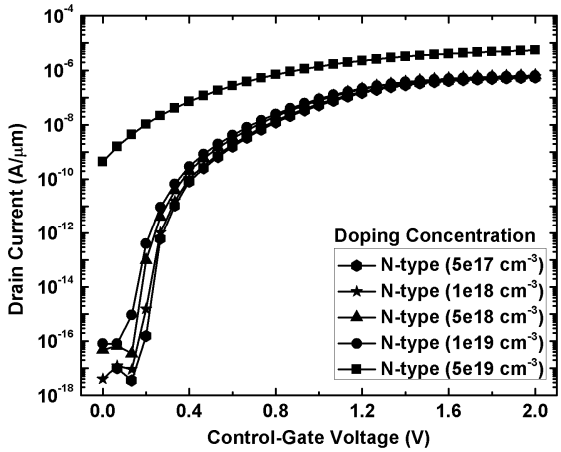


Fig. 6. I_D-V_{GS} characteristics of proposed JL-TFET with variation in body doping concentration, using TiO_2 as gate dielectric.

tration are shown in Fig. 6. The doping concentration is varied from 5×10^{17} cm^{-3} to 5×10^{19} cm^{-3}.

As doping concentration is increased, there is an increase in I_{ON} of the device. But for higher doping concentration than 1×10^{19} cm^{-3}, there is a drastic increase in I_{OFF} of the device which is not desired. Thus using TiO_2 material as gate dielectric with 2 nm width and keeping the isolation oxide layer width 5 nm, the optimized value of N-type doping concentration is 1×10^{19} cm^{-3}. Different optimized values can be achieved for devices with different physical dimensions and parameters.

IV. Conclusions

A new structure for JL-TFET with a floating gate is introduced and basic static operations are investigated in this work. A fixed gate with different metal work function over the source region is replaced by a conventional floating gate which removes the fabrication limitation. Dielectric constant and stored charge density in FG can be used to improve the ION and SS of the device. Excellent ON-OFF characteristics were exhibited by the proposed device in our simulations and seems to be a promising candidate for switching performance.

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References

[1] T. Skotnicki, et al, "The end of CMOS scaling: toward the introduction of new materials and structural changes to improve MOSFET performance," *Circuits and Devices, IEEE Magazine of*, Vol.21, No.1, pp.16-26, Feb.,2005.

[2] R. R. Troutman, "VLSI limitations from drain-induced barrier lowering," *Solid-State Circuits, IEEE*

Journal of, Vol.14, NO.2, pp.383-391, Apr., 1979.

[3] G. V. William, et al, "Figure of merit for and identification of sub-60 mV/decade devices," *Applied Physics Lett.,* Vol.102, No.1, pp.013510(1-4), Jan., 2013

[4] L. Chang, et al, "Direct-tunneling gate leakage current in double-gate and ultrathin body MOSFETs," *Electron Devices, IEEE Transactions on*, Vol.49, No.12, pp.2288-2295, Dec., 2002.

[5] K. Boucart and A. M. Ionescu, "Double-gate tunnel FET with High-κ gate dielectric," *Electron Devices, IEEE Transactions on,* Vol.54, No.7, pp.1725-1733, Jun., 2007.

[6] J-P Colinge, et al, "Nanowire transistors without junctions," *Nat. Nanotechnology*, Vol.5, pp.225-229, Mar., 2010.

[7] J-P Colinge, "Multi-gate SOI MOSFETs," *Microelectronic Engineering, Journal of,* Vol.84, No.9-10, pp.2071-2076, Oct., 2007.

[8] B. Ghosh and M. W. Akram, "Junctionless Tunnel Field Effect Transistor," *Electron Device, IEEE Letters on*, Vol.34, No.5, pp.584-586, May., 2013.

[9] Y-C Yeo, "Metal gate technology for nanoscale transistors-material selection and process integration issues," *Thin Solid Films, Journal of,* Vol.462-463, pp.34-41, Sep., 2004.

[10] W. P. Maszara, "Fully Silicided Metal Gates for High-Performance CMOS Technology: A Review," *The Electrochemical Society, Journal of,* Vol.152, No.7, pp,G550-G555, Jun., 2005.

[11] K-H Park, et al, "Novel Double-Gate 1T-DRAM Cell Using Nonvolatile Memory Functionality for High-Performance and Highly Scalable Embedded DRAMs," *Electron Devices, IEEE Transactions on,* Vol.57, NO.3, pp.614-619, Mar., 2010.

[12] S. C. Jain and D. J. Roulston, "A Simple Expression for Band Gap Narrowing (BGN) in Heavily Doped Si, Ge, GaAs and GexSii-x Strained layers," *Solid-State Electronics, Joournal of,* Vol.34, No.5, pp.453-465, May., 1991.

[13] Y. Khatami and K. Banerjee, "Steep Subthreshold Slope n- and p-Type Tunnel-FET Devices for Low-Power and Energy-Efficient Digital Circuits," *Electron Devices, IEEE Transactions on,* Vol.56, No.11, pp.2753-2761, Nov., 2009.

[14] J. Robertson, "High dielectric constant oxides," *Applied Physics, European Journal of,* Vol.28, pp.265-291, Dec., 2004.

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