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# Advanced ZigBee Baseband Processor with Variable Data Rates for Internet-of-things Applications

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*Abstract*—**In this paper, an advanced ZigBee (AZB) system for internet-of-things (IoT) applications is proposed which can support various data rates from 31.25 Kbps to 2 Mbps, and the implementation results of the AZB baseband processor are presented. Repetition coding for 32-chip direct-sequence spread spectrum (DSSS) symbol is applied for low rates under 250 Kbps to extend the coverage. Convolution coding, puncturing, and interleaving for non-DSSS symbol are performed for high rates from 500 Kbps to 2 Mbps for multi-media services. Simulation results show that the coverage increases at the rate of 51.8-77.3% for various environments compared with IEEE 802.15.4 ZigBee. AZB baseband processor was implemented in 180 nm CMOS process and total gate counts are 260K with the size of 5.8 mm$^2$.**

*Index Terms*—**Advanced ZigBee, direct-sequence spread spectrum, IEEE 802.15.4, internet of things**

## I. INTRODUCTION

With the internet-of-things (IoT) technology, a domain shift for human life is expected towards connected devices and machines which are autonomously requesting and supplying information via wireless networks [1-3]. As the connectivity solution for IoT, IEEE 802.15.4 ZigBee is being considered because of its low-power and low-cost property [4-6]. However, since ZigBee devices support only one data rate of 250 Kbps at 2.4 GHz frequency band, it is difficult to be applied to various applications [7]. That is, sensor network applications such as smart grid systems require longer coverage with lower data rates. However, multi-media applications such as audio/video transmission need higher data rates with shorter coverage. Hence, to overcome the limit of existing ZigBee systems and to satisfy the requirements of various IoT applications, a new definition is needed for the physical (PHY) layer of advanced ZigBee (AZB) systems.

This paper proposes a method of supporting variable data rates from low data rate of 31.25 Kbps that has relatively long coverage to high data rate of 2 Mbps that is capable of high-quality audio and video transmissions. Repetition coding for direct-sequence spread spectrum (DSSS) symbol is applied for low rates from 31.25 Kbps to 125 Kbps, which makes possible the coverage extension owing to the signal-to-noise power ratio (SNR) gain. On the other hand, convolution coding, puncturing, and interleaving for non-DSSS symbol are performed for high rates from 500 Kbps to 2 Mbps, which can be applied to multi-media services within small area. Especially, since the proposed AZB can not only support the data rates of 250 Kbps but also satisfy the spectral mask requirements defined in IEEE 802.15.4 standard, it is backward-compatible with existing ZigBee systems and therefore can be implemented by using existing infrastructure.

The remainder of this paper is organized as follows:

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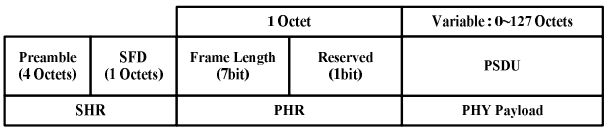


**Fig. 1.** Packet structure of IEEE 802.15.4 ZigBee system.

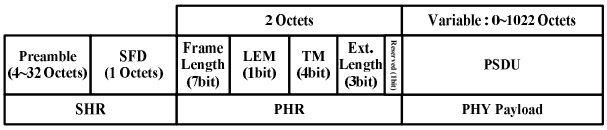


**Fig. 2.** Packet structure of the proposed AZB systems.

Section 2 explains the proposed AZB systems and Section 3 describes the proposed demodulation algorithm for the AZB systems. Section 4 presents the performance evaluation results and Section 5 describes the hardware architecture design and implementation results. Finally, Section 6 concludes the paper.

## II. ADVANCED ZIGBEE SYSTEMS

### 1. System Description

As shown in Fig. 1, the packet structure of IEEE 802.15.4 ZigBee is composed of synchronization header (SHR), PHY header (PHR) and PHY layer convergence protocol (PLCP) service data unit (PSDU). SHR consists of preamble which is 8x repeated index-0 symbols ($S_0$'s) and start-of-frame delimiter (SFD) which is a field indicating the end-timing of preamble. PHR is 8-bit field which includes the frame length information, and PSDU is a data payload whose maximum length is 127 octets [7].

As illustrated in Fig. 2, the preamble in the proposed AZB systems is extended to maximum 32 octets for the time-synchronization in low SNR environment in order to increase the coverage. PHR is also extended to 2 octets for indicating the packet length increase for multi-media applications. Reserved bit in PHR of IEEE 802.15.4 standard is replaced by length-extension mode (LEM) field. That is, if LEM is '1', frame-length field is extended to 10 bits and therefore, PSDU of maximum 1022 octets is supported. If LEM is '0', packet structure is the same as that in IEEE 802.15.4 standard.

The transmission mode (TM) field in PHR of the proposed AZB systems indicates 9 types of transmission modes as shown in Table 1.

**Table 1.** Transmission mode (TM) of the AZB systems

| TM | Data Rate | Spreading / Error Correction Coding |
|---|---|---|
| 0 | 32.15 Kbps | 8x RC for 32-chip DSSS symbol |
| 1 | 62.5 Kbps | 4x RC for 32-chip DSSS symbol |
| 2 | 125 Kbps | 2x RC or 32-chip DSSS symbol |
| 3 | 250 Kbps | 32-chip DSSS (standard-compatible) |
| 4 | 500 Kbps | 2x RC and CC-1/2 for non-DSSS symbol |
| 5 | 1 Mbps | CC-1/2 for non-DSSS symbol |
| 6 | 1.33 Mbps | CC-2/3 for non-DSSS symbol |
| 7 | 1.5 Mbps | CC-3/4 for non-DSSS symbol |
| 8 | 2 Mbps | Unspread and Uncoded |

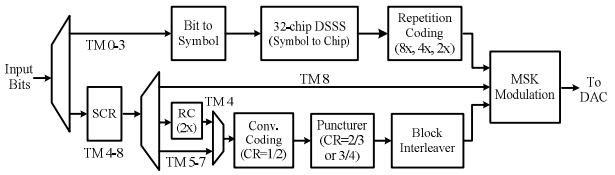


**Fig. 3.** Transmitter structure of the proposed AZB systems.

In case of TM0-3, repetition coding (RC) for 32-chip DSSS symbol is applied for coverage extension with low data rates such as 32.15 Kbps, 62.5 Kbps and 125 Kbps. TM4 is the IEEE 802.15.4 standard-compatible with the data rate of 250 Kbps. In case of TM5-7, scrambling (SCR), convolutional coding (CC), puncturing and interleaving for non-DSSS symbol are applied for multi-media applications with high data rates such as 500 Kbps, 1 Mbps and 1.33 Mbps. Length-127 scrambler is used to prevent the DC component, where the generator polynomial $S(x)$ is given by

$$S(x) = x^7 + x^4 + 1 \tag{1}$$

Convolutional code of code rate (CR) 1/2 is applied to enhance link reliability, of which constraint length K is 5, generator polynomial is $G_1$=23 and $G_2$=35. TM8 supports maximum data rate of 2 Mbps and there is no encoding and spreading. For all TMs, minimum shift keying (MSK) modulation is also applied as shown in Fig. 3, which depicts the transmitter structure of AZB systems.

### 2. Preamble Structure

In order to perform time-synchronization in the receiver, the correlation property for preamble is utilized as shown in Fig. 4. Correlation peak is detected at the location where the received preamble and the correlation window precisely coincide. To enhance the performance

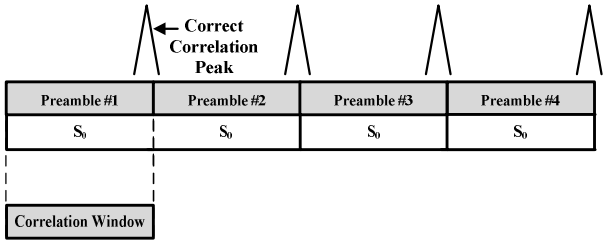


**Fig. 4.** Correlation property for preamble specified in IEEE 802.15.4 standard.

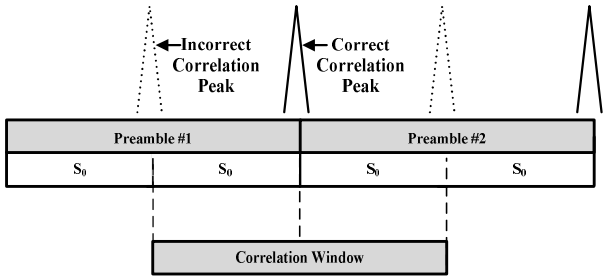


**Fig. 5.** Correlation property for the repeated preamble.

of time synchronization, preamble length needs to be extended for the superior correlation property. New long preamble such as gold code can be applied. However, new preamble requires additional complexity because it needs extra correlator and preamble storage memory. Therefore, the extension of preamble length using repetition coding is better than that using new gold code. However, when doubling the length of preamble by repeating the identical indix-0 symbol $S_0$, correlation peak may appear when the correlation window is located at the middle point of the first and second symbol as depicted in Fig. 5, which makes the accurate time synchronization hard. Hence, a novel preamble transmission structure is required that can improve the performance of time synchronization by increasing the length of preamble, instead of transmission by simply repeating the identical preamble symbol.

Fig. 6 shows the structure of the proposed preamble for AZB systems. The preamble length increases according to transmission mode so that the performance of time synchronization can be improved and no correlation peak is detected in false location. Each of preamble symbol $S_p$, $S_q$, $S_r$ is set at one of the 16 data symbols defined in Table 2, which is also specified in IEEE 802.15.4 standard. Since these DSSS symbols are used for the transmission of information data, extra memory to store the preamble is not needed. The

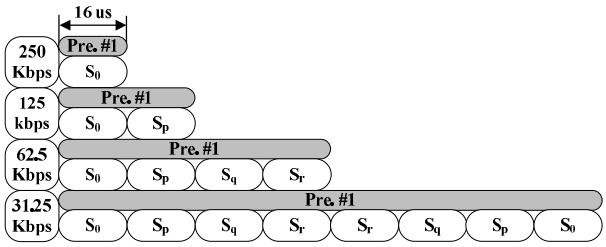


**Fig. 6.** Structure of the proposed preamble.

**Table 2.** 32-chip sequence for DSSS symbol

| Data Symbol | Spread Chip Sequence ($C_0$, $C_1$, ..., $C_{30}$, $C_{31}$) |
|---|---|
| $S_0$ | 1 1 0 1 1 0 0 1 1 1 0 0 0 0 1 1 0 1 0 1 0 0 1 0 0 0 1 0 1 1 1 0 |
| $S_1$ | 1 1 1 0 1 1 0 1 1 0 0 1 1 1 0 0 0 0 1 1 0 1 0 1 0 0 1 0 0 0 1 0 |
| $S_2$ | 0 0 1 0 1 1 1 0 1 1 0 1 1 0 0 1 1 1 0 0 0 0 1 1 0 1 0 1 0 0 1 0 |
| $S_3$ | 0 0 1 0 0 0 1 0 1 1 1 0 1 1 0 1 1 0 0 1 1 1 0 0 0 0 1 1 0 1 0 1 |
| $S_4$ | 0 1 0 1 0 0 1 0 0 0 1 0 1 1 1 0 1 1 0 1 1 0 0 1 1 1 0 0 0 0 1 1 |
| $S_5$ | 0 0 1 1 0 1 0 1 0 0 1 0 0 0 1 0 1 1 1 0 1 1 0 1 1 0 0 1 1 1 0 0 |
| $S_6$ | 1 1 0 0 0 0 1 1 0 1 0 1 0 0 1 0 0 0 1 0 1 1 1 0 1 1 0 1 1 0 0 1 |
| $S_7$ | 1 0 0 1 1 1 0 0 0 0 1 1 0 1 0 1 0 0 1 0 0 0 1 0 1 1 1 0 1 1 0 1 |
| $S_8$ | 1 0 0 0 1 1 0 0 1 0 0 1 0 1 1 0 0 0 0 0 0 0 1 1 1 0 1 1 1 1 0 1 1 |
| $S_9$ | 1 0 1 1 1 0 0 0 1 1 0 0 1 0 0 1 0 1 1 0 0 0 0 0 0 0 1 1 1 0 1 1 1 |
| $S_{10}$ | 0 1 1 1 1 0 1 1 1 0 0 0 1 1 0 0 1 0 0 1 0 1 1 0 0 0 0 0 0 0 1 1 1 |
| $S_{11}$ | 0 1 1 1 0 1 1 1 1 0 1 1 1 0 0 0 1 1 0 0 1 0 0 1 0 1 1 0 0 0 0 0 |
| $S_{12}$ | 0 0 0 0 0 1 1 1 0 1 1 1 1 0 1 1 1 0 0 0 1 1 0 0 1 0 0 1 0 1 1 0 |
| $S_{13}$ | 0 1 1 0 0 0 0 0 0 1 1 1 0 1 1 1 1 0 1 1 1 0 0 0 1 1 0 0 1 0 0 1 |
| $S_{14}$ | 1 0 0 1 0 1 1 0 0 0 0 0 0 0 1 1 1 0 1 1 1 1 0 1 1 1 0 0 0 1 1 0 0 |
| $S_{15}$ | 1 1 0 0 1 0 0 1 0 1 1 0 0 0 0 0 0 0 1 1 1 0 1 1 1 1 0 1 1 1 0 0 0 |

proposed preamble structure is composed such that the required number of preamble symbol is minimized, while maintaining the correlation property. Moreover, to minimize the number of correlators, each first preamble symbol is set to the symbol $S_0$ so that the correlator for $S_0$ can be shared for low-complexity implementation. Also, the correlators for $S_p$, $S_q$, and $S_r$ can be shared as the transmission mode.

## III. DEMODULATION ALGORITHM

### 1. Double-correlation Based Demodulation

There exists maximum frequency offset of ±40ppm in ZigBee systems as specified in IEEE 802.15.4 standard and such offset causes the phase variation for the received signal. Hence, non-coherent demodulation is appropriate for ZigBee systems because it can be performed independently from the phase change of the

received signal. There have been several research results for non-coherent demodulation for ZigBee systems. In [8], asynchronous zero-crossing detection (AZCD) was proposed, which can reduce the complexity by using hard limiter unit and eliminating symbol timing recovery unit. Even though the complexity is quite reduced, its performance is not satisfactory because of hard limiter unit. In [9], maximum likelihood estimation (MLE) based demodulation algorithm was proposed, which shows superior performance owing to matched filter-type cross-correlation. However, this matched filter-type cross-correlation causes the severe increase of the complexity.

Double-correlation based demodulation [10, 11] is one of good solutions, which utilizes the phase difference between the received signal and its delayed version by DSSS symbol period. The received DSSS signal including the frequency offset can be expressed as

$$Y_k(n) = S_k^i(n) \cdot e^{j\omega_0 n+\theta} + W_k(n) \tag{2}$$

where $n$ is the sample index that takes value of 0~$N_s$-1 and $k$ is the time-index for DSSS symbol. $N_s$ is the number of samples that are included in one DSSS symbol. In case of 4x oversampling for 32-chip sequence, $N_s$ becomes 128. $S_k^i(n)$ is $n$-th sample of $k$-th transmitted DSSS symbol and the index $i$ takes one of sixteen DSSS symbols specified in Table 2. $\omega_0$ is the frequency offset and $\theta$ is the initial phase offset. $W_k(n)$ denotes the additive white Gaussian noise (AWGN) for $n$-th sample of $k$-th symbol. In order to detect the transmitted symbol, sixteen double-correlations are performed and the $m$-th ($m \in \{0,1,...,15\}$) double-correlation can be expressed as

$$\begin{aligned} C_{DC}^m &= \sum_{n=0}^{N_S-1} \left(Y_k^*(n)Y_{k-1}(n)\right) \cdot \left(S_k^m(n)\hat{S}_{k-1}^*(n)\right) \\ &= \sum_{n=0}^{N_S-1} \left(S_k^{i^*}(n)e^{-(j\omega_0 n+\theta)}\right)\left(\hat{S}_{k-1}(n)e^{j\omega_0(n-N_S)+\theta}\right)\left(S_k^m(n)\hat{S}_{k-1}^*(n)\right) \\ &= e^{-j\omega_0 N_S} \cdot \sum_{n=0}^{N_S-1} \left(S_k^{i^*}(n)S_k^m(n)\left|\hat{S}_{k-1}(n)\right|^2\right) \end{aligned} \tag{3}$$

For simplicity, AWGN is ignored in (3). Here, $Y_k^*(n)$ is the conjugate of $Y_k(n)$ and $Y_{k-1}(n)$ is the ($k$-1)-th received DSSS symbol. $S_k^m(n)$ is the $m$-th DSSS symbol and $\hat{S}_{k-1}^*(n)$ is the ($k$-1)-th symbol that was already detected. When $i$ is equal to $m$ in (3), $S_k^{i^*}(n)S_k^m(n)$ is expressed as positive integer and hence $C_{DC}^m$ has the maximum value. That is, by finding the maximum value out of sixteen double-correlations, the transmitted symbol can be detected. In (3), the residual frequency offset is fixed at time-irrelevant constant of $e^{-j\omega_0 N_S}$ and its effect on the comparison of correlation results is insignificant because $\omega_0 N_S$ is small number. Therefore, double-correlation demodulation becomes robust to frequency offset.

Meanwhile, double-correlation based demodulation algorithm requires the memory of DSSS symbol length for the storage of the delayed DSSS symbol. In the proposed AZB systems, DSSS symbol is extended eight times and therefore the memory size should be increased eight times. Moreover, as the symbol period $N_s$ increases, the impact of residual frequency offset also increases. Hence, we propose the low-complexity non-coherent demodulation algorithm, which is based on the single-correlation with differential detection for MSK symbol. By using single-correlation, the required memory size can be dramatically reduced.

## 2. Proposed Demodulation Algorithm

Since the phase rotation between the consecutive MSK symbols is ±90° and the 4x oversampling is applied, the product of two consecutive MSK symbols, $s_k^i(n+N_D) \cdot s_k^{i^*}(n)$, makes a sequence which consists of the followings:

$$s_k^i(n+N_D) \cdot s_k^{i^*}(n) \in \left\{-j,\ -\frac{1}{\sqrt{2}}-\frac{j}{\sqrt{2}},\ 1,\ \frac{1}{\sqrt{2}}+\frac{j}{\sqrt{2}},\ j\right\} \tag{4}$$

where $N_D$ is the number of delayed sample, which is four in case of 4x oversampling and $s_k^i(n)$ is $n$-th sample of $k$-th transmitted MSK symbol. By using the correlation for these sequences generated from the product of consecutive MSK symbols, the transmitted symbol can be detected with low-complexity, which is also very similar to the differential detection for MSK symbol.

Single-correlation in the proposed demodulation

algorithm can be expressed as

$$C_{SC}^{m} = \sum_{n=0}^{N_S-N_D-1} D_k^{i*}(n) \cdot D_{ref}^{m}(n) \quad (5)$$

$D_k^i(n)$ is a sequence generated from the product of consecutive MSK symbols in the receiver and is given by

$$\begin{aligned} D_k^i(n) &= y_k(n+N_D) \cdot y_k^*(n) \\ &= \left(s_k^i(n+N_D)e^{j\omega_0(n+N_D)+\theta}\right) \cdot \left(s_k^{i*}(n)e^{-(j\omega_0 n+\theta)}\right) \\ &= e^{j\omega_0 N_D} \cdot \left(s_k^i(n+N_D) \cdot s_k^{i*}(n)\right) \end{aligned} \quad (6)$$

where $y_k(n)$ is $n$-th sample of the $k$-th received MSK symbol. $D_{ref}^m(n)$ is also the $m$-th reference sequence generated from MSK symbol in DSSS symbol in Table 2 and is given by

$$D_{ref}^m(n) = s_k^m(n+N_D) \cdot s_k^{m*}(n) \quad (7)$$

Substituting (5) with (6) and (7), (5) can be expressed as

$$\begin{aligned} C_{SC}^{m} &= \sum_{n=0}^{N_S-N_D-1} D_k^{i*}(n) \cdot D_{ref}^{m}(n) \\ &= e^{-j\omega_0 N_D} \cdot \sum_{n=0}^{N_S-N_D-1} \left(s_k^{i*}(n+N_D)s_k^i(n)\right)\left(s_k^m(n+N_D) \cdot s_k^{m*}(n)\right) \end{aligned} \quad (8)$$

Similarly to (3), $C_{SC}^m$ has the maximum value when $i$ is equal to $m$. The transmitted symbol can be detected by comparing these sixteen correlations. However, unlike (3), the required memory is dramatically reduced by four sample size because the storage of $y_k(n+N_D)$ is just needed. Moreover, since $\omega_0 N_D$ is very small number compared with $\omega_0 N_S$, the effect of the residual frequency offset can be ignored and the performance gain can be achieved.

Table 3 summarizes the required memory size of the proposed algorithm and the existing double-correlation algorithm. As shown in Table 3, the memory size of the proposed algorithm is reduced by maximum 99.6% compared with that of the existing algorithm. Even in case of TM3 that is standard-compatible, the required memory size is reduced by 96.9%.

**Table 3.** Required memory size of the proposed and existing algorithms (unit: word)

| TM | 0 | 1 | 2 | 3 |
|---|---|---|---|---|
| Double-correlation | 1024 | 512 | 256 | 128 |
| Proposed | 4 | 4 | 4 | 4 |
| Reduction rate (%) | 99.6 | 99.2 | 98.4 | 96.9 |

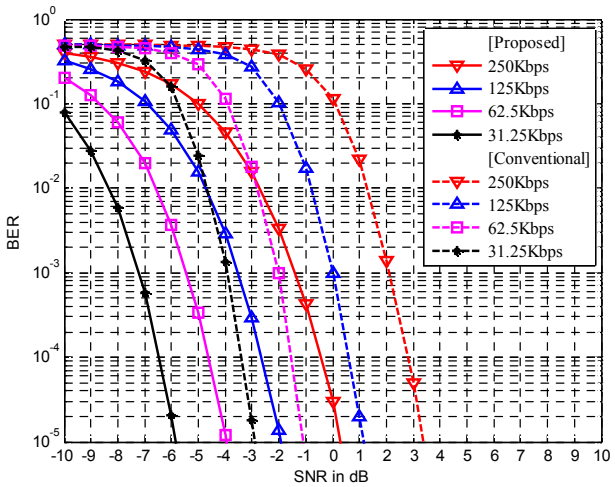


**Fig. 7.** BER performance of the proposed demodulation algorithm and double-correlation algorithm.

## IV. Performance Evaluation Results

Fig. 7 illustrates the bit error rate (BER) performance of the proposed demodulation algorithm and the existing double-correlation algorithm. The frequency offset of ±40 ppm and AWGN were considered. As shown in Fig. 7, the proposed algorithm achieves a SNR gain of 3 dB owing to the reduced effect of the residual frequency offset compared with the double-correlation algorithm.

Fig. 8 shows the packet error rate (PER) performance for the proposed AZB systems. As the data rate decreases, the required SNR also decreases, which means the coverage can be extended. In addition, the performance of TM8 is comparable with that of Bluetooth EDR and therefore it is expected that the proposed AZB system can be utilized for applications of wireless personal area networks (WPANs).

By using the following equation in [12], the coverage performance of the proposed AZB systems were evaluated:

$$\text{Coverage} = 10^{\left(\frac{G_{rx}+G_{tx}+27.6-20\log(F)+G_{ad}+P_{tx}-S_{rx}}{N}\right)} \quad (9)$$

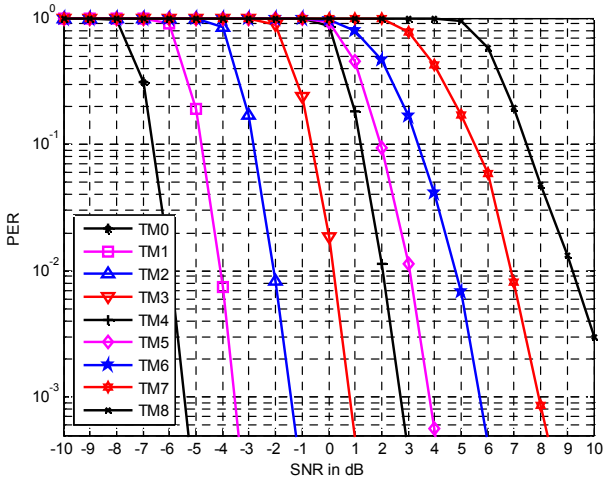


**Fig. 8.** PER performance of the proposed AZB systems.

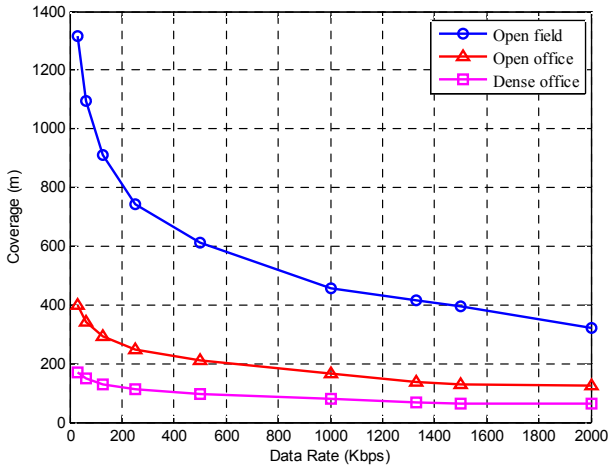


**Fig. 9.** Coverage performance of the proposed AZB systems for various fields.

$G_{tx}$ and $G_{rx}$ denote the antenna gains of transmitter and receiver, respectively. $F$ denotes the operating frequency of 2.4 GHz. $G_{ad}$ is the additional path loss that depends on the object causing the path loss such as wall and floor. $N$ denotes the path loss factor that depends on the field such as open field, open office and dense office. $P_{tx}$ is the transmitter output power and is set to 9 dB. $S_{rx}$ is the receiver sensitivity and is calculated from the PER performance.

Fig. 9 shows the coverage performance for various fields such as open field, open office and dense office. $G_{tx}$ and $G_{rx}$ were set to 0 dB, respectively. $G_{ad}$ was also assumed to be 0 dB. The path loss factor $N$ for open field, open office and dense office were set to 25 dB, 30 dB and 40 dB, respectively. In case of the open field, the coverage of TM0 is extended to maximum 1,317 m,

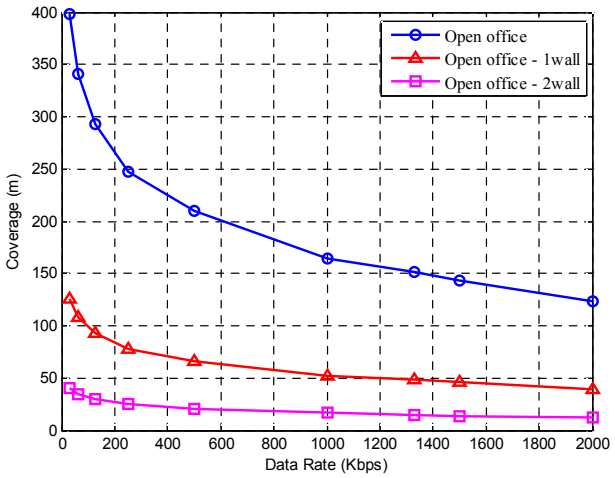


**Fig. 10.** Coverage performance of the proposed AZB systems for various number of walls in case of open office.

while the coverage of the standard-compatible TM3 is 743 m. Even in case of dense office, the coverage of TM0 is elongated to about 169 m, while that of TM3 is 112 m.

Fig. 10 shows the coverage performance for the number of walls in open office environment. The additional path loss $G_{ad}$ for one wall and two walls are set to -15 dB and -30 dB, respectively. Similarly to the results in Fig. 9, the coverage of TM0 is extended to 126 m in case of one wall, while that of TM3 is 78 m. In case of two walls, the coverage of TM0 is elongated to 40 m, while that of TM3 is 24 m. Table 4 summarizes the coverage performance of the proposed AZB systems. It is confirmed that the coverage of the proposed AZB system can be extended to maximum 77.3% compared with that of the existing standard-compatible ZigBee system in case of open field. Even in open office and dense office, the coverage of AZB system can increase by 61.1% and 51.8%, respectively.

## V. Design and Implementation of The Proposed AZB Baseband Processor

Fig. 11 shows the hardware architecture of the proposed AZB baseband processor which can support variable data rates of 32.15 Kbps, 62.5 Kbps, 125 Kbps, 250 Kbps, 500 Kbps, 1 Mbps, 1.3 Mbps, 1.33 Mbps and 2 Mbps. The transmitter of the AZB baseband processor is composed of TX low rate unit (TLRU), TX high rate unit (THRU) and MSK modulator. TLRU supports low

**Table 4**. Coverage performance of the proposed AZB systems

| Path Loss Factor | | $G_{ad}$ (dB) | Transmission Modes (TMs) | | | | | | | | | Increase Rate for TM3 (%) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Field | $N$ | | TM0 | TM1 | TM2 | TM3 | TM4 | TM5 | TM6 | TM7 | TM8 | |
| Open field | 25 | 0 | 1317 | 1095 | 911 | 743 | 610 | 456 | 416 | 395 | 321 | 77.3 |
| Open office | 30 | 0 | 398 | 341 | 293 | 247 | 207 | 164 | 137 | 129 | 122 | 61.1 |
| Dense office | 40 | 0 | 170 | 149 | 130 | 112 | 95 | 79 | 67 | 63 | 61 | 51.8 |
| Open office-1 wall | 30 | -15 | 126 | 108 | 93 | 78 | 69 | 52 | 48 | 45 | 38 | 61.5 |
| Open office-2 wall | 30 | -30 | 40 | 34 | 29 | 24 | 21 | 16 | 14 | 13 | 12 | 66.7 |

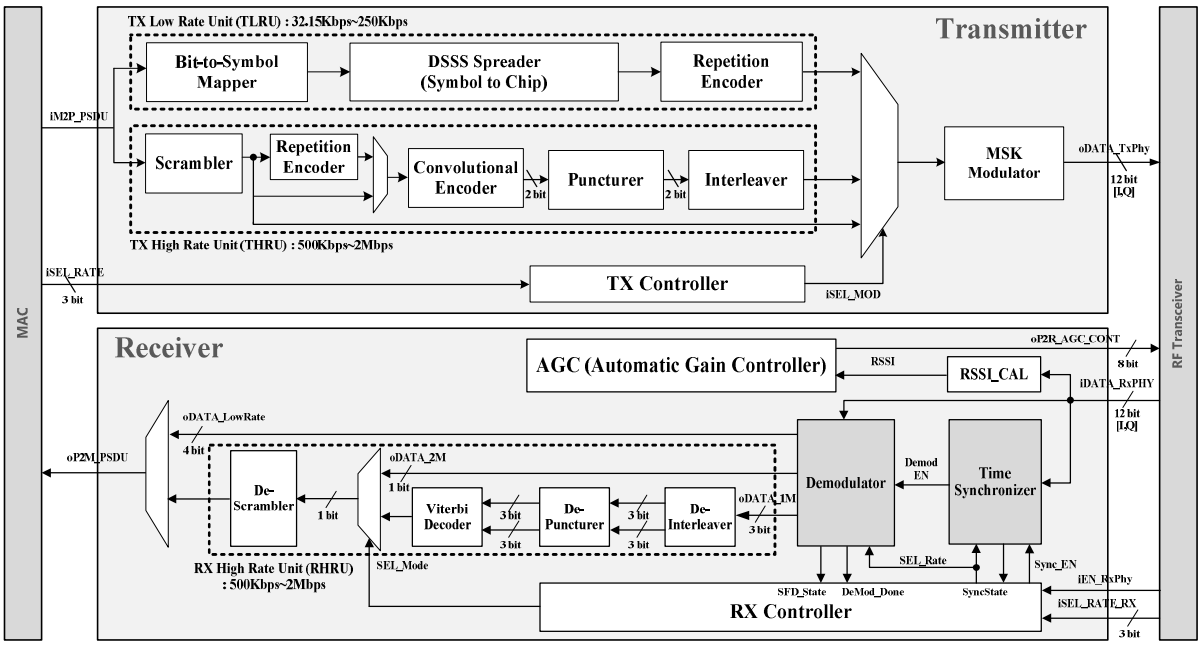


**Fig. 11**. Hardware architecture of the proposed AZB baseband processor.

data rate under 250 Kbps and consists of a bit-to-symbol mapper, DSSS spreader and repetition encoder unit. THRU supports high data rate over 500Kbps and consists of scrambler, convolutional encoder, puncturer and block interleaver. The receiver is composed of automatic gain controller (AGC), time synchronizer, demodulator and RX high rate unit (RHRU). The AGC controls the gain of the amplifier in the RF transceiver to provide a constant amplitude for the received signal. Time synchronizer finds the DSSS symbol boundary by using the matched filter with DSSS symbol size and demodulator detects the transmitted symbol by using the proposed demodulation algorithm. RHRU performs an inverse process to THRU and is composed of de-interleaver, de-puncturer, Viterbi decoder and de-scrambler. One-point scheme is applied to Viterbi decoder for low-complexity implementation, which can perform the write operation 4x faster than the read operation on trace-back memory [13].

The proposed AZB baseband processor was designed in HDL and implemented using a 180 nm 1-poly 6-metal (1P6M) 1.8 V CMOS standard cell library. Table 5 depicts the logic synthesis results for the operating clock frequency of 8 MHz. As shown in this Table, the proposed AZB baseband processor includes about 260K logic gates, which increase by 3.3 times compared to that of the existing ZigBee baseband processor because its gate counts are 76K as presented in [14]. The time synchronizer is the largest block because it requires the matched filter for the extended preamble. Also, it is confirmed that the proportion of demodulator is just 5.29% owing to the proposed demodulation algorithm.

Fig. 12 shows the layout view of the proposed AZB modem chip which includes RF transceiver, analog front-end (AFE), and baseband processor. Total chip size is 14 $mm^2$ and the core size is 12.6 $mm^2$ including RF transceiver and AFE such as analog-to-digital converter (ADC) and digital-to-analog converter (DAC). The size

**Table 5**. Synthesis results of the proposed AZB baseband processor

| Block | | Gate Count (K) | Proportion (%) |
|---|---|---|---|
| TX | | 6.97 | 2.67 |
| RX | AGC | 10.84 | 4.16 |
| | Time Synchronizer | 192.19 | 73.67 |
| | Demodulator | 13.80 | 5.29 |
| | Deinterleaver | 8.11 | 3.11 |
| | Viterbi Decoder | 23.75 | 9.10 |
| | Descrambler | 0.60 | 0.23 |
| | ETC | 4.62 | 1.77 |
| Total | | 260.88 | 100 |

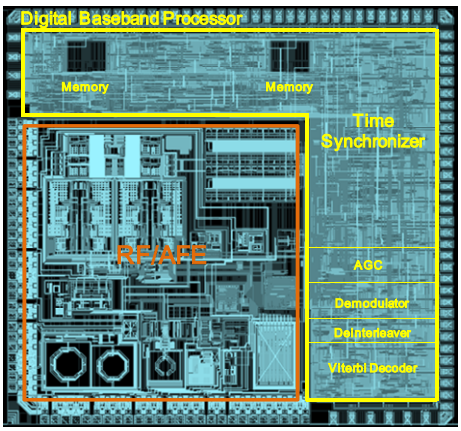


**Fig. 12**. Layout of the proposed AZB modem processor.

**Table 6.** Key features of the fabricated AZB modem

| | |
|---|---|
| Technology | 180 nm 1P6M CMOS |
| Package Type | 128 pin QFP |
| Supply Voltage | I/O : 3.3 V, Core : 1.8 V |
| Clock Frequency | 8 MHz |
| Internal Memory | 64 Byte |
| Area ($mm^2$) | Chip : 3.845 × 3.645 $mm^2$<br>Core : 3.650 × 3.450 $mm^2$ |
| Power Consumption (mW) | TX : 18 mW, RX : 16 mW |

of the digital AZB baseband processor is 5.8 $mm^2$ including two dual-port memories for the verification. Power consumption of AZB modem chip was measured using verification platform. The power consumption of transmitter was 18 mW, while that of receiver was 16mW. The real-time operation of the proposed AZB modem was successfully evaluated. The key features of the fabricated AZB modem chip are summarized in Table 6.

## VI. Conclusions

The AZB system for IoT applications was proposed and the implementation results of the AZB baseband processor were presented. The proposed AZB systems can support various data rates from 32.15 Kbps to 2 Mbps, and can be applied to various applications such as sensor networks in wide area and multi-media services in small area. The proposed AZB baseband processor was fabricated using 180 nm CMOS process with RF transceiver and AFE, and was successfully tested with verification platform.

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