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Planetary 형 반응기에서 웨이퍼와 기판 사이의 틈새가 웨이퍼 온도에 미치는 영향에 대한 연구

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Numerical Study on Wafer Temperature Considering Gap between Wafer and Substrate in a Planetary Reactor

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ABSTRACT

Multi-wafer planetary type chemical vapor deposition reactors are widely used in thin film growth and suitable for large scale production because of the high degree of growth rate uniformity and process reproducibility. In this study, a two-dimensional model for estimating the effect of the gap between satellite and wafer on the wafer surface temperature distribution is developed and analyzed using computational fluid dynamics technique. The simulation results are compared with the results obtained from an analytical method. The simulation results show that a drop in the temperature is noticed in the center of the wafer, the temperature difference between the center and wafer edges is about 5~7℃ for all different ranges of the gap, and the temperature of the wafer surface decreases when the size of the gap increases. The simulation results show a good agreement with the analytical ones which is based on one-dimensional heat conduction model.

Key Words : Planetary reactor, Chemical vapor deposition, Silicon wafer, Heat conduction, Susceptor

1. Introduction

Chemical vapor deposition (CVD) is a widely used technology to manufacture the highest quality semiconductors thin films, which can be used to manufacture electronic or optoelectronic devices such as LEDs, lasers, and solar cells. The planetary reactor technology is based on the principle of horizontal laminar flow. The precursor gases enter the deposition chamber through a nozzle or injector located in the center of the reactor. This inlet permits the separation of several gases. The gases flow radially from the center to the edges of susceptor passing over the wafer surface. This causes the precursor gases to decompose producing gas phase species capable of deposition on the wafer. Each wafer is located on a separate satellite, which is rotating on its individual axis during this deposition process in addition to the susceptor rotating, providing a uniform distribution of the materials across the wafer.

Silicon epitaxy deposition produced by CVD process is one of the most important technological requirements in the semiconductor industry. Silicon has recently become one of the favorite materials in flexible semiconductors development. In epitaxial growth the silicon and dopant atoms are brought to the single crystal surface by gaseous

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transport[1,2]. Silicon epitaxy deposition is a complex dynamical process involving simultaneous mass, momentum and energy transport and complex chemical reactions. Hence, the quality of the films produced will be determined by the interactions of various transport processes and the chemical reactions in the epitaxial reactor chamber, which in turn depend on process conditions such as flow rates, pressure, temperature, concentration of chemical species, reactor geometry, etc. In addition, during the epitaxy process the control of epitaxial film purity is critical to the establishment of electrical properties.

Dichlorosilane (DCS) has been used for silicon growth in many experiments[3-6]. The accurate description of reaction mechanism was conducted by Coon and co-workers[7, 8]. Hierleman et al.[9] introduced a model for silicon epitaxial growth with DCS and showed in his work a simultaneous calculation of velocity, temperature and pressure together with a detailed chemical reaction mechanism.

Current CVD epitaxial growth systems[10] for silicon wafer rely on rotation to achieve uniform growth rate. As larger wafers are used, the effects of chemical component depletion and temperature variation become more pronounced causing non-uniform epitaxial layers. Multi-wafer production reactors employ both susceptor and wafer rotation, so called the “planetary rotation” as a way to average the variation of growth rate on the rotating wafer[10]. This rotation causes an extensive bowing to the wafer. This bowing or gap between the satellite and the wafer influenced by several factors, and it is so difficult to know the actual contact points and the gap size. This gap has a decisive impact on temperature distribution on the wafer surface, which in turn influences the uniformity and deposition rate on the wafer surface. For this reason, the knowledge of the exact wafer temperature is essential for growing high quality devices. Temperature measurement in CVD reactors is usually obtained from a thermocouple, which measures the temperature on or below the susceptor, which might be different from the true temperature of the wafer. In addition, bowing or wafer bending results in temperature variation across the wafer because the wafer loses contact to the susceptor. In recent years, experimental methods have been developed to determine the stress and curvature profile of the wafer during tin film deposition[11-14]. A method for determining the curvature of a substrate using an established temperature profile for the substrate has been developed[15]. However, up to now, no studies have been conducted to investigate the impact of wafer curvature profile on the wafer temperature. Therefore, in this study, we assume that the wafer is flat and there is a gap between the wafer and satellite. And then, we have investigated the effect of gap size on the wafer temperature non-uniformity.

In this study we tried to analyze the temperature non-uniformity of the silicon wafer that might be caused by the gap between the wafer and satellite. To do this a two-dimensional heat transfer calculation is carried out to investigate the gap size influence on temperatures profile of the wafer surface.

2. Modeling Approach

Fig. 1 shows a description of the problem. Fig. 1 (a) shows the main graphite susceptor, the satellite disks, wafers and rotating gas system. Hydrogen enters from feeding point to rotate the satellite by running through semi-spiral channels. DCS, H_2 and HCl mixture enters parallel to wafer. The gap between the satellites and the susceptor, which is the point of interest, is illustrated in Fig. 1 (b).

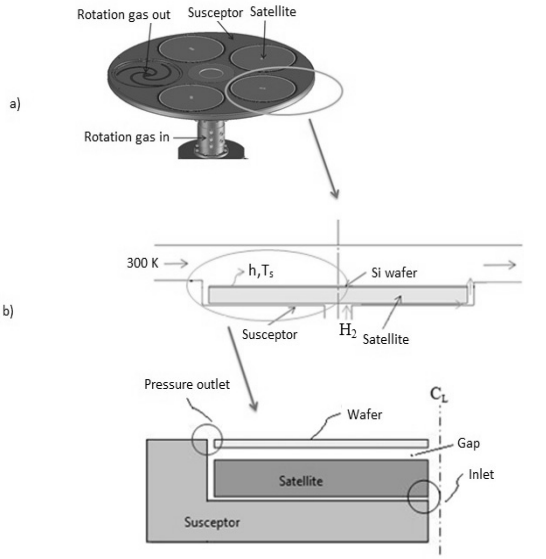

Fig. 1. Schematic representation of the domain under the study, (a) the whole susceptor and (b) detailed view with gap.

Giving convection boundary conditions to the wafer surface instead of including the gas mixture flowing over it reduces the simulation cost and simplifies the domain under study. Therefore, the simulation is divided into two parts. The first part is to calculate the heat transfer coefficient from the wafer to the bulk gas. The second part is to find the gap effect on the wafer surface temperature, which is the main topic of this study. The calculated heat transfer coefficient in the first part is used as a boundary condition in the second simulation.

In the present study, a commercial finite volume code Fluent V17.2 is used for the simulations. For the first part, a mesh system with 12 thousand cells is used, whereas a mesh with around 160 thousand cells is used for the second part. Physical properties of hydrogen are calculated using the kinetic theory because the operating pressure is relatively low. The ideal gas law is used and the flow is modeled as laminar. Governing equations of continuity, momentum and energy for a steady state flow are solved. The second order upwind scheme is employed for the spatial discretization of the advection terms of the governing equations. Constant thermal properties are used for solid graphite parts; the specific heat Cp equals to 720 J/kg-K and the thermal conductivity k equals to 470 W/m-K.

Heat transfer coefficient is assumed to be uniform along the wafer surface. Thickness of the wafer is neglected in this study. Heat transfer coefficient h from the wafer to the bulk gas is found by finding temperature distribution in the area between the wafer surface and reactor ceiling. After plotting temperature distribution as shown in Fig. 2, we calculated the average value of the temperature gradient on the wafer, $\Delta T/\Delta y$, here ΔT is the difference between the cell temperature adjacent to the wall and the wall temperature and Δy is the difference between the two points. Using the temperature gradient, heat transfer coefficient is calculated from the Nusselt number,

$$Nu = \frac{hd}{k_f} = \frac{-\left(\Delta T/\Delta y\right)d}{T_s - T_b} \quad (1)$$

where k_f is the fluid thermal conductivity, d is the wafer diameter, T_b is the bulk temperature of bulk gas and T_s is the susceptor temperature. Determined heat transfer coefficient is 5.88 W/m^2-K and this value is used when a convective heat transfer boundary condition is applied on the wafer in the second simulation.

Fig. 2. Temperature distribution in the reactor used to calculate heat transfer coefficient on the wafer.

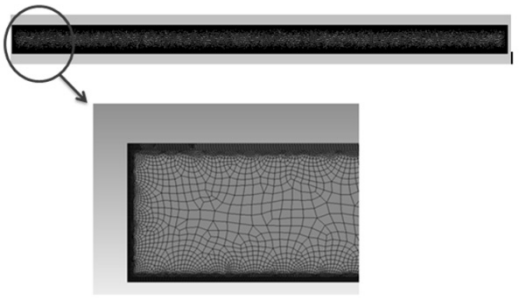

Fig. 3. An example of the eight generated grid systems, the below is the enlarged view of the left edge of the domain.

In the second simulation, to study the gap effect, different girds are generated for all ranges of the gap. Fig. 3 shows one of the generated grids. The minimum size of the cell is 0.05 mm and the total number of cells is around 160 thousand. Different levels of refinement are used near the gap; a smaller gap size requires finer grid. Hydrogen gas enters from feeding point at flow rate of 0.2 l /min. Temperature of the inlet gas is assumed to be 300 K. Two different susceptor temperatures, 873 K and 1003 K and three operating pressures, 10, 30 and 350 torr are considered in the simulations.

3. Results and Discussion

3.1 Numerical calculation results

Relatively low susceptor temperature of 873 K is considered at first. Fig. 4 illustrates velocity and temperatures profiles from the simulations when the operating pressure p is 10 torr. As can be seen in Fig. 4 (a), a stagnation region could be noticed. The left figure shows the contour of the

velocity magnitude and the right figure shows velocity vectors. We can see there is no more gas flow between the wafer and the satellite. In other words there is no convection heat transfer between the wafer and the satellite. Therefore, conduction is the major heat transfer mechanism.

It is found that the behavior of temperature distribution for a given gap size and under different operation pressures is almost the same. Fig. 5 shows wafer temperature profiles for 0.2 and 1 mm gap under 10, 30 and 350 torr. Operating pressure has no significant effect to the temperature distribution in the gap.

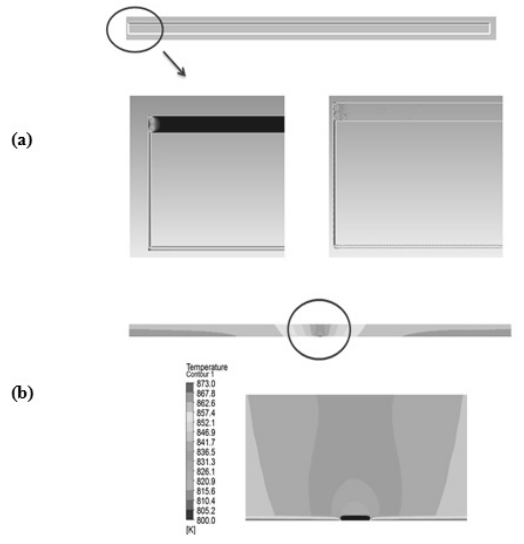

Fig. 4. (a) Velocity profiles and (b) temperature distribution when T_s = 873 K and p =10 torr.

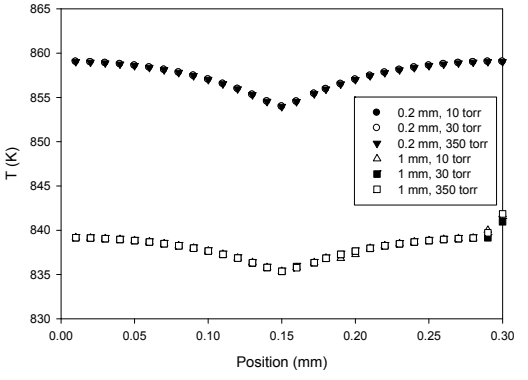

Fig. 5. Wafer temperature according to the gap size, T_s = 873 K and p =10 torr.

Fig. 6 shows temperature profiles along the wafer surface for different gap sizes. A drop in temperature is noticed in the center of the wafer. The drop between the center and wafer edges is between 5~7 K in all situations. However by increasing the gap size the temperature on the wafer surface decreases. Fig. 7 illustrates the temperatures in the center and the edges for all different ranges of the gap. The drop in temperature when the gap size increased from 0.1~1 mm is about 25 K.

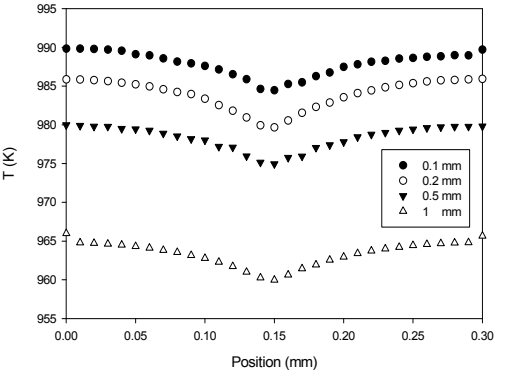

Fig. 6. Temperature profiles along the wafer surface, T_s = 873 K and p =10 torr.

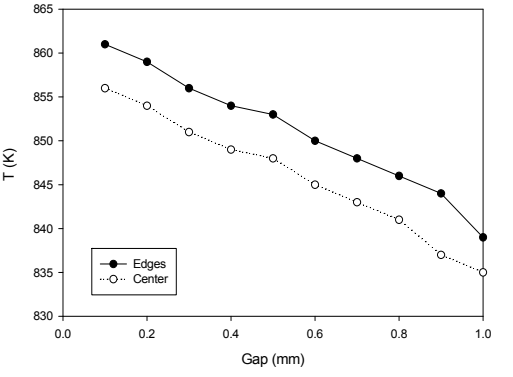

Fig. 7. Wafer temperature according to the gap size, T_s = 873 K and p = 10 torr.

Fig. 8 shows temperature profiles along the wafer surface in different gap size when the temperature of susceptor is 1003 K. The same behavior is noticed here and the temperature drop between the center and wafer edges is between 5~7 K. Temperature drop when the gap size

increases from 0.1~1 mm is also around 25 K as shown in fig.9. Therefore it can be said that temperature drop due to the gap between a wafer and susceptor is not affected by the susceptor temperature.

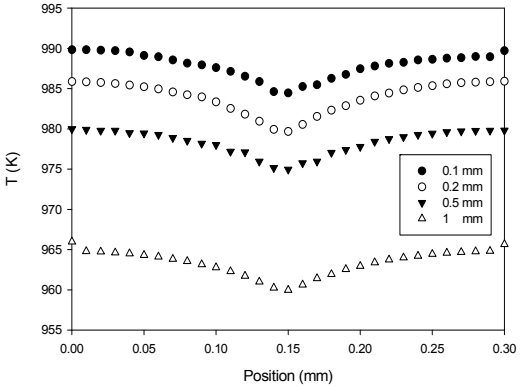

Fig. 8. Temperature profiles along the wafer surface, T_s = 1003 K and p =10 torr.

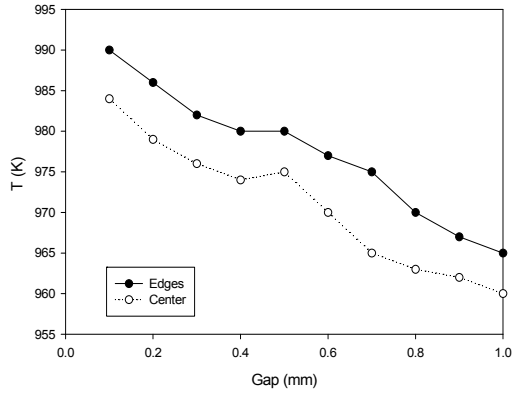

Fig. 9. Wafer temperature according to the gap size, T_s = 1003 K and p =10 torr.

3.2 Analytical results

The simulation results of the temperature distribution showed that there is no convection heat transfer between the wafer and the satellite. This reason made us to simplify the model to the one-dimensional conduction problem. For one-dimensional heat conduction the heat transfer rate is given as,

$$Q = \frac{T_s - T_w}{R_t} \tag{2}$$

where T_w is the wafer surface temperature and R_t is the total thermal resistance. The total thermal resistance from the susceptor to the wafer shown in Fig. 1 (b) is the serial network of the three thermal resistances. Therefore, R_t is the summation of each thermal resistance,

$$R_t = R_{g1} + R_s + R_{g2} \tag{3}$$

where R_{g1} is the resistance for the gap between the wafer and the satellite, R_s is the resistance of the satellite itself and R_{g2} is the resistance of the gap between the satellite and the susceptor. Since the gap between the satellite and the susceptor is constant, R_t is proportional only to the gap size between the wafer and the satellite. Table 1 lists the values used in calculations.

Table 1. Values used to calculate the thermal resistance

Variable	Value	Unit
y_{g1}	0.1~1	mm
y_s	34	mm
y_{g2}	0.3	mm
k_{g1} , k_{g2}	0.167	W/m.K
k_s	470	W/m.K

Fig. 10 shows the comparison between the simulation and the analytical results for (a) T_s = 873 K and (b) T_s = 1003 K, respectively. The figure shows that the analytical results are in a good agreement with the edge temperatures than the center temperatures. This agreement is reasonable since the hydrogen in our simulation enters the inlet with a temperature lower than the suscepetor temperature and thus reduces temperatures in the center of the wafer. In the analytical study, we consider it as a conduction problem thus the effect of the inlet is ignored making the very close agreement with edge temperature. Based on these results, the uniformity and growth rate of silicon on the wafer can be predicted using the dependence of the growth rate on substrate temperature. Deposition rate might decrease as the gap size increases due the drop in temperature. The relatively small drop in temperature between the center and wafer edge could results in a small difference in deposition rate of silicon across the wafer surface.

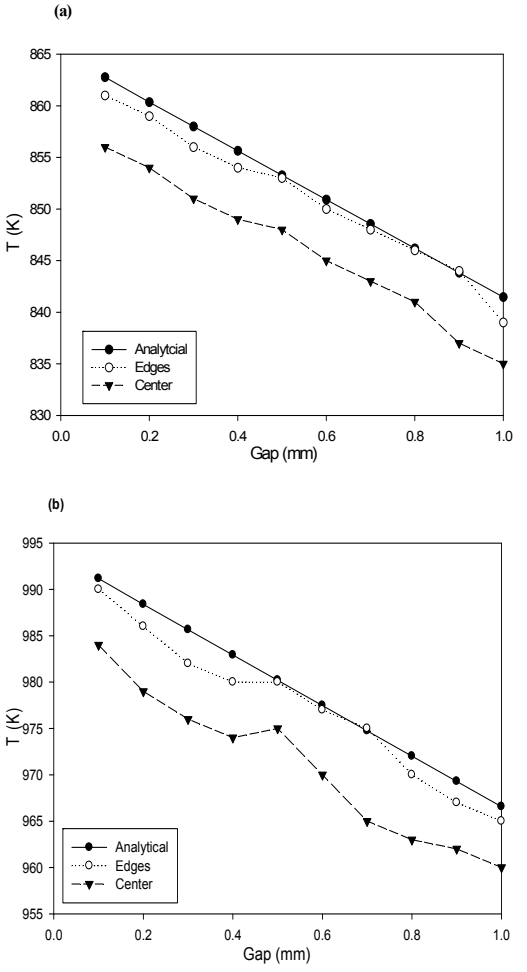

Fig. 10. Comparison between the simulation and the analytical results for (a) T_s = 873 K and (b) T_s =1003 K.

4. Conclusion

In this study, a two-dimensional model for estimating the effect of the gap between satellite and wafer on the wafer surface temperature distribution is proposed. The gap between the satellite and the wafer is increased gradually form 0.1 mm to 1 mm, and all case are studied under several operation conditions for pressure and susceptor temperature. Computational results of heat transfer show that a drop in temperature can be noticed in the center of the wafer. Increasing the gap size increases temperatures drop of wafer surface. The difference in temperature between the center and the edge remains the same for all gap sizes. The analytical calculation of one-dimensional heat conduction as the simplified model showed a good agreement with the computed results.

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Nomenclature

Cp :	Specific heat at constant pressure
k :	Thermal conductivity
T :	Temperature
p :	Pressure
h :	Heat transfer coefficient
d :	Wafer diameter
Nu :	Nusselt Number
Q :	Heat transfer rate
R :	Thermal resistance

Subscripts

s :	Susceptor
w :	Wafer
f :	fluid
b :	Bulk gas
g1 :	Gap between wafer and satellite
g2 :	Gap between satellite and susceptor

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