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Reactive Ion Etching Process Integration on Monocrystalline Silicon Solar Cell for Industrial Production

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ABSTRACT: The reactive ion etching (RIE) technology which enables nano-texturatization of surface is applied on monocrystalline silicon solar cell. The additional RIE process on alkalized textured surface further improves the blue response and short circuit current. Such parameter is characterized by surface reflectance and quantum efficiency measurement. By varying the RIE process time and matching the subsequent processes, the absolute efficiency gain of 0.13% is achieved. However, the result indicates potential efficiency gain could be higher due to process integration. The critical etch process time is discussed which minimizes both front surface reflectance and etching damage, considering the challenges of required system throughput in industry.

Key words: Monocrystalline silicon, Passivation, Reactive ion etching, Reflectance, Surface texture

1. Introduction

Reactive ion etching (RIE) has been widely adopted in silicon PV industry for high efficiency "black silicon" product. The industry-scale RIE system has demonstrated absolute efficiency gain of more than 0.6% abs. for multicrystalline silicon solar cell[1-3]. The RIE process relies on self-masking mechanism in which the plasma ions react with silicon to form polymer mask and also remove unmasked wafer surface as cyclic process. Its anisotropic etching process independent of crystal orientation is applicable to replace conventional wet texturing as well as removing grain boundaries. The role of nano-textured surface is known to improve the short circuit current by enhanced blue response of spectrum and thereby the conversion efficiency of solar cell[3-5]. The same technique could apply for monocrystalline wafer with appropriate surface conditioning. However, high quality monocrystalline wafer is more sensitive to plasma etching damage than multicrystalline wafer. The relative efficiency gain against process cost needs to be measured for industrial application.

In this paper, the RIE process is applied on top of micro-textured surface of monocrystalline wafer, which enables simple integration with formal mass production process. The RIE system parameters such RF power, pressure, gas ratio of $SF_6/O_2/Cl_2$ were kept constant and only etch time was varied. In this way the total surface area can be monitored based on sheet resistance and deposited film thickness which are linearly correlated with etch time. We confirmed the reflectance gain becomes trivial beyond a certain etch process time. This corresponds to 150 s with etch depth limited to 500 nm for nano-texturing. Considering the throughput for industrial process, the maximum reflectance gain is found in 100 ~ 110 s. Beyond this etch time causes severe wafer edge discoloration after plasma enhanced chemical vapor deposition (PECVD) process due to chemical discontinuity at the edge.

2. Experiment

Industrial monocrystalline 6 inch p-type silicon with thickness of 180 μm and resistivity of 1 ~ 3 ohm-cm is employed. The conventional aluminum back surface field (Al-BSF) manufacturing steps include alkaline texturing and phosphorous diffusion followed by PSG removal and junction isolation via inline wet process. High quality passivation is then obtained by growing thin thermal oxide layer and depositing SiN_x layer with PECVD process. The front and rear contacts are screen printed with silver and aluminum paste and co-fired at peak temperature of 850°C. The additional RIE process is implemented prior to diffusion process, and subsequent surface cleaning is performed to remove the residual of RIE byproduct such as fluoride

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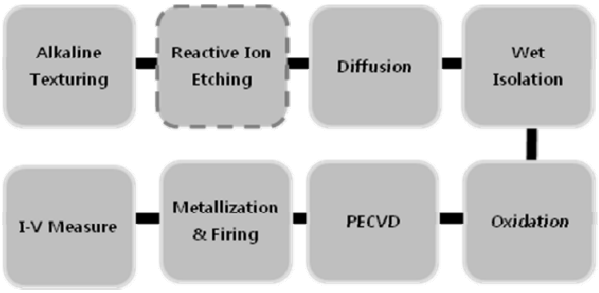

Fig. 1. RIE cell fabrication flow chart

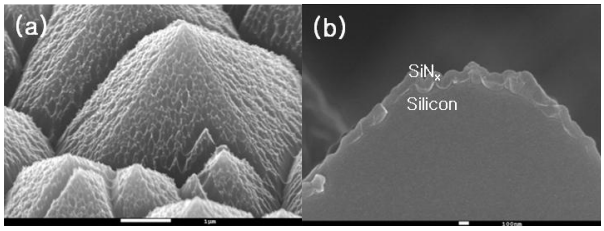

Fig. 2. (a) RIE textured morphology and (b) cross-sectional view of deposited SiN_x film on RIE surface

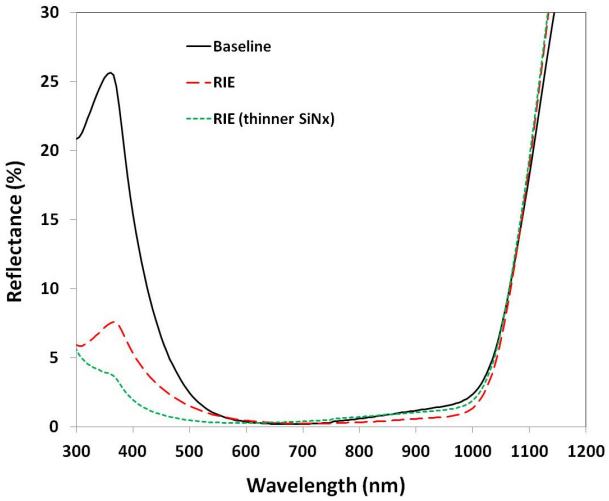

Fig. 3. Reflectance of front surface after SiN_x film deposition on both sides of wafer by PECVD

powder. The simplified process flow diagram for Al-BSF cell fabrication with RIE is described in Fig. 1.

Emitter sheet resistance and implied V_{oc} are measured for both RIE cell and our baseline. The doping profile is also checked by ECV for applicability of the junction depth. In order to have proper passivation and minimum reflectance, either the PECVD process time or deposition rate needs to be increased. The samples are split into having SiN_x thickness (1) equivalent to the baseline, (2) 10 ~ 15 nm thinner than the baseline. As for the production throughout, thinner SiN_x layer is also recommended for starting point.

3. Results and Discussion

The surface morphology of our baseline and RIE processed for 100 s is characterized by SEM as shown in Fig. 2. The nano-scale RIE surface is visible on pyramid formed by alkaline texturing process while the tips are slightly rounded in (a). The SiN_x film is uniformed deposited on RIE textured surface after PECVD process can be observed in (b). The valleys of pyramid have sharp transition surface and there are some chance of having voids which directly affect surface recombination. SiN_x layer thickness of 80 nm or above provides better step coverage, but thinner film below 80 nm is more effective in utilizing nano-textured surface reflectivity at short wavelength. As an alternative, RF power and pressure of PECVD process can be adjusted to produce more dense films and prevent voids problems for film below 80 nm.

Fig. 3 shows the reflectance of all samples from 300 nm to 1200 nm after passivated with SiO_2/SiN_x, and their average weighted reflectance (AWR) measured at AM1.5 is calculated. The AWR of all RIE processed samples is below 4% as a result of improvement in both short and long wavelength, with the short wavelength improvement being the dominant one. The largest reflectance gain can be seen on the RIE sample with SiN_x deposited 10 ~ 15 nm thinner than our baseline, which also appears to be more black. However, the difference in short wavelength below 550 nm gain is more dependent on the RIE process time matched with bare wafer condition and corresponding PECVD process time while the improvement in the long-wavelength above 700 nm is usually controlled by the SiN_x thickness. The improvement in the long-wavelength response is expected to contribute more on passivated emitter rear contact (PERC) structure because such structure is much more efficient at long wavelength light compared to the conventional AL-BSF structure[6].

The implied V_{oc} is an important parameter for diagnosing passivation quality ahead of the metallization step. Because the surface has been enlarged, the trade-off between surface recombination and reflectance gain is addressed. The challenge is to minimize recombination by passivation processes. Fig. 4 shows the implied V_{oc} after PECVD process. To achieve symmetric passivation, the same thickness of SiN_x on rear side is also deposited. For samples before fast firing, the implied V_{oc} is determined by how much SiN_x film is deposited and amount of hydrogen contents in it. The actual thickness between the RIE

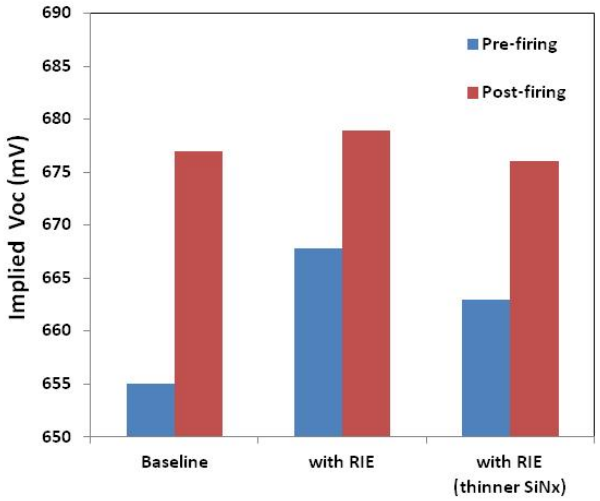

Fig. 4. Passivation quality before and after fast firing process as measured by QSSPC technique

Table 1. I-V parameters of fabricated samples

	Pm [W]	Voc [mV]	Jsc [mA/cm^2]	Rsh [Ω]	Rs [mΩ]	FF [%]	Eff [%]
Baseline (80 nm SiNx)	4.813	642.9	38.19	89	4.41	80.2	19.70
RIE (80 nm SiNx)	4.845	641.7	38.46	23	4.15	80.4	19.83
RIE(<70 nm SiNx)	4.830	640.3	38.34	46	4.19	80.5	19.77
RIE(>90 nm SiNx)	4.772	643.1	38.01	62	4.55	79.9	19.53

sample and our baseline is similar, but the deposition process time of two differs by more than 50% in order to compensate for increased surface area. The longer deposition time is expected to improve the hydrogenation during the deposition which leads to higher implied V_{oc} values for RIE processed samples before firing. The firing process enables further hydrogenation from the SiN_x film into emitter layer and improves surface passivation resulted in a vast improvement in implied V_{oc} after firing[7]. The implied V_{oc} after firing is influenced by the combination of RIE induced defect and hydrogenation of the surface.

The trend of SiN_x thickness on RIE process is evident at cell level. Another set of wafers is processed with SiN_x layer 10 ~ 15 nm thicker than the baseline to see if high V_{oc} can be maintained. The cell with thicker SiN_x layer indeed exhibits a higher V_{oc} but less light can penetrate to the front surface and the generated current is reduced. Moreover, a much lower fill factor and a relatively high series resistance (Rs) suggest that the peak temperature of 850°C could not form good front contact with this thick SiN_x layer (> 90 nm). In case of the thinner SiN_x,

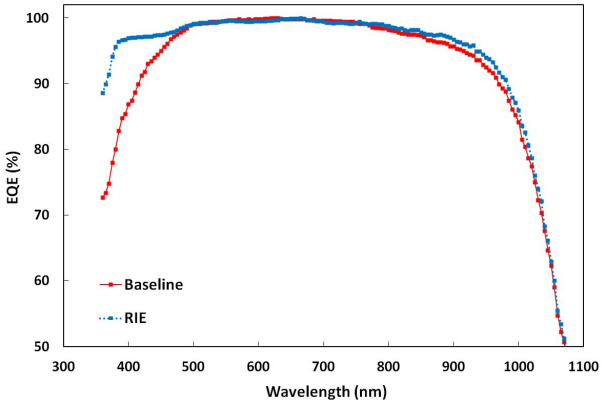

Fig. 5. External quantum efficiency of fabricated samples

surface recombination on larger surface area dominates and so the current gain becomes trivial. The implied V_{oc} indicates thick passivation could potentially help to reach efficiency higher than the one obtained with thinner passivation. However, the fast firing temperature needs to be increased to achieve punch-through of thick SiN_x layer. This would create thick Al-BSF layer and pose more challenges such as wafer bowing and non-uniform BSF quality with process integration[8]. The optimization strategy is to take advantage of high fill factor for thin passivation layer and deal with passivation quality on the RIE surface.

The electrical parameters of fabricated cells are listed in Table 1. The result shows average efficiency increases by 0.13%. for RIE cell passivated with SiO_2/SiN_x compared to our baseline cell. RIE processed cell benefits from not only increased current but also greater surface area which reduces contact resistance resulting higher fill factor. Although higher implied V_{oc} for RIE processed cells has been demonstrated with proper passivation, the actual V_{oc} after metallization is lower. This loss indicates that either the metal paste reaction or doping profile in the emitter region after fast firing process has influenced the result. The efficiency gain could be much higher if V_{oc} value is equal to the baseline cell. Similar parameter trade-off between V_{oc} and J_{sc} values is shown in a paper applying RIE to interdigitated back-contact (IBC) structure[9].

Also, it was observed that all RIE processed samples tend to have lower shunt resistance (Rsh) compared to our baseline. The incomplete step coverage by SiNx film on the uneven surface previously observed by SEM may be responsible for the low shunt values.

The best efficiency sample of each process is selected and their external quantum efficiency (EQE) is measured as shown in Fig. 5. Similar to the reflectance measurement, the short wave-

length region has improved significantly and increased response between 800 nm and 1000 nm wavelength also indicates excellent optical and electrical property of the fabricated solar cell despite lower V_{oc} value.

4. Conclusion

The industry feasible RIE process for monocrystalline silicon solar cell is demonstrated with absolute efficiency gain of 0.13%. The etch time was controlled to achieve maximum gain from light trapping and the corresponding SiN_x thickness was optimized with the PECVD process to account for the enlarged surface area. Various characterizations including SEM, reflectance, and implied V_{oc} measurement were conducted to confirm the impact of RIE on each process. The non-uniform deposition of SiN_x film is affected by enlarged nano-surface while the metallization contact is benefited from lower series resistance. The relatively lower V_{oc} values for RIE processed cells can be attributed to increased surface recombination by larger surface area and changed doping profile condition. The thicker SiN_x film works as supplementary to passivation quality, but thinner SiN_x film results high fill factor.

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