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Capacitance-Voltage (C-V) Characteristics of Cu/n-type InP Schottky Diodes

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Using capacitance-voltage (*C-V*) and conductance-voltage (*G/ω-V*) measurements, the electrical properties of Cu/n-InP Schottky diodes were investigated. The values of C and *G/ω* were found to decrease with increasing frequency. The presence of interface states might cause excess capacitance, leading to frequency dispersion. The negative capacitance was observed under a forward bias voltage, which may be due to contact injection, interface states or minority-carrier injection. The barrier heights from *C-V* measurements were found to depend on the frequency. In particular, the barrier height at 200 kHz was found to be 0.65 eV, which was similar to the flat band barrier height of 0.66 eV.

Keywords: InP, Capacitance, Interface states

1. INTRODUCTION

InP and related materials have attracted attention in the fabrication of optoelectronic, microwave, and high power and high speed electronic devices, due to their direct band gap, good temperature stability, high frequency response and high electron saturation velocity [1-3]. When realizing such devices, metal-semiconductor (MS) and metal-insulator-semiconductor (MIS) type Schottky contacts are frequently used, and it is thus necessary to understand the electrical properties of MS and MIS interfaces in detail. However, a complete description of charge carrier transport through MS and MIS contacts is yet to be obtained.

Capacitance-voltage (*C-V*) and conductance-voltage (*G/ω-V*) measurements can be used to evaluate the electrical properties of Schottky junctions. For example, *C-V* measurements will show an increase in capacitance with increasing forward bias voltage, which can be quite different at low and moderate frequencies in the depletion and accumulation regions, due to carriers in interface states, the presence of an interfacial insulator layer and the series resistance [4]. Interestingly, an anomalous peak and negative capacitance in the forward bias region have been observed for many electronic devices [5-10]. Demet *et al.* found that the negative capacitance of Au/n-GaAs Schottky contacts may be explained by polarization (especially at low frequencies) and the introduction of more carriers to the structure [5]. Temperature-dependent negative capacitance behavior of Al/rhodamine-101/n-GaAs Schottky diodes has been observed, and it has been explained by the loss of interface charges localized at the MS interface through the impact ionization process [8]. Zhu *et al.* showed that the negative capacitance behavior in light-emitting diodes (LEDs) was highly related to injected carrier recombination in the active region of luminescence [9]. Jones *et al.* attributed the negative capacitance to the relaxation-like nature of the material [10]. Although there have been a number of studies on the physical origin of negative capacitance, it has not yet been fully confirmed. In this work, the *C-V* and *G/ω-V* characteristics of Cu/n-InP Schottky contacts were explored and a detailed analysis is presented based on the results.

2. EXPERIMENTAL

Single-side polished undoped (unintentionally n-type doped) InP (100) wafer (thickness: 350 μm), with a carrier concentra-

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tion of ~1 × 10^{16} cm^{-3} was used as a starting material. The wafer was cut into small pieces and then cleaned. Then, 100 nm-thick Cu films were deposited onto the polished side as Schottky contacts using radio-frequency (RF) magnetron sputtering through a shadow mask with an exposed diameter of 500 μm. For ohmic contacts, 150 nm-thick Al metal was deposited over the entire back surface of the samples. Current-voltage (*I-V*) and capacitance-voltage (*C-V*) measurements were carried out at room temperature using a Keithley 238 current source and an HP 4284A LCR meter.

3. RESULTS AND DISCUSSION

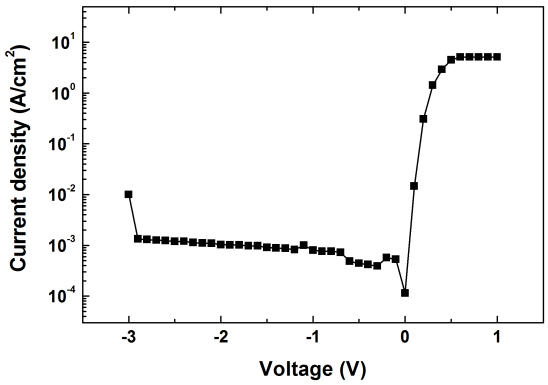

Fig. 1. Semilogarithmic current density-voltage (*J-V*) curve measured at room temperature.

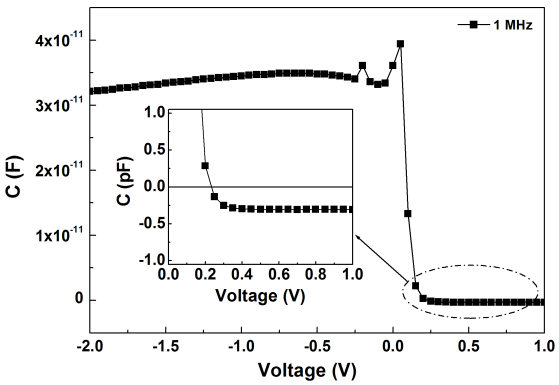

Fig. 2. Capacitance-voltage (*C-V*) characteristic measured at 1 MHz. The inset shows the magnified *C-V* characteristic under forward bias conditions.

Figure 1 shows a typical semilogarithmic *I-V* curve measured at room temperature. The diode showed a rectifying characteristic with a rectifying ratio of 1 × 10^4 at ± 0.5 V. The Schottky barrier height (SBH, Φ_B) and ideality factor (n) were determined from the forward bias *I-V* curve, based on the thermionic emission (TE) model [4]. The forward *I-V* analysis produced a barrier height of 0.54 eV and an ideality factor of 1.27. *C-V* measurements performed using the Keithley 4200 SCS instrument by other research groups yielded a similar negative capacitance, indicating that the origin of negative capacitance is more likely to be related to interface charges than measurement errors. If the work function of Cu (Φ_M = 4.65 eV [11]) and the electron affinity of InP (χ_S = 4.4 eV [12]) are considered, the Schottky-Mott relationship ($\Phi_B = \Phi_M - \chi_S$) yields a barrier height of about 0.25 eV, which is much lower

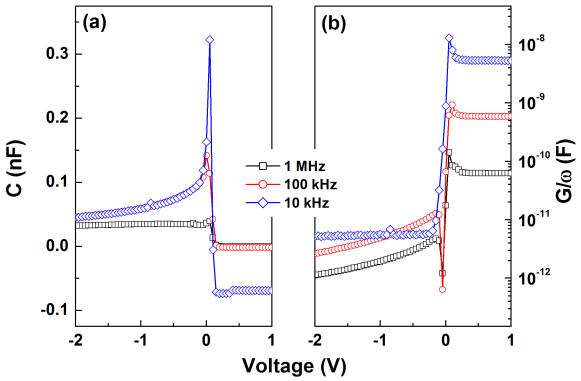

Fig. 3. (a) *C-V* and (b) conductance-voltage (*G/ω-V*) characteristics measured at different frequencies.

than the barrier height obtained from the *I-V* measurements. Fermi-level pinning at energies 0.4-0.5 eV below the conduction band edge of the n-type InP can lead to a barrier height as great as 0.5 eV [13]. A higher ideality factor than unity also implies the combined effect of the insulator layer and interface states [14].

When the thermionic field emission (TFE) or field emission (FE) model controls the current transport, the forward bias currents are described as $I \propto \exp(qV / E_0)$, where $E_0 = E_{00} \coth(E_{00} / kT)$ is a parameter dependent on barrier transparency and E_{00} is the characteristic energy related to the tunneling probability [15]. The value of E_{00} determines the dominant current transport mechanism, with TE observed for E_{00}/kT<<1, TFE for E_{00}/kT~1, and FE for E_{00}/kT>>1 [16]. Considering the kT value of 25.9 meV at room temperature, the value of E_{00} obtained from the *I-V* curve suggests tunneling effects, resulting from the presence of the insulator layer and/or interface states.

Figure 2 shows the *C-V* curve measured at 1 MHz. The capacitance increased slowly with decreasing reverse bias voltage, indicating that the width of the depletion layer varied with the applied bias voltage. The *C-V* curve also revealed an anomalous peak with increasing bias voltage, associated with the distribution of deep traps in the gap, the series resistance, and interface states [17,18]. The inset in Fig. 2 shows that negative capacitance was observed under a forward bias. *C-V* measurements were performed on several diodes to check whether the negative capacitance arises from variations between each diode; however, a similar negative capacitance behavior was observed in all samples. Frequency dependent *C-V* and *G/ω-V* characteristics of Cu/n-InP Schottky junctions were measured under various frequency ranges.

Figure 3 shows that the values of C and *G/ω* decreased with increasing frequency. At low frequencies, the interface states can follow the a.c. signal, which yields an excess capacitance and conductance that depends on the frequency. At high frequencies, the interface states cannot follow the a.c. signal, reducing the contribution of interface states to the total capacitance. This frequency dispersion can also be associated with the formation of an inhomogeneous layer at the MS interface. The capacitance of such layers connected in series with the oxide capacitance may cause frequency dispersion.

The values of negative capacitance shown in Fig. 3 were observed with increasing forward applied voltage for all frequencies. The physical mechanisms of the negative capacitance in different devices have been associated with the contact injection, interface states or minority-carrier injection [19,20]. Wu *et al.* stated that the negative capacitance can be explained by considering the loss of interface charge at occupied states below

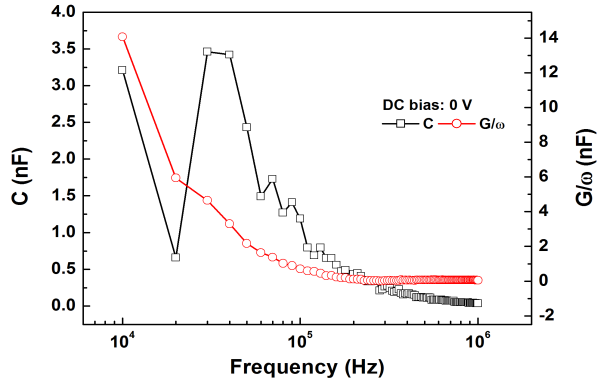

Fig. 4. Capacitance-frequency (*C-f*) and conductance-frequency (*G/ω-f*) characteristics measured at a d.c. bias voltage of 0 V.

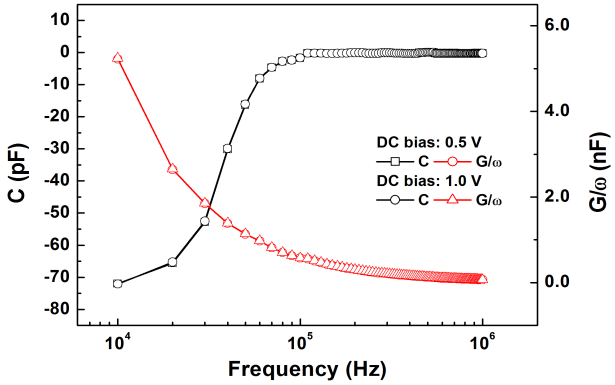

Fig. 5. *C-f* and *G/ω-f* characteristics measured at d.c. bias voltages of 0.5 and 1.0 V.

the Fermi level due to impact ionization. Instrumental problems such as parasitic inductance or poor measurement experiment calibration have also been considered to explain the negative capacitance [21]. The existence of interface states, the interfacial layer at the MS interface, and the series resistance of the device have been provided as other explanations for the negative capacitance [22]. Another explanation is that when the forward bias voltage reaches a maximum value, the effect of recombination exceeds that of diffusion and then the contact capacitance decreases rapidly, becoming negative [23]. The lower value of negative capacitance in Fig. 3(a), at lower frequencies in the forward bias region, can be attributed to an inductive contribution to the impedance resulting from the high-level injection of minority carriers into the bulk semiconductor [24].

As shown in Fig. 3, the change in the C and *G/ω* values became more significant in the forward bias region than in the reverse bias region. Hence, values of C and *G/ω* with different bias voltages were investigated in more detail. The capacitance-frequency (*C-f*) and conductance-frequency (*G/ω-f*) characteristics for different applied d.c. bias voltages of 0, 0.5 and 1.0 V are shown in Figs. 4 and 5. The values of C and *G/ω* were higher at 0 V compared to other bias voltages and these values were almost the same at 0.5 and 1.0 V. It can also be seen that the decrease in C corresponds to an increase in *G/ω*. The increase in the *G/ω* value at a low frequency can be explained by the increase in the number of charge carriers available for a given relaxation time of the interface states [5]. In Au/n-Si Schottky diodes, Bati *et al.* observed an excess capacitance arising from the diffusion of minority carriers and they explained that the presence of an interfacial

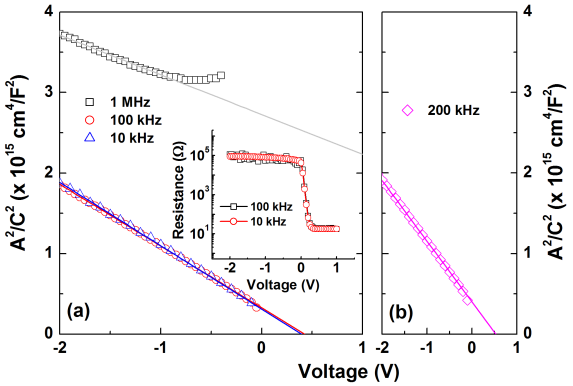

Fig. 6. A^2/C^2 vs. V plots measured at (a) 1 MHz, 100 kHz, and 10 kHz and (b) 200 kHz. The inset in Fig. 6 (a) shows the resistance values measured at frequencies of 100 and 10 kHz.

layer at the MS interface increased the capacitance with decreasing frequency due to the interface states [25]. Therefore, such C and *G/ω* behaviors with applied bias voltage and frequency can result from the influence of interface states.

The *C-V* characteristics under reverse bias were used to obtain the barrier heights of the Schottky diodes. The relationship between the capacitance and the applied voltage in Schottky diodes is given by [4]

$$A^2 / C^2 = 2\left(\frac{V_{bi} - kT/q - V}{qN_D\varepsilon_S\varepsilon_0}\right) \quad (1)$$

where V_{bi} is the built-in potential, χ_S is the dielectric constant of the semiconductor, ε_0 is the permittivity in vacuum, and N_D is the donor concentration. The carrier concentration can be extracted from the slope of a plot of A^2/C^2 vs. V, as shown in Fig. 6. The SBH can be obtained from $\phi_B^{(C-V)} = V_0 + \xi + kT/q$, where V_0 is the intercept on the voltage axis according to Eq. (1), and $\xi[\xi = (kT/q)\ln(N_C/N_D)]$ is the energy difference between the conduction band and the Fermi level. Here, N_C is the effective density of states in the conduction band (N_C = 5.7 × 10^{17} cm^{-3} in InP).

Figure 6 shows that the barrier height at 1 MHz can be more than 5 eV, which is unacceptably high. When a thin oxide layer is present, an increase in the barrier height in *C-V* measurements can be expected [26]. It is likely that the measurement error due to the series resistance at 1 MHz is significant. To reduce such an error, the barrier heights were obtained at lower frequencies, of 100 and 10 kHz. The obtained carrier concentration was found to be about 1.45 × 10^{16} cm^{-3}, which is similar to the value provided by the manufacturer. The barrier heights were then calculated to be 0.55 and 0.52 eV at 100 and 10 kHz, respectively. The inset in Fig. 6 shows the measured resistance values according to the bias voltage at 100 and 10 kHz. The resistances approached almost constant values above 0.4 V, corresponding to the series resistance. The average value of series resistance was about 18 Ω, similar to the value of 17.5 Ω obtained from the *I-V* measurement shown in Fig. 1.

The fundamental or flat band barrier height was also calculated using the ideality factor (n) and the effective barrier height (Φ_B), given by the TE model [27]:

$$\phi_{Bf} = n\phi_B - (n-1)kT/q\ln(N_C/N_D) \quad (2)$$

The electric field in the semiconductor was zero under the flat band condition and the effects of tunneling and image force lowering on the *I-V* characteristics were negligible. Using Eq. (2), the flat band barrier height was found to be 0.66 eV, which was higher than the barrier heights obtained from both the *I-V* and *C-V* measurements. To explain this discrepancy, the *C-V* data measured at 200 kHz was also analyzed, as shown in Fig. 6(b). The barrier height at 200 kHz was found to be 0.65 eV, which was similar to the flat band barrier height. The *C-V* data at 500 kHz was also analyzed and the barrier height was found to be 1.05 eV, which was higher than the flat band barrier height. At low frequencies (below 100 kHz), the interface states that followed the a.c. signal caused an excess capacitance, leading to a lower barrier height. At high frequencies (> 500 kHz), the interface states cannot follow the a.c. signal, but the presence of a native oxide layer and the effect of series resistance probably produced a barrier height greater than the flat band barrier height. In other words, the contribution of excess capacitance to total capacitance at higher frequencies was insignificant. Instead of *I-V* characteristics, this work focused more on analyzing the *C-V* characteristics using various measurement conditions. The results can be useful in diagnosing the properties of Schottky diodes. For example, the barrier height obtained from different frequencies is related to the presence of interface traps and/or the insulator layer. Then, the improvement of device performance can be achieved by reducing the density of interface traps.

4. CONCLUSIONS

The electrical properties of Cu/n-InP Schottky junctions were investigated using *C-V* and *G/ω-V* measurements. It was found that the values of C and *G/ω* decreased with increasing frequency. Such a frequency dispersion in the values of C and *G/ω* might be associated with the presence of interface states. Negative capacitance was observed under forward bias conditions. The origin of the negative capacitance may be related to contact injection, interface states or minority-carrier injection. The barrier heights from *C-V* measurements were found to depend on the measurement frequency. The flat band barrier height was found to be 0.66 eV, which was similar to the barrier height of 0.65 eV at 200 kHz.

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