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An L-band Stacked SOI CMOS Amplifier

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Abstract

This paper presents a two stage L-band power amplifier realized with a 0.32 µm Silicon-On-Insulator (SOI) CMOS technology. To overcome a low breakdown voltage limit of MOSFET, stacked-FET structures are employed, where three transistors in the first stage amplifier and four transistors in the second stage amplifier are connected in series so that their output voltage swings are added in phase. The stacked-FET structures enable the proposed amplifier to achieve a 21.5 dB small-signal gain and 15.7 dBm output 1-dB compression power at 1.9 GHz with a 122 mA DC current from a 4 V supply. The amplifier delivers a 19.7 dBm. This paper presents a two stage L-band power amplifier realized with a 0.32 µm Silicon-On-Insulator (SOI) CMOS technology. To overcome a low breakdown voltage limit of MOSFET, stacked-FET structures are employed, where three transistors in the first stage amplifier and four transistors in the second stage amplifier are connected in series so that their output voltage swings are added in phase. The stacked-FET structures enable the proposed amplifier to achieve a 21.5 dB small-signal gain and 15.7 dBm output 1-dB compression power at 1.9 GHz with a 122 mA DC current from a 4 V supply. The amplifier delivers a 19.7 dBm saturated output power with a 16 % maximum Power Added Efficiency (PAE). A bond wire fine tuning technology enables the amplifier a 23.67 dBm saturated output power with a 20.4 % maximum PAE. The die area is 1.9 mm x 0.6 mm.

Key words :SOI CMOS, L-band amplifier, stack FET amplifier, CMOS-MMIC, Silicon-On-Insulator (SOI), stacked transistors, CMOS amplifier

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I. Introduction

CMOS technology has become an attractive choice for single-chip radio transceivers by virtue of its low cost and high-integration possibility. CMOS RF amplifiers offer the potential of reducing complexity and cost by combining the integration of a transceiver and digital baseband circuitry on the same chip. However, most of researcher has been hesitated to launch a CMOS RF integrated circuit due to the low resistive silicon substrate and low breakdown voltage [1], [2].

The SOI CMOS research program by the IBM

Research Division in early 1989, triggered the quasi CMOS SOI technology based PowerPC in 1994. Motivated by leading activity in IBM group, the low resistive silicon substrate is not the final limit of silicon RF integrated circuit any more now when a mature SOI technology has been developed [3].

Several circuit topologies have been proposed to overcome the limit of low breakdown voltage in CMOS transistors, such as transformer [4], cascode [5], and stacked structures [6].

The transformer occupies a lot of die area and low resistive silicon substrate degrades the high frequency performance. In addition, the transformer is not available in commercially available standard silicon foundry process so a very accurate passive component modeling and conformation for the integrated RF circuit entails a large burden for the circuit designer. Employing the cascode structure can double the limit of low drain breakdown voltage in FET by sharing the voltage drop between the two transistors and extend the pole frequency, which is associated with Miller effect, of a single device. Stacking more than two FETs has a potential to extend the limit of the low drain breakdown voltage of device much higher than twice if the substrate's resistance is high enough to accommodate the high voltage swing at drain.

Stacking of SOl transistors in series has been reported to overcome the low voltage breakdown limit of device by combining voltage swing of each device and facilitate high output impedance [7].

The top transistor in the stack can easily reach gate oxide breakdown because maximum swing of drain voltage can reach twice of the DC supply voltage while its gate voltage is fixed. The capacitive parasitics from transistor layouts and interconnections on the low resistive silicon substrate invokes large variations in drain-source voltages of transistors in the stack. The voltage variations lead at the top transistors of the stack to have higher voltage swings than other transistors and cause premature voltage breakdown which degrades the amplifying performance. For these reasons, the number of stacked transistors is limited [7].

Stacking of four electrically isolated 0.28 μm SOl CMOS FETs in series has been applied for L-band amplifier circuit with a 9 V DC voltage supply [6]. An 1.8 GHz power amplifier with a 12 V supply has been reported using stacked 16 dynamically biased thin oxide transistors in a 45 nm CMOS SOl process [7]. Stacking of three 0.45 nm SOl transistors has been used for W-band amplifier with a 4.2 V supply [8].

In this paper, a two stage SOI CMOS power amplifier circuit with stacked three transistors in the first stage amplifier circuit and stacked four transistors in the second stage for L-band application is presented.

Ⅱ. Circuit Design

The 1st amplifier with the stacked-FET structure presented in this study is shown in Fig. 1. The circuit inside the dotted rectangle presents integrated circuit.

The circuit is composed of three stacked transistors connected in series so that their output swings are added in phase. The amplifier with less than three stacked FETs showed potentially higher gain, however it suffered from stability issues in the circuit design simulation. All three FETs must have equal voltage headroom to prevent a premature breakdown at the top device and an early compression at the bottom device.

The bond wire on drain pad is used as a choke inductor whose length is tuned accurately to provide optimum impedance yielding maximum small signal gain. All pads for bonding are protected with ESD diodes.

Two MIM capacitors are connected in series for each symbol of the capacitor to prevent an

early voltage breakdown between two metals in the capacitor when high voltage swings are applied.

In the second stage amplifier, four transistors are stacked in series to accommodate amplified voltage swing from the first stage amplifier output as shown in Fig. 2.

The inter-stage matching circuit between the 1st and the 2nd stage amplifier is implemented with a parallel inductor L2p, parallel connected series capacitors C21, C22, C23, C24, and a series capacitor C1c.

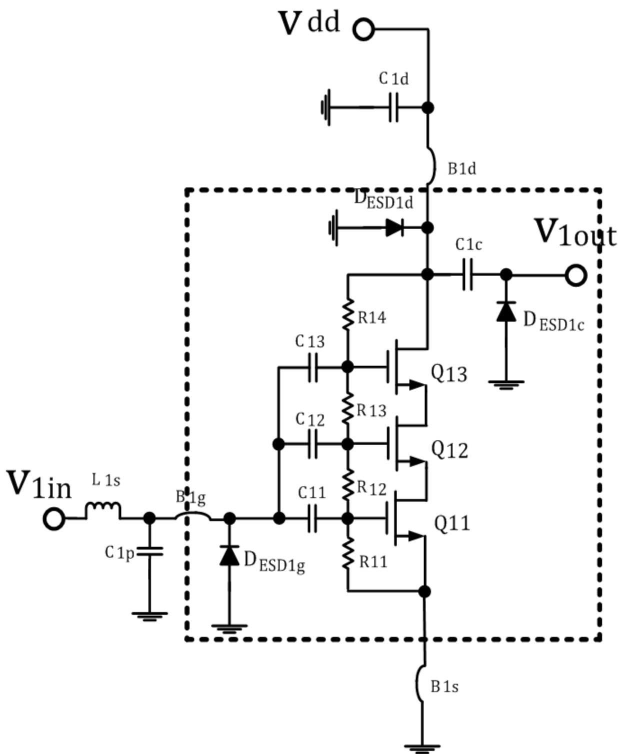

Fig. 1. Schematic diagram of the proposed 1st stage amplifier circuit with three stacked transistors

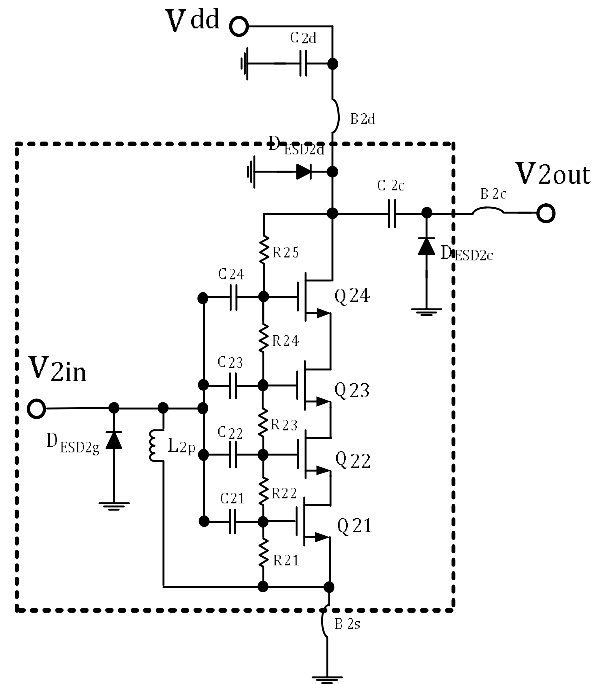

Fig. 2. Schematic diagram of the proposed 2nd stage amplifier circuit

III Experimental Results

The designed circuit was implemented using 0.32-μm SOI CMOS technology from IBM. A micrograph of the fabricated die is shown in Fig. 3. The chip size is 1.9 mm x 0.6 mm. A bond with a very short wire is used for the interconnection between two amplifiers because the output pad of the first stage amplifier is very close to the input pad of the second amplifier.

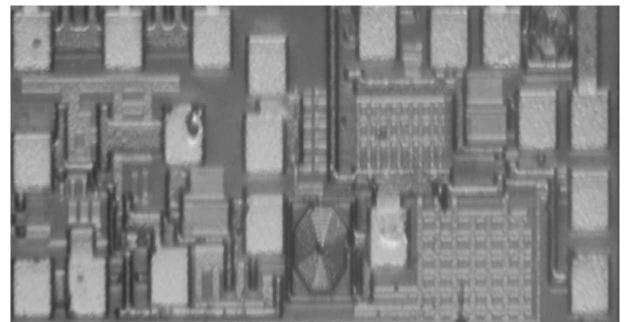

Fig. 3. A micrograph of the fabricated SOI amplifier

The die is wire bonded to a printed circuit board with off-chip lumped passive element matching circuit which is consisted of a series inductor L1s and a parallel capacitor C1p at the input port. No matching refinement was performed at the output port.

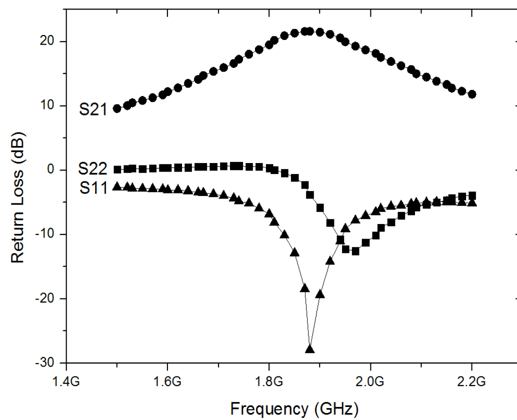

Fig. 4. Measured small signal S-parameters of the fabricated SOI amplifier

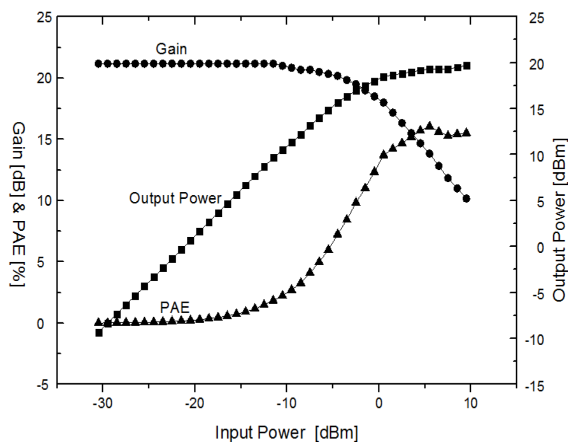

Fig. 5. Measured gain, PAE, and output power as a function of input power with a continuous wave input from a 4 V supply

Fig. 4 shows the measured small signal parameters of the amplifier. The amplifier shows a 21.5 dB gain, a -28 dB input return loss, and a -5.8 dB output return loss at 1.9 GHz. It consumes dc current of 122 mA including bias circuit from a 4 V supply. The output 1 dB compression power of the amplifier is a 15.7 dBm with a 7.3 % PAE at this power level as shown in Fig. 5. The amplifier provides a saturated output power of a 19.7 dBm. It shows a 16 % of maximum PAE.

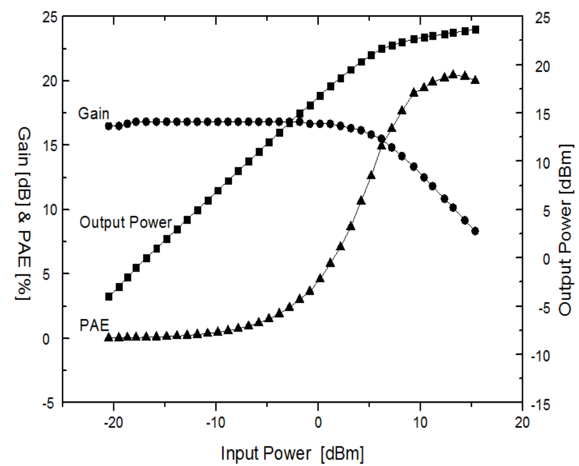

Fig. 6. Measured gain, PAE, and output power as a function of input power with a continuous wave input from a 5.2 V supply

The bond wires is fine tuned for a power amplifier application with a higher supply voltage. With a 5.2 V supply, the output 1 dB compression power of the amplifier is enhanced to a 21.5 dBm with a 14.8 % PAE at this power level as shown in Fig. 6. The amplifier provides a saturated output power of a 23.67 dBm with a 20.4 % of maximum PAE. However, the increased supply voltage suppresses the small signal power gain down to 16.8 dB.

Table 1 shows a summary of the measured results compared to other integrated L-band SOI and CMOS power amplifiers that have been reported. It is noticeable that the supply voltages for the power amplifiers with CMOS technology are less than 3.4 V [9], [10], [11]. The supply voltages are higher than 5.2 V for the circuits with SOI in reference [7], [6], and this work which is result of multi-stacked structures of SOI based circuits.

Table 1. Integrated SOI and CMOS power amplifiers

Ref.	Freq. (GHz)	Gain (dB)	Pout @1dB (dBm)	Saturated Power (dBm)	PAE (%)	Supply Voltage (V)	Technology	Topology
[7]	1.8	10.2	21	26.5	19	12	SOI 45 nm	single–stage 16 stack
[9]	1.8	25	25.4	29.4	37.9	3.4	CMOS 65 nm	two-stage stacked–cascode
[6]	1.9	14.6	30.8	29.4	41.4	6.5	SOI 130 nm	single–stage 4 stack
[10]	1.75	24.3	20.2	24	29	3.3	COMS 0.5 μm	two-stage common source
[11]	1.95	26	25.4	26	46.4	3.4	COMS 0.18 μm	two-stage cascode
This work	1.9	21.5	14	19.7	16	4	SOI 0.32 μm	two-stage 3 stack+4 stack
This work	1.9	16.8	21.5	23.67	20.4	5.2	SOI 0.32 μm	two-stage 3 stack+4 stack

IV. Conclusion

The design of a high gain amplifier at L-band realized with a two-stage amplifier based on a standard 0.32-μm SOI CMOS technology is presented in this paper. The circuit structure is based on multi-stacked transistors to overcome the low breakdown voltage of the CMOS device as is presented in this work.

A two stage power amplifier with three stacked FETs in the first stage amplifier and four stacked FETs in the second amplifier is proposed for a high gain L-band application. The proposed structure has been provided a solution to overcome limit of the low breakdown voltage between drain and source of MOSFET device.

Based on the presented stacked-transistors topology, an amplifier is implemented and achieved a measured gain of 21.5 dB and a maximum PAE of 16 % with a saturated output power of a 19.7 dBm at 1.9 GHz with a 4 V supply. A 23.67 dBm saturated output power and a 20.4 % maximum PAE with a 5.2 V supply are achieved by the bond wire fine tuning technology.

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