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Accurate Sub-1 V CMOS Bandgap Voltage Reference with PSRR of -118 dB

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***Abstract*—A low voltage high PSRR CMOS Bandgap circuit capable of generating a stable voltage of less than 1 V (0.8 V and 0.5 V) robust to Process, Voltage and Temperature (PVT) variations is proposed. The high PSRR of the circuit is guaranteed by a low-voltage current mode regulator at the central aspect of the bandgap circuitry, which isolates the bandgap voltage from power supply variations and noise. The isolating current mirrors create an internal regulated voltage V_{reg} for the BG core and Op-Amp rather than the V_{DD}. These current mirrors reduce the impact of supply voltage variations. The proposed circuit is implemented in a 0.35 µm CMOS technology. The BGR circuit occupies 0.024 mm^2 of the die area and consumes 200 µW from a 5 V supply voltage at room temperature. Experimental results demonstrate that the PSRR of the voltage reference achieved -118 dB at frequencies up to 1 kHz and -55 dB at 1 MHz without additional circuits for the curvature compensation. A temperature coefficient of 60 ppm/°C is obtained in the range of -40 to 120°C.**

***Index Terms*—Bandgap reference (BGR), high PSRR, low voltage, line regulation, current-mode regulator**

I. INTRODUCTION

Most systems require a voltage reference independent of the variation of power supply, process, or temperature, and a bandgap voltage reference (BGR) often serves this purpose [1]. The design of robust low-voltage and high power supply rejection ratio (PSRR) reference voltage has become more important especially in system on chip design. Bandgap (BG) reference voltage generators are known to be the most popular solution for the generation of such a precise reference voltage in CMOS integrated circuits [1-5].

In this paper, the general configuration of the reference generator circuit and the utilized bias is similar to that of the voltage reference circuit proposed in [1]. In order to reduce the supply source noise at the reference voltage, a current mode regulator is used to isolate the area between the supply source and the bandgap reference circuit.

In fact, a constant voltage is created that is almost independent from the supply source V_{REG}, as shown in Fig. 1, and is used to supply the bandgap reference circuit. However, because the operational amplifier (Op-Amp) is supplied with a voltage of V_{DD}, and due to the inadequacy of Op-Amp PSRR, the supply source ripple is initially transmitted to Op-Amp, and then again to V_{REG}.

This results in incomplete independence of the

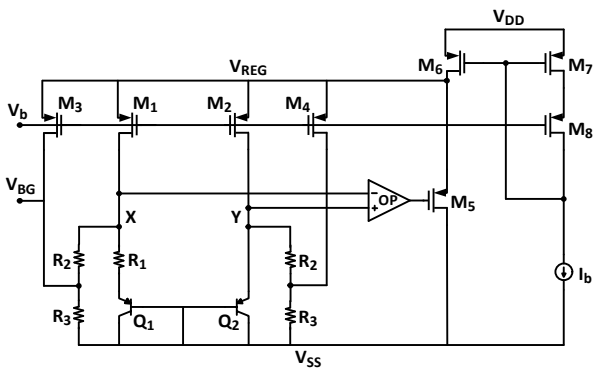

Fig. 1. Configuration of voltage reference, introduced at [1].

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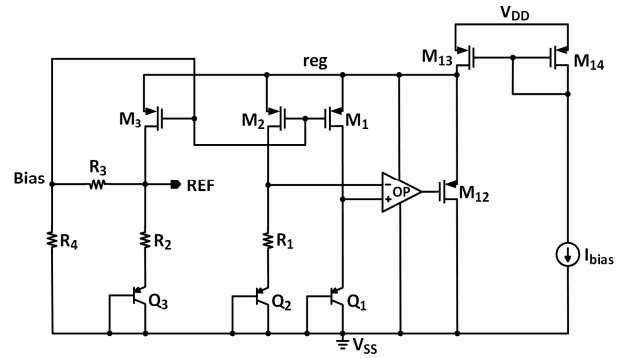

Fig. 2. Proposed voltage circuit configuration.

reference voltage generator circuit from the supply voltage variations. However, in this paper, in order to provide complete independence of the BGR circuit from the V_{DD} variations, we used an internal regulated voltage V_{reg} for the BG core and Op-Amp was used instead of V_{DD}. In this article, accurate sub-1V BGR circuit is presented to achieve high PSRR, fast settling with low power dissipation for a low-dropout (LDO) regulator and current reference generator in an RF Transceiver system. Improvement in PSRR is due to a low voltage current mode circuit which works with the specified voltage headroom.

This paper is organized as follows. In Section II the proposed circuit design in 0.35 μm CMOS is presented. Section III reports the performance results, followed by the conclusion in Section IV.

II. PROPOSED VOLTAGE REFERENCE

Fig. 2 depicts the general configuration of proposed voltage reference circuit. This voltage reference must be able to completely remove the supply voltage noise at lower frequencies and maintain this ability at higher frequencies.

In this structure, the adjusted V_{reg} voltage, in addition to supplying a BG reference circuit, also addresses the supply of the supplying error amplifier, which contributes to complete independence of the circuit from the supply source.

In addition, modifications have been made to the BG reference circuit configuration which, in comparison to the previous configuration, results in ease of determining the reference voltage value, and achieving zero temperature coefficient at a desirable voltage.

Performing *KVL* at the Op-Amp inlet circuit will result in:

$$I_{d2} = \frac{V_{EBQ1} - V_{EBQ2}}{R_1} = \frac{V_T \ln(N)}{R_1} \tag{1}$$

Considering $I_{d2} = I_{d3}$, we will also have:

$$V_{ref} = [R_2 \,||\, (R_3 + R_4)]I_{d3} + (\frac{R_3 + R_4}{R_3 + R_4 + R_2})V_{EBQ3} \tag{2}$$

Additionally, at the Bias node we will have:

$$V_{Bias} = (\frac{R_4}{R_3 + R_4})V_{ref} = \alpha V_{ref} \tag{3}$$

which demonstrates that variation of this voltage is similar to that of the reference voltage. Fig. 3 illustrates the deployment of the proposed structure. In this configuration, in order to guarantee activity of M_8 and M_{11} transistors, the V_{Bias} value is adjusted very closely to

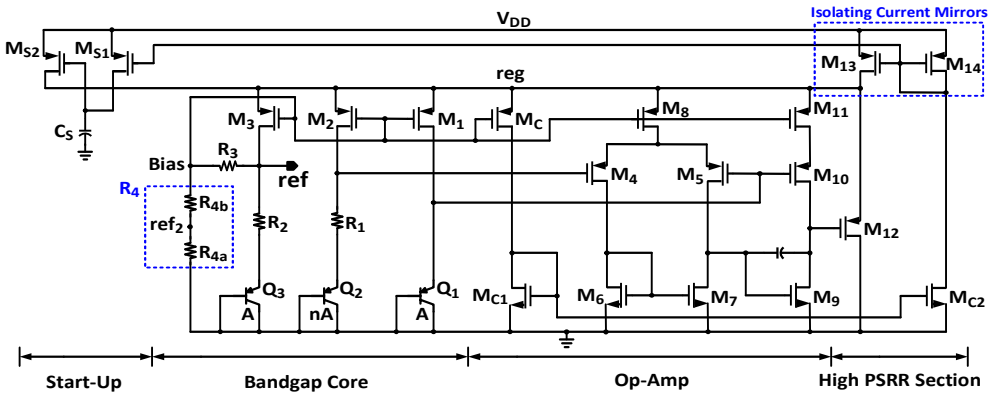

Fig. 3. Complete schematic of the proposed low-voltage bandgap reference circuit.

V_{ref} ($\alpha \approx 1$).

To deploy the Op-Amp, a two-stage amplifier is used which, in addition to supplying sufficient loop gain, has an acceptable phase margin and bandwidth. In this design, V_{ref} = 800 mV, and if a reference voltage of less than 0.8 V is required, we can split up the R_4 resistance into two smaller resistances and, without imposing any other modifications, we can create this voltage.

For example, V_{ref2} =500 mV with maximum variation of 5 mV in this design. The M_{s1} and M_{s2} transistors and the C_S capacitor work together as the start-up circuit. Initially, the M_{s1} transistor is on and the *reg* node voltage (V_{reg}) is placed at an acceptable range; the adequate current is then generated at the M_1, M_2 transistors, is then transmitted to the M_{14}, and M_{s2}. The C_S capacitor is recharged, and the M_{s1} transistor will then turn off.

The Op-Amp achieves the fast settling time of the reference voltage with a positive current feedback. These two circuits, start-up and Op-Amp, provide a fast settling time for the BGR.

III. Post-Layout Simulation and Experimental Results

The Bandgap reference voltage has been fabricated as part of 4 mm×4 mm chip in the 0.35 µm 5 V CMOS process. The microphotograph of the device is shown in Fig. 4. It occupies an area of 0.024 mm^2.

Fig. 5 depicts the simulated result of the proposed voltage reference circuit thermal behavior. As seen in the figure, the maximum deviation from reference voltage is around 8 mV, at the temperature range of -40 to 120°C. Fig. 6 shows the reference voltage and V_{reg} variations, in response to supply voltage variation from 0 to 5 V.

As can be seen, starting from a voltage of almost 2.3 V, the reference voltage values together are an acceptable amount. The thermal variation of the V_{ref2} voltage is shown at Fig. 7, which is based on the maximum variation of V_{ref2} being around 5 mV. In order to examine feedback loop stability, AC analysis is conducted, which is assisted by opening the feedback loop at the voltage reference circuit.

Results from this analysis are shown in Fig. 8, showing that PM=62° (Phase Margin), UGB=12.5 MHz (Unity Gain Bandwidth), and ALG=88 dB (Loop Gain Magnitude). Also, Fig. 9 shows the Monte Carlo

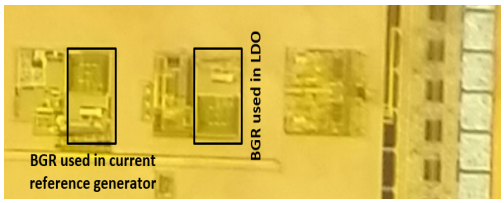

Fig. 4. Chip microphotograph.

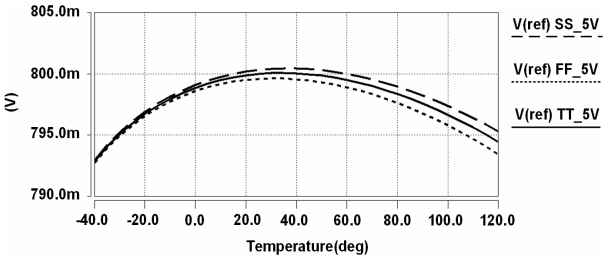

Fig. 5. Bandgap reference simulations given different process corners, in response to temperature variation.

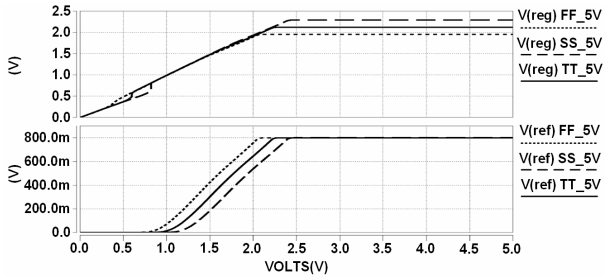

Fig. 6. Reference voltage, and V_{reg} variations, in response to supply voltage variation at corner cases (Line regulation).

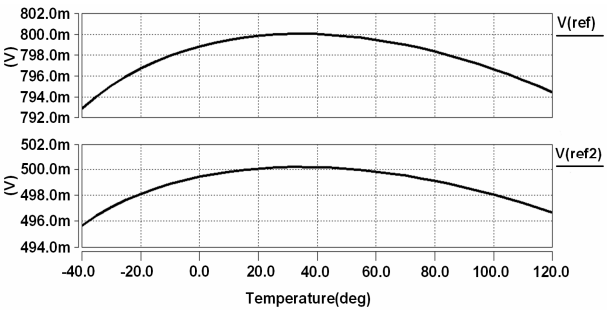

Fig. 7. Proposed voltage reference circuit thermal behavior at ref, and ref_2 node.

simulations of this operational amplifier. In order to address PSRR at the proposed voltage reference, AC analysis is conducted as shown in Fig. 10.

The figure shows that, for V_{ref} at frequencies up to 1 kHz, the PSRR magnitude is equal to -120 dB from the simulation result. Also, AC analysis for different circuit nodes is conducted as shown in Fig. 11, which shows that for V_{reg} at frequencies up to 1 kHz, the PSRR

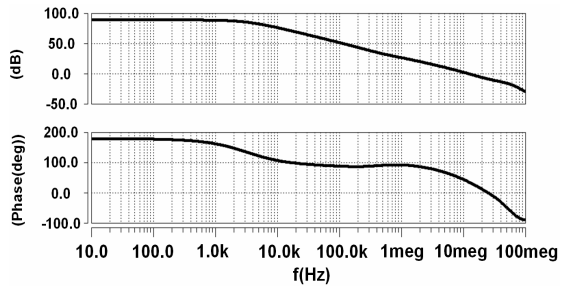

Fig. 8. Feedback loop AC analysis at voltage reference circuit.

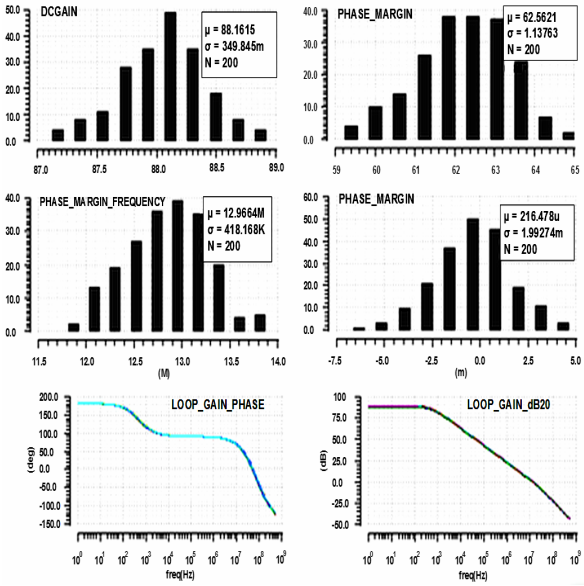

Fig. 9. Monte Carlo Analysis of Op-Amp.

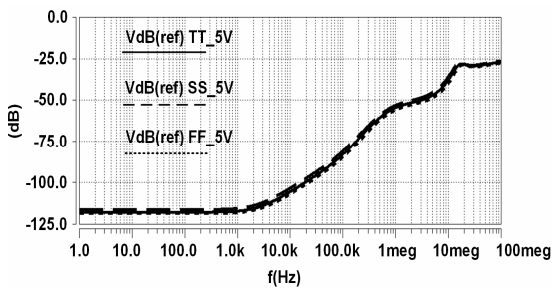

Fig. 10. PSRR of the proposed BGR at different process corners.

magnitude is equal to -118 dB, and for V_{ref2} is -123 dB.

In order to analyze the startup circuit, imposing the step input on the supply voltage, the transient response is simulated, as shown in Fig. 12, demonstrating that the reference voltage would attain its final value in less than 4 μs.

The distribution of the BGR output voltage V_{REF}, as obtained from Monte Carlo simulation of 200 runs, is shown at Fig. 13. The average of V_{REF} was 803.35 mV,

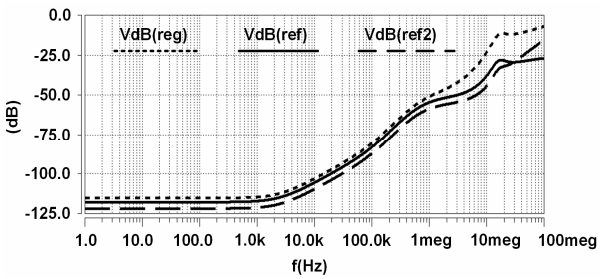

Fig. 11. Proposed voltage reference PSRR diagram at different circuit nodes.

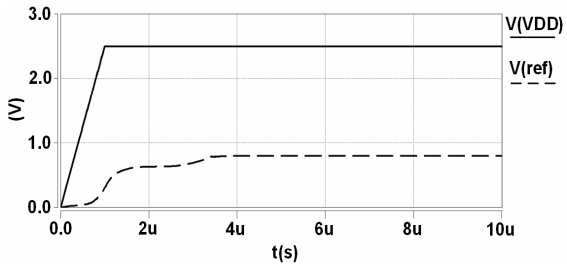

Fig. 12. V_{BG} during start-up.

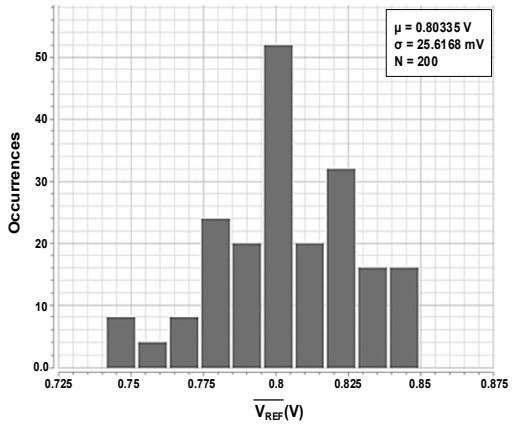

Fig. 13. Distribution of output voltage (V_{ref}), as obtained from Monte Carlo simulation of 200 runs.

and the standard deviation was 25.61 mV. The coefficient of variation σ/μ was 3.2%.

The measured reference voltage V_{ref} as a function of temperature, with various V_{DDs} is presented in Fig. 14. The average output voltage was 798.6 mV, with a temperature variation of 8.25 mV in a temperature range from -40 to 120°C. Fig. 15 illustrates the output voltage V_{ref} at room temperature as a function of V_{DD}. The circuit operated correctly when the power supply was greater than 2.35 V.

The measured line regulation was 7.2 μV/V when the supply voltage was swept from 2.35 V to 5 V. The measured power supply rejection ratio (PSRR) at room

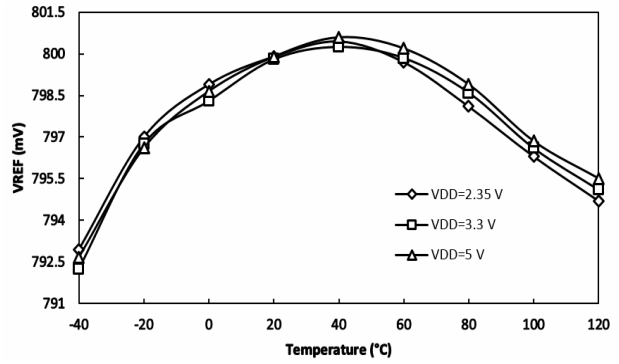

Fig. 14. Measured output voltage V_{ref} as a function of temperature, with various supply voltages.

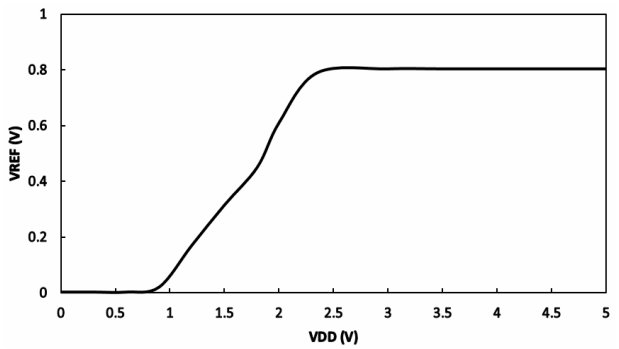

Fig. 15. Measured output voltage V_{ref} at room temperature as a function of power supply.

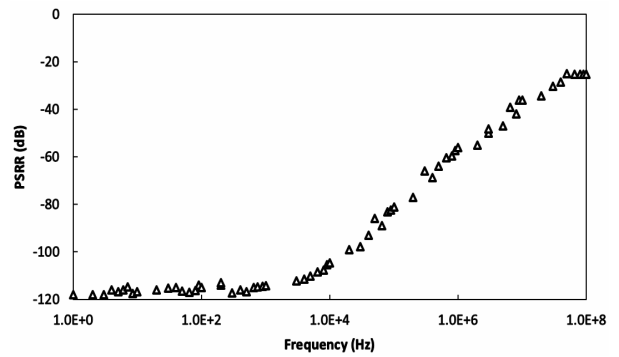

Fig. 16. Measured PSRR at room temperature with a 3.3 V supply voltage.

temperature with 3.3 V supply voltage is presented in Fig. 16. It can be seen that the PSRR is close to -118 dB at frequencies below 1 KHz, and remains greater than -55 dB up to 1 MHz. Thus, we were able to achieve the reference voltage circuit that was almost independent of temperature and V_{DD}.

In order to draw a comparison between the proposed configuration and other voltage references, the results are summarized in Table 1.

Table 1. Measurement and simulation results summary and comparison.

	[1]	[4]	[5]	**This work**
Technology (CMOS)	0.18 µm	65 nm	0.35 µm	**0.35 µm**
V_{DD} (min)	1.2 V	1.6 V	1.4 V	**2.3 V/2.35 V[(1)]**
V_{ref} (mV)	698	950	745	**800/798.6[(1)]**
I_{supply} (µA)	112	-	0.215	**40[(1)]**
TC (ppm/°C)	20	2.87	7	**54/60[(1)]**
Temperature (°C)	-40 to 140	-40 to 125	-20 to 80	**-40 to 120**
Line regulation	-	-	20 ppm/V	**6.6(µV/V) @ worst case/ 7.2(µV/V)[(1)]**
PSRR@ DC (dB)	-95	-72	-45	**-120/-118[(1)]**
PSRR@ 1 MHz (dB)	-60	-	-	**-58/-56[(1)]**
PSRR@ 10 MHz (dB)	-	-	-	**-38/-36.2[(1)]**
Area (mm^2)	0.027	0.02	0.055	**0.024**

[(1)] Measured results

IV. CONCLUSIONS

In this paper, a high PSRR low-voltage circuit used to generate a 798.6 mV BG reference voltage with a maximum variation of 8.25 mV was presented. The high PSRR of the circuit is achieved by using the current mode regulator and adjusted voltage V_{reg}, which isolates the Op-Amp and the bandgap voltage from power supply variations and noise. This, in comparison with similar previous works improves the reference voltage PSRR significantly, especially at lower frequencies. In addition, the line regulation of the proposed circuit is 7.2 µV/V at the worst case. The transient response of the BGR is less than 4 µsec, and its PSRR is -118 dB at DC frequencies. The current consumption of the BGR was set to 40 µA from a 5 V V_{DD} at room temperature, and the current consumption can be reduced with a larger R_2. The topology of the circuit allows it to be portable to several different CMOS processes with minimal redesign effort.

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