JOURNAL OF SEMICONDUCTOR TECHNOLOGY AND SCIENCE, VOL.16, NO.4, AUGUST, 2016
http://dx.doi.org/10.5573/JSTS.2016.16.4.497
ISSN(Print) 1598-1657
ISSN(Online) 2233-4866

Area and Power Efficient VLSI Architecture for Two Dimensional 16-point Modified Gate Diffusion Input Discrete Cosine Transform

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Abstract—**The two-dimensional (2D) Discrete Cosine Transform (DCT) is used widely in image and video processing systems. The perception of human visualization permits us to design approximate rather than exact DCT. In this paper, we propose a digital implementation of 16-point approximate 2D DCT architecture based on one-dimensional (1D) DCT and Modified Gate Diffusion Input (MGDI) technique. The 8-point 1D Approximate DCT architecture requires only 12 additions for realization in digital VLSI. Additions can be performed using the proposed 8 transistor (8T) MGDI Full Adder which reduces 2 transistors than the existing 10 transistor (10T) MGDI Full Adder. The Approximate MGDI 2D DCT using 8T MGDI Full adders is simulated in Tanner SPICE for 0.18µm CMOS process technology at 100MHZ.The simulation result shows that 13.9% of area and 15.08 % of power is reduced in the 8-point approximate 2D DCT, 10.63 % of area and 15.48% of power is reduced in case of 16-point approximate 2D DCT using 8 Transistor MGDI Full Adder than 10 Transistor MGDI Full Adder. The proposed architecture enhances results in terms of hardware complexity, regularity and modularity with a little compromise in accuracy.**

Index Terms—**Two-dimension, discrete cosine transform, one-dimension, modified gate diffusion input**

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I. INTRODUCTION

Signal processing is mostly used to retrieve information from signals or to convert information carrying signals from time domain to frequency domain. In signal processing, image and video signal processing is the most craved area in real world, it is more convenient and easy to work in frequency domain. Karhunen-Loève Transform (KLT) is the optimum transform but the complexity grows with input. It doesn't have a systematic procedure. Discrete Cosine Transform (DCT) is a very close substitute for the KLT, used to convert a signal from spatial domain to frequency domain. DCT is an essential mathematical tool in signal processing due to its high energy compaction property. The one-dimensional DCT is useful in processing one-dimensional signals such as speech waveforms. Several imaging standards such as JPEG, MPEG-1, MPEG-2, H.261, H.263 and H.264/AVC adopts the two dimensional (2D) version of the 8-point DCT.

Image and video compression frequently uses DCT. Computation intensive DCT with fast algorithms results in efficient calculation [1]. The 2D DCT can be computed by applying 1D transforms. The 1D DCT is applied to each row of input matrix and then to each column of the result. Thus, the transform of input matrix is given by

$$S(u,v)=\frac{2}{\sqrt{nm}}C(u)C(v)\sum_{y=0}^{m-1}\sum_{x=0}^{n-1}s(x,y)\cos\frac{(2x+1)u\pi}{2n}\cos\frac{(2y+1)u\pi}{2m}\quad u=0,..,n;v=0,...,m$$

where

$$c(u) = \frac{1}{\sqrt{2}} \quad \text{for} \quad u=0$$
$$=1 \quad \text{otherwise} \qquad (1)$$

The main aim of the approximation algorithm for DCT is to reduce complexity by eliminating strong and power consuming operations like multiplications and also to obtain meaningful estimation of DCT. The approximation is more suitable for higher-size DCT considering the computational complexity of the DCT which grows nonlinearly. In existing methods [2], the design cannot be extended for larger transform sizes such as 16-point and 32-point. DCTs for several image processing applications such as tracking and simultaneous compression and encryption require large transform sizes.

The idea of this paper is three-fold. First, review and implement hardware of approximate DCT using 8T MGDI Adder. It will possess reduced circuit complexity. Second, extending the architecture of 8-point MGDI 1D DCT for 16-point MGDI 1D DCT and third, proposes hardware implementation of MGDI 2D approximate DCT using MGDI 1D DCT.

Gate Diffusion Input (GDI) design technique [3] was confirmed as a new promising alternate to usual CMOS Logic design for low power digital systems. The basic GDI inverter is similar to the standard CMOS inverter, but there are few important differences.

1) The three inputs of GDI cell are G (gate input of both), P (input to the source of pMOS), and N (input to the source nMOS).

2) Bulks of the transistors are connected to the source.

MGDI [4] cell bulk of PMOS connected to supply voltage and bulk of NMOS connected to Ground in order to get full-swing output.

The paper unfolds as follows. Section II presents a literature survey. Section III introduces the methods and materials employed in this work. Section IV gives the proposed work. Section V reports the observational results and its discussion. Section VI concludes the paper.

II. LITERATURE REVIEW

Features of approximate DCT are its low computational complexity, orthogonality, low error energy and should work for higher lengths of DCT. The existing methods are not efficient in terms of scalability, generalization for higher sizes, and orthogonality. Error energy is reduced in the DCT due to orthogonality property.

The transformation matrix of the 8-point DCT approximation methods is mathematically described as [Diagonal matrix] x [low-complexity matrix]. (2)

The reduced complexity of the diagonal matrix reduces the complexity of the approximation. The irrational numbers in the form $1/\sqrt{m}$, where m is a small positive integer forms the diagonal matrix. The computational complexity of the diagonal matrix is increased by this irrational numbers. Since the entries of the low complexity matrix comprise only powers of two {0, ±1/2, ±1, ±2}, multiplicative complexity achieved is null.

In [5], a low complexity approximate was introduced by Bouguezel et al. and called BAS-2008 Approximation. Its mathematical structure is $C_1=D_1.T_1$ where D_1=diag($1/\sqrt{8}$, $1/\sqrt{4}$, $1/\sqrt{5}$, $1/\sqrt{2}$, $1/\sqrt{8}$, $1/\sqrt{4}$, $1/\sqrt{5}$, $1/\sqrt{2}$}.It requires only 18 additions and 2 shifts for its computation.

The parametric transform proposed in 2011 by Bouguezel-Ahmad-Swamy [6] is an 8-point orthogonal transform containing a single parameter 'a'. Its mathematical structure is $C_1=D_1.T_1$ where D_1=diag ($1/\sqrt{8}$, $1/\sqrt{2}$, $1/\sqrt{(4+4a^2)}$, $1/\sqrt{2}$, $1/\sqrt{8}$, $1/\sqrt{2}$, $1/\sqrt{2}$, $1/\sqrt{(4+4a^2)}$}.It requires only 16 additions for its computation.

In [7], CB-2011 rounding-off the elements of exact DCT matrix, a DCT approximation was obtained. The resulting 8-point approximation matrix is orthogonal and contains elements only in {0, ±1}.It possesses very low arithmetic complexity. The transformation matrix $C_1=D_1.T_1$ where D_1=diag ($1/\sqrt{8}$, $1/\sqrt{6}$, 1/2, $1/\sqrt{6}$, $1/\sqrt{8}$, $1/\sqrt{6}$, $1/\sqrt{2}$, $1/\sqrt{6}$}.It requires only 22 additions for its computation.

In [8], CB-2011 is modified by replacing elements of the CB-2011 matrix with zeros. The transformation matrix $C_1=D_1.T_1$ where D_1=diag ($1/\sqrt{8}$, $1/\sqrt{2}$, 1/2, $1/\sqrt{2}$, $1/\sqrt{8}$, $1/\sqrt{2}$, 1/2, $1/\sqrt{2}$}.It needs only 14 addition for its computation.

In [9], a DCT approximation tailored for a particular radio- frequency (RF) application was obtained in accordance with an complete computational hunt. The transformation matrix $C_1=D_1.T_1$ where D_1=1/2.diag ($1/\sqrt{2}$, $1/\sqrt{3}$, $1/\sqrt{5}$, $1/\sqrt{3}$, $1/\sqrt{2}$, $1/\sqrt{3}$, $1/\sqrt{5}$, $1/\sqrt{3}$}. It requires only

Table 1. Comparison of Existing approximate DCTs

Arithmetic complexity analysis				
Method	Multiplications	Additions	Shifts	Total
Conventional DCT	64	56	0	120
BAS-2008	0	18	2	20
BAS-2011	0	16	0	16
CB-2011	0	22	0	22
Modified CB-2011	0	14	0	14
Potluri-2012	0	24	6	30
Potluri-2014	0	14	0	14
Vaithiyanathan-2014	0	12	0	12

24 additions and 6 shifts for its computation.

In [10], a low-complexity approximate DCT define the cost of a transformation matrix as the number of arithmetic operations required for its computation. Elements of matrix intend to be in {0, ±1, ±2} to insure that resulting multiplicative complexity is null. The transformation matrix $C_1=D_1.T_1$ where D_1=diag (1/√8, 1/√2, 1/2, 1/√2, 1/√8, 1/√2, 1/2, 1/√2}. It requires only 14 additions for its computation.

In [11], a low-complexity approximate DCT is obtained by reproducing the butterfly structure. The common computations are identified and shared to remove the redundancy in DCT matrix. Elements of matrix intend to be in {0, ±1} to insure that resulting multiplicative complexity is null. The transformation matrix $C_1=D_1.T_1$ where D_1= ½ .diag (1, 1, 1, 1, 1, 1, 1, 1}. It requires only 12 additions for its computation. All rows of $T_1$are non-null. Matrix T_1. T_1^T must be an orthogonal diagonal matrix.

Some of the existing methods are not efficient in terms of scalability, generalization for higher sizes and orthogonality. Error energy is reduced in the DCT due to orthogonality Property.

DCTs of large size are required for several image processing applications such as tracking and simultaneous compression and encryption.

The approximation is used to reduce the computational complexity. It can be obtained by using diagonal matrices with few non-zero coefficients. The elements of the low complexity diagonal matrix [12, 13] are only powers of two, null multiplicative complexity is obtained. In Table 1, the computational complexity for various existing 8-point approximate DCTs are listed. Common computations are identified and shared to remove redundancy in DCT matrix.

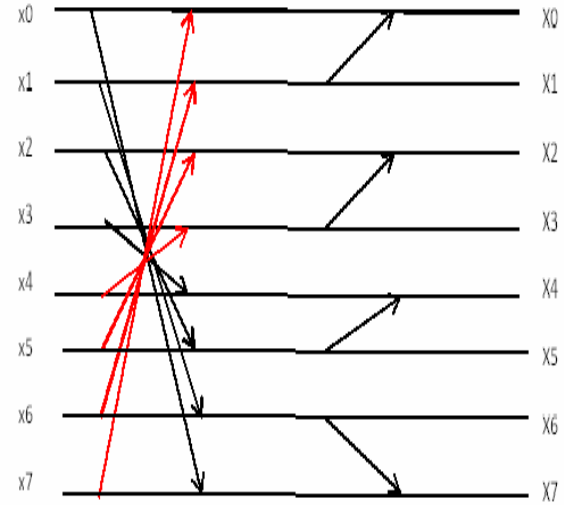

Fig. 1. Signal flow graph of approximate DCT using 12 additions.

After a detailed survey and simulation of existing approximate DCTs in Tanner Spice, a low-complexity 8-point approximate DCT using only 12 additions is preferred.

III. Methods and Materials.

1. Digital Architecture of 8-point Approximate 1D DCT

The approximate DCT [11] matrix contains only zeros and ones which requires only adders and eliminates multipliers and shifters. The number of adders are further reduced which in turn reduces the computation complexity.

$$X=\begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \\ 1 & 1 & 0 & 0 & 0 & 0 & 1 & 1 \\ 0 & 0 & 1 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 1 & 1 & 1 & 0 & 0 \\ 0 & 0 & 1 & 1 & -1 & -1 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & -1 & 0 & 0 \\ 1 & 1 & 0 & 0 & 0 & 0 & -1 & -1 \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 & -1 \end{bmatrix}$$

The signal flow graph in Fig. 1 shows the number of additions in this transform. The black and red line represents multiplication by +1 and -1 respectively.

This DCT approximation is reproducing and reviewing

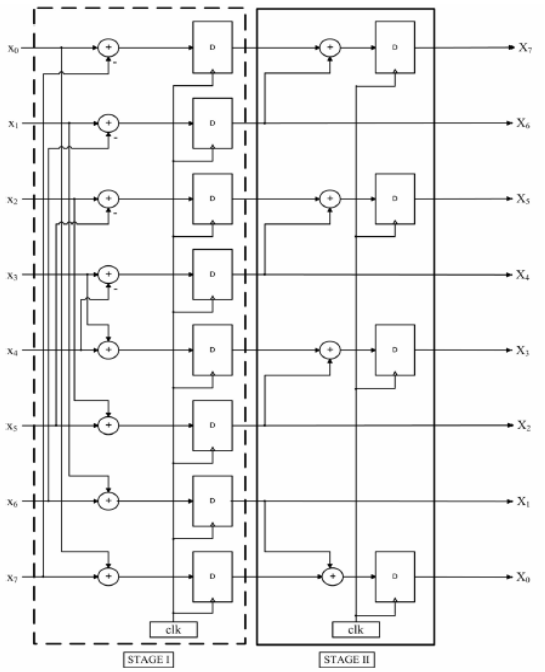

Fig. 2. Digital Architecture of 8-point approximate DCT.

the butterfly structure. The Digital architecture of approximate DCT using 12 additions is shown in Fig. 2.

2. Modified Gate Diffusion Input.

Modified-GDI [MGDI] cell contains a low-voltage terminal (bulk of PMOS) configured to be connected to a high constant voltage (i.e. supply voltage) and a high-voltage terminal (bulk of NMOS) configured to be connected to a low constant voltage (i.e. Ground) in order to get full-swing output.

Existing MGDI Full Adder uses 10 Transistors, 5 PMOS and 5 NMOS which is used for the addition of 1-bit numbers.

A. 8T MGDI Full Adder

MGDI Full Adder using 8 Transistor is proposed. 5 PMOS and only 3 NMOS transistors are used.

The actual operation of the MGDI [14] Full adder in Fig. 3 with equal strength transistors produces erroneous result. It can be overcome by designing the NMOS transistors N1 and N2 in the 8T MGDI adder as weak transistors when compared to the rest of PMOS and NMOS transistors.

The ideal equations in three regions of operation are

i) Cut-off (Vgs<Vt)

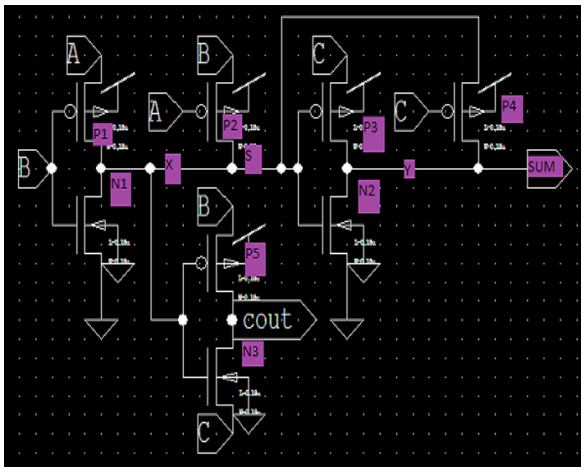

Fig. 3. 8T MGDI Full Adder.

$$I_{ds} \approx 0 \tag{3}$$

ii) Linear Region (Vgs>Vt, 0<Vds<Vgs-Vt)

$$I_{ds} = \beta[(v_{gs} - v_t)v_{ds} - \frac{v_{ds}^2}{2}] \tag{4}$$

iii) Saturation Region(Vgs>Vt ,0>Vds>Vgs-Vt)

$$I_{ds} = \frac{\beta}{2}\left(v_{gs} - v_t\right)^2 \tag{5}$$

where

$$\beta = \frac{W}{L}.\frac{\mu\varepsilon}{t_{ox}} \tag{6}$$

In all three regions of operation, $I_{ds} \propto \beta$, the transistor gain. The transistor gain $\beta \propto W, \beta \propto \frac{1}{L}.\beta$ decides the current driving capability of any transistor. By choosing transistor width W less than length L, driving current of the transistor is less and it is called weak transistor.

Full adders are the basic circuit for binary addition. Lot of full adders is available in CMOS logic which can be used to perform vector additions of n-bit data. A Modified GDI Full adder in Fig. 3 uses only 8 Transistors. For 1-bit adder, two transistors are reduced. The power consumption and delay are also reduced than 10T MGDI Full adder. The 8T MGDI full adder is used to construct 16-bit ripple carry adder for addition of 16-bit inputs which reduces the transistor count by 32. The binary subtraction can be performed by two's complement addition.

The 8-bit D Latch is designed to delay or latch 8-bit input data without waiting for clock. It will change state according to the change in data. The input is latched to subsequent stage of adders in DCT with unit delay.

IV. DIGITAL ARCHITECTURE OF MGDI APPROXIMATE DCT

An 8-point Approximate 1D-DCT architecture using 8T MGDI Full Adder is designed and simulated. The transistor count is reduced by 384 in addition to reduction in power and delay.

1. 16-point Approximate DCT using MGDI Adder

The 8-point DCTs were widely used in traditional video coding standards. However larger size 16/32-point DCT has in present and next generation video standard such as HEVC. To fulfill this requirement, this work proposes a fast computation intensive architecture for large size DCT.

Two units for the computation of C_8 are used along with an input adder unit and output permutation unit. The structures of 16-point DCT of Fig. 4 [15] could be extended to obtain the DCT of higher sizes. A pair of 16-point DCTs with an input adder block and output permutation block can be combined to obtain the structure for the computation of 32-point DCT and so on.

It can be found that the proposed method requires the lowest number of additions, and does not require any shift operations. Shift operation has indirect contribution to the hardware complexity because it increases bit-width which is given to the arithmetic units. Significance of approximation methods are less computational complexity than conventional DCT algorithms. In conventional DCT, an 8-point 1D DCT requires 64 multiplications and 56 additions and 8-point 2D DCT requires 1024 multiplications and 896 additions. Approximate DCT [11] computation requires only 12, 40, 112 and 288 additions respectively for 8, 16, 32, and 64-point with no multiplications.

2. Two Dimensional Approximate DCT using MGDI Adder

An 8 or 16-point Approximate 1D DCT architecture using 8T MGDI Full Adder is useful for transforming one dimensional signal like speech. But the two dimensional signals like image and video needs 2D DCT for its processing. So an Approximate 2D-DCT architecture using 8T MGDI Full Adder is designed.

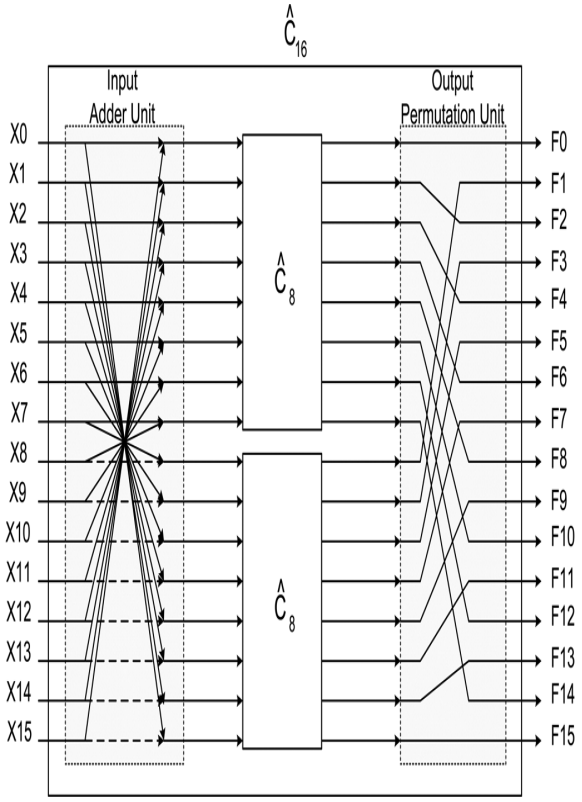

Fig. 4. Block diagram of the approximate 16-point DCT.

The proposed digital architectures are custom designed for the real-time implementation of the approximate algorithms [5-11].The proposed architecture employs two parallel realizations of DCT approximation blocks, as shown in Fig. 5.

The 1-D approximate DCT blocks implement a particular approximate algorithm chosen from the existing works. The first and second instantiation of the DCT block furnishes a row wise and column wise transform computation of the input image respectively. The row and column wise transforms can be any of the existing DCT approximations. Both row and column wise transforms need not be the same. However, for simplicity, identical transforms for both steps are adopted.

A. Transposition Buffer

Between the approximate DCT blocks a real-time row parallel transposition buffer circuit is required. It orders

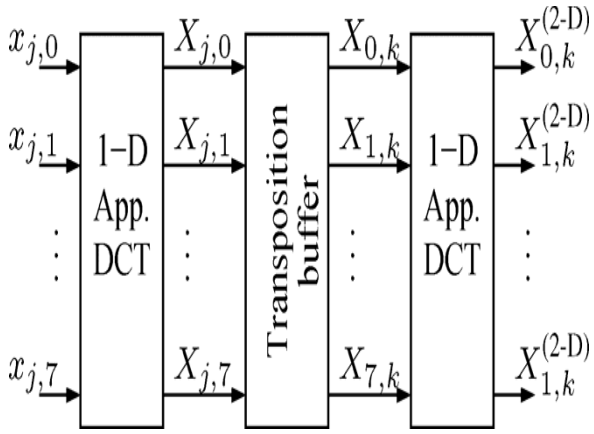

Fig. 5. Two dimensional approximate transform by means of 1D approximate transform.

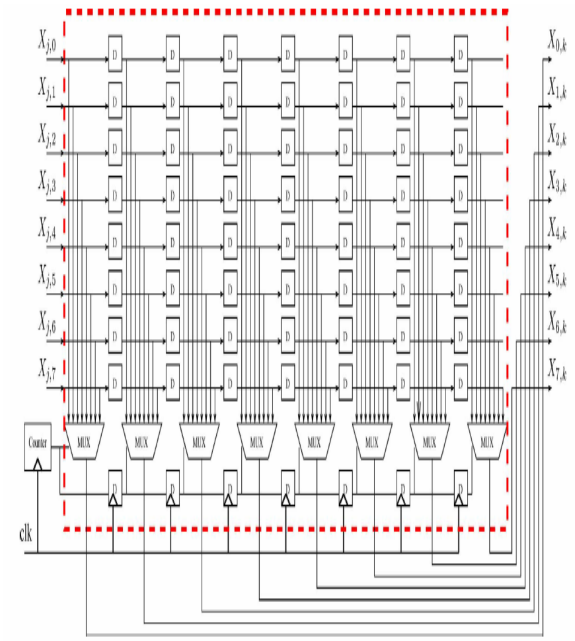

Fig. 6. Detailed circuit of the transposition Buffer Block.

the row transformed data from the first DCT approximation circuit to a transposed format as required by the column transform circuit. The transposition buffer block is detailed in Fig. 6.

V. Results and Discussions

The conventional DCT requires 64 additions and 56 multiplications. Approximate DCTs with reduced circuit complexity can be used for image and videos.

The approximate DCT algorithm [10] requires only 14 additions, which are simpler and makes the design energy efficient. The approximate DCT matrix [11] contains only zeros and ones which also requires only adders reduced to 12.

Table 2. Comparison result of 1D Approximate 8-point DCTs

8 Point DCT	Area(No.of transistors)	Power(watts)
CMOS Conventional DCT	124208	3.57e-01
10T MGDI Conventional DCT	97792	2.812e-01
8T MGDI Conventional DCT	87680	2.005e-01
8T MGDI Approximate DCT using 14 additions	4112	3.332e-04
8T MGDI Approximate DCT using 12 additions	3136	2.778e-04

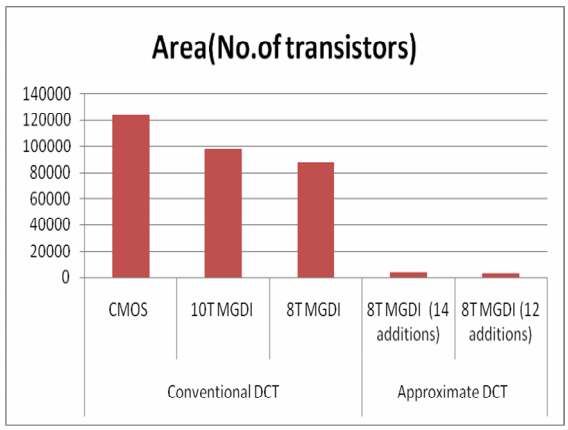

Fig. 7. Transistor Count of Approximate 8-point 1D DCTs.

1. Comparison of 8 Point DCT Architectures.

A proposed Full adder using MGDI uses only 8 Transistors whereas existing MGDI uses 10 transistors. So complexity and also power is further reduced by using MGDI Full adder for DCT using 12 additions. It is extended for 16-point approximate DCT. Finally 2D 16-point approximate MGDI DCT is proposed and analysed. The results of this proposed work is discussed.

The conventional DCT gives accurate results but having high circuit complexity. The architecture for 8-point DCT is implemented with CMOS logic, GDI and MGDI technique and compared. Humans are able to perceive and identify the information from slightly erroneous images. Approximate DCTs reduce the circuit complexity with slight compromise in accuracy. The approximate DCT [10] requiring 14 additions and [11] requiring 12 additions are compared in terms of area and power shown in Table 2, Fig. 7 and 8 for MGDI Implementation.

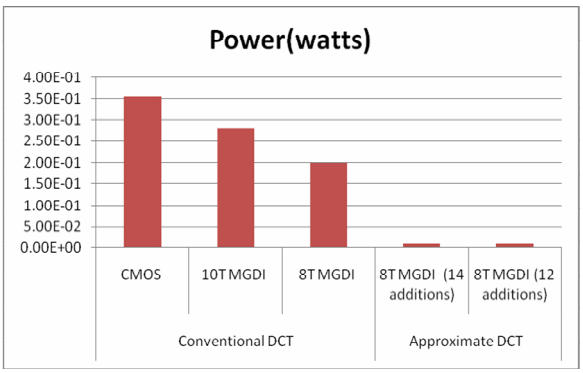

Fig. 8. Power consumption of various 1D Approximate DCTs.

Table 3. Comparison result of 16 point Approximate DCTs

16 Point DCT	Area(No. of transistors)	Power(watts)
MGDI Approximate 1D DCT [10]	9376	6.72e-04
MGDI Approximate 1D DCT [11]	7424	5.58e-04

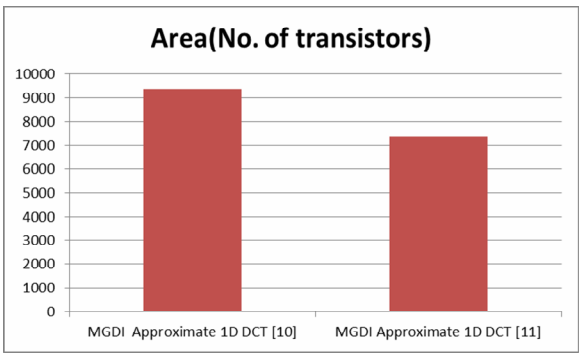

Fig. 9. Transistor Count of 16-Point Approximate DCTs.

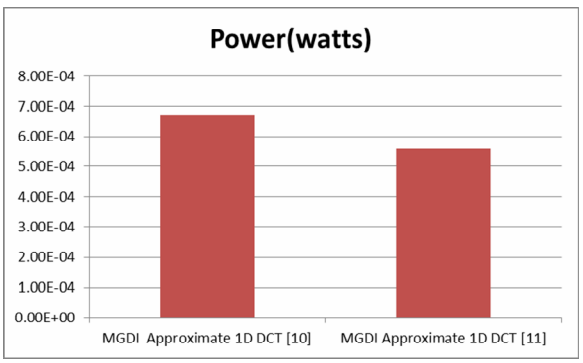

Fig. 10. Power Consumption of 16-Point Approximate DCTs.

2. 16 point Approximate DCT

Two units for the computation of C_8 are used along with an input adder unit and output permutation unit in 16-point Approximate DCT [15]. The structures of 16-point DCT could be extended to obtain the DCT of higher sizes. The approximate 16-point DCT architecture for C_8 with 14 1nd 12 additions are implemented with MDGI technique and compared in terms of area and power shown in Table 3, Fig. 9 and 10.

Table 4. Comparison result of 2D approximate 8-point DCTs

DCT	Area (No. of transistors)	Power (watts)
MGDI Approximate 2D 8-point DCT [10]	14016	4.1218e-02
MGDI Approximate 2D 8-point DCT [11]	12064	3.50e-002
MGDI Approximate 2D 16-point DCT [10]	31958	8.312e-02
MGDI Approximate 2D 16-point DCT [11]	28560	7.025e-02

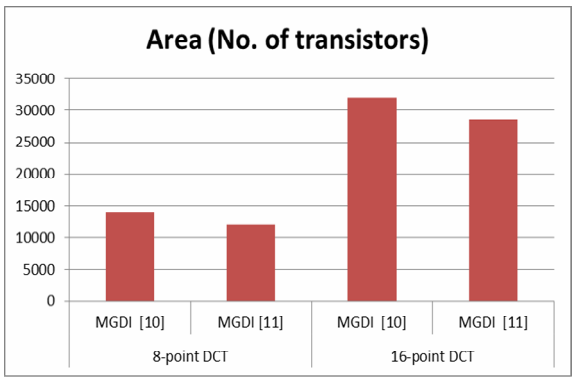

Fig. 11. Transistor Count of various 2D Approximate DCTs.

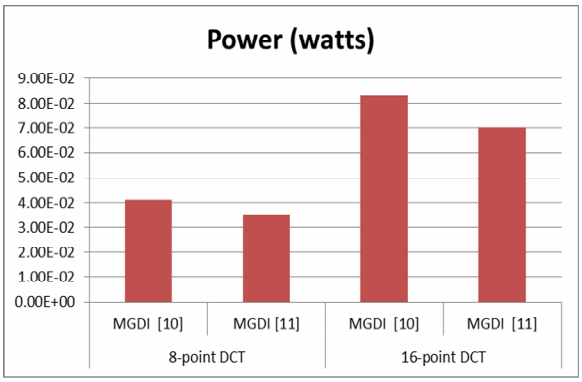

Fig. 12. Power Consumption of various 2D Approximate DCTs.

3. Two Dimensional Approximate DCT

In 2D approximate DCT, the first instantiation of the DCT block furnishes a row wise transform computation of the input image, while the second implementation furnishes a column wise transformation of the intermediate result.

A transformation buffer is used in between row and column transformation. The 2D approximate 8-point and 16-point DCT architecture for C_8 with 14 and 12 additions are implemented with MDGI technique and compared in terms of area and power shown in Table 4, Fig. 11 and 12.

VI. CONCLUSION

A digital implementation of 16-point approximate 2D DCT architecture based on one-dimensional (1D) DCT and Modified Gate Diffusion Input (MGDI) technique is proposed. Conventional DCT produces exact results but the complexity is too high. So Approximate DCT architectures are used which reduces the computational complexity. From the review and simulation of existing approximate DCTs, an 8-point DCT architecture using 12 additions is chosen. The proposed 8T MGDI Full Adder is used to replace the adders of approximate DCT. The proposed 8T MGDI Adder reduces 13.9% of area and 15.08 % of power of the 8-point approximate DCT. A 16-point Approximate DCT and the 2D architecture for 8 and 16-point DCT are developed. It results in reduction of 10.63 % of area and 15.48% of power in 16-point approximate 2D DCT using 8 Transistor MGDI Full Adder than existing 10 Transistor MGDI Full Adder. Approximate multiplier-free MGDI DCTs are simulated in Tanner SPICE for 0.18 µm CMOS process technology at 100 MHZ.The proposed architecture is found to offer many advantages in terms of hardware complexity, regularity and modularity with a little compromise in accuracy.

REFERENCES

[1] M. Rezaei, S. Wenger and M. Gabbouj, "Video rate control for streaming and local recording optimized for mobile devices," *in Proc. IEEE 16th International Symposium Personal, Indoor Mobile Radio Communications (PIMRC)*, vol. 4, 2005.

[2] K. Lengwehasatit and A. Ortega, "Scalable variable complexity approximate forward DCT," *IEEE Transactions on Circuits System. Video Technology*, vol. 14, no. 11, 2004.

[3] Arkadiy Morgenshtein, Viacheslav Yuzhaninov, Alexey Kovshilovsky, Alexander Fish, "Full-Swing Gate Diffusion Input logic—Case-study of low-power CLA adder design" *INTEGRATION, the VLSI journal*, vol. 47, no.1, 2014.

[4] Pankaj Verma, Ruchi Singh and Y. K. Mishra, "Modified GDI Technique - A Power Efficient Method for Digital Circuit Design" *International Journal of Electronics and Computer Science Engineering*, vol. 2, no. 4, 2013.

[5] S. Bouguezel, M. O. Ahmad, and M. N. S.Swamy, "Low-complexity 8x8 transform for image compression", *Electronics Letter*, vol. 44, no. 21, 2008.

[6] S. Bouguezel, M. O. Ahmad, and M. N. S. Swamy, "A low-complexity parametric transform for image compression" *in Proceedings of the IEEE International Symposium on Circuits and Systems*, 2011.

[7] R. J. Cintra and F. M. Bayer, "A DCT approximation for image compression", *IEEE Signal Processing Letter*, vol. 18 no. 10, 2011.

[8] F. M. Bayer and R. J. Cintra, "DCT-like transform for image compression requires 14 additions only", *Electronics Letter*, Vol. 48, no .15, 2012.

[9] U. S. Potluri, A. Madanayake, R. J. Cintra, F. M. Bayer, and N. Rajapaksha, "Multiplier-free DCT approximations for RF multi-beam digital aperture-array space imaging and directional sensing" *Meas. Sci. Technol.*, vol. 23, no. 11, 2012.

[10] Uma Sadhvi Potluri, Arjuna Madanayake, Renato J. Cintra, Fábio M. Bayer, Sunera Kulasekera, and Amila Edirisuriya, "Improved 8-Point Approximate DCT for Image and Video Compression Requiring Only 14 Additions", *IEEE Transactions on circuits and systems—I: Regular Papers*, vol. 61, no. 6, 2014.

[11] Vaithiyanathan Dhandapani, seshasayanan Ramachandran, "Area and power efficient architecture for image compression", *Eurasip journal of advances in signal processing*, 2014.

[12] D. Vaithiyanathan, R. Seshayanan, "Low Power DCT architecture for image compression", *proceeding of the international conference on advanced Computing and communication systems*, 2013.

[13] D. Vaithiyanathan, R. Seshayanan, s. Anith, K. Kunaraj, "A Low complexity DCT approximation for image compression with 14 additions",

proceeding of the international conference on Green Computing, Communication and Conservation of energy, 2013.

[14] Dhilip Kumar, Karthik Raja, Hari Kannan, Thiruveni, "A Novel Design of Low Power 8T-CMOS Full Adder", *International Journal of Applied Engineering and Research*, vol. 10, no. 5, 2015.

[15] F. M. Bayer, R. J. Cintra, A. Edirisuriya, and A. Madanayake, "A digital hardware fast algorithm and FPGA-based prototype for a novel 16-point approximate DCT for image compression applications", *Meas. Sci. Technol.*, vol. 23, no. 11, 2012.

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