JOURNAL OF SEMICONDUCTOR TECHNOLOGY AND SCIENCE, VOL.16, NO.4, AUGUST, 2016
http://dx.doi.org/10.5573/JSTS.2016.16.4.443
ISSN(Print) 1598-1657
ISSN(Online) 2233-4866

A 2 GHz 20 dBm IIP3 Low-Power CMOS LNA with Modified DS Linearization Technique

Habib Rastegar[1], Jae-Hwan Lim[2], and Jee-Youl Ryu[1,*]

***Abstract*—The linearization technique for low noise amplifier (LNA) has been implemented in standard 0.18-µm BiCMOS process. The MOS-BJT derivative superposition (MBDS) technique exploits a parallel LC tank in the emitter of bipolar transistor to reduce the second-order non-linear coefficient (g_{m2}) which limits the enhancement of linearity performance. Two feedback capacitances are used in parallel with the base-collector and gate-drain capacitances to adjust the phase of third-order non-linear coefficients of bipolar and MOS transistors to improve the linearity characteristics. The MBDS technique is also employed cascode configuration to further reduce the second-order nonlinear coefficient. The proposed LNA exhibits gain of 9.3 dB and noise figure (*NF*) of 2.3 dB at 2 GHz. The excellent *IIP3* of 20 dBm and low-power power consumption of 5.14 mW at the power supply of 1 V are achieved. The input return loss (S_{11}) and output return loss (S_{22}) are kept below -10 dB and -15 dB, respectively. The reverse isolation (S_{12}) is better than -50 dB.**

***Index Terms*—BiCMOS, low noise amplifier (LNA), RF, MBDS technique, derivative superposition (DS), current-reused**

I. INTRODUCTION

The low-noise amplifier (LNA) is a crucial component for radio receivers, and it must meet several requirements such as good input matching, adequate gain and reasonably low noise figure (*NF*) to elevate received signal-to-noise ratio (*SNR*) as well as energy-efficiency for battery-powered portable devices [1, 2]. In the modern wireless communication systems such as WLAN, UMTS, PCS and 4 G LTE, due to the large-scaled interference signals at the input port of the LNA, high linearity is an important requirement for broadband receivers. For narrowband LNA design, one may only need to high third-order linearity, while for UWB LNA design; we need to consider both the second-order and third-order distortions due to the large numbers of in-band interferences, and the cross-modulation/inter-modulation caused by blockers or transmitter leakage [3].

Several techniques have been proposed to achieve high linearity. The pre-distortion method adds a nonlinear element (also called linearizer) prior to an amplifier such that the combined transfer characteristic of the two devices is linear. In practice, it is impossible to cancel all orders of nonlinearity simultaneously. Therefore, the linearizer is usually designed to cancel the nonlinearity of a certain order. Optimum gate biasing technique is based on the bias condition of the transistors at zero crossing point. The LNA achieves high linearity but the bottlenecks of this technique are that the bias point is bound to change due to the process variations, and the region over which this linearity boost can be obtained is very narrow [4]. The feedforward system has been used in many applications because of its unconditionally stable characteristics and ability to provide a broad-band and highly linear amplifier [5, 6]. However, the feedforward technique is very sensitive to component tolerance and drift, and it requires adaptive control [6].

Manuscript received Jul. 3, 2015; accepted Mar. 7, 2016
[1] Information and Communications Engineering, Pukyong National University, Busan, Korea
[2] Dongnam Institute for Regional Program Evaluation, Busan, Korea
E-mail : ryujy@pknu.ac.kr

Derivative superposition (DS) is the most favorite linearization technique to achieve high linearity [7, 8]. The DS is a special case of the feedforward technique. It consists of two parallel transistors. Main transistor works in the strong inversion region and the auxiliary transistor works in the weak inversion region. In DS method, by tuning the sizes and bias conditions of the transistors, the third-order nonlinear transconductance coefficient (g_{m3}) can be closed to zero. However, it is not necessary to completely eliminate the second-order nonlinear transconductance coefficient (g_{m2}) contribution to third-order intermodulation (IM_3). It is noteworthy that since DS method employs multiple transistors in parallel with their gates connected together, it is also called the "multiple gated transistor technique (MGTR)". Since in the DS technique the auxiliary transistor is biased in the triode region, the negative peak magnitude of g_{m3} is much smaller than the g_{m3} positive peak of the main transistor.

Therefore, the proposed LNA can improve both power gain and linearity in high-data-rate standards such as WiMAX, and 4 G LTE for handsets, and can be tuned to the desired frequency band. Examples of applications in these ISM bands include radio-frequency process heating, and medical diathermy machines. The powerful emissions of these devices can create electromagnetic interference and disrupt radio communication using the same frequency, so these devices were limited to certain bands of frequencies. In general, communications equipment operating in these bands must tolerate any interference generated by ISM equipment, and users have no regulatory protection from ISM device operation

In the proposed MBDS technique a parallel LC tank is used in the emitter of bipolar transistor to reduce the effect of g_{m2} on the third-order input intercept point (*IIP3*). Furthermore, MBDS technique is used in the cascode configuration to further reduce the g_{m2}. By paralleling two capacitances with the gate-to-drain and base-to-collector capacitances of the MOS and bipolar transistors, the phase of g_{m3} can be adjusted respectively, and then the *IIP3* of the whole LNA can be enhanced. The proposed LNA has several applications such as UMTS, PCS and 4 G LTE.

This paper is organized as follows. In section II, we bring the technical discussions in depth detail, and we prove our proposed idea with mathematic equations and results. In section III, measurement results along with brief explanations and comparison summary with recently published works will be discussed. At the end of this paper, the summary of this work will be presented in conclusion section.

II. Circuit Design and Linearization

1. Fundamentals

In transistors the major factor for nonlinear behavior of the RF blocks is the nonlinear voltage-current relationship, and it is further degraded as the scaling down of the technology. The voltage-current relationship of transistors is as follows:

$$i = g_{m1}v + g_{m2}v^2 + g_{m3}v^3 \tag{1}$$

where g_{mi}, (i=1,2,3) is the i^{th}-order nonlinear coefficient. The *IIP3* is the most important parameter for monitoring the linearity performance of the whole LNA circuit and can be expressed as follows [6]:

$$IIP3 = \sqrt{\frac{4}{3}\left|\frac{g_{m1}}{g_{m3}}\right|} \tag{2}$$

Therefore, g_{m3} is the main source of non-linearity in LNAs and by cancelling out it, the linearity can be enhanced. The Taylor expansion series of bipolar transistor can be approximated as:

$$i_{CE} = \alpha_1 v_{be} + \alpha_2 v_{be}^2 + \alpha_3 v_{be}^3 \tag{3}$$

$$i_{CE} = I_{S0} e^{\frac{V_{BEQ}+v_{be}}{\varphi_t}} = I_{S0} e^{\frac{V_{BEQ}}{\varphi_t}} e^{\frac{v_{be}}{\varphi_t}} = I_Q e^{\frac{v_{be}}{\varphi_t}} \tag{4}$$

where V_{BEQ} is the base-to-emitter bias voltage, I_{S0} is saturation current, and φ_t is the thermal voltage. The third-order coefficient can be written as:

$$\alpha_3 = \frac{I_Q}{6\varphi_t^3} \tag{5}$$

According to Eq. (5), α_3 has positive value due to the exponential relationship between the collector current and base-to-emitter voltage. For MOS transistor with negative third-order coefficient the voltage-current

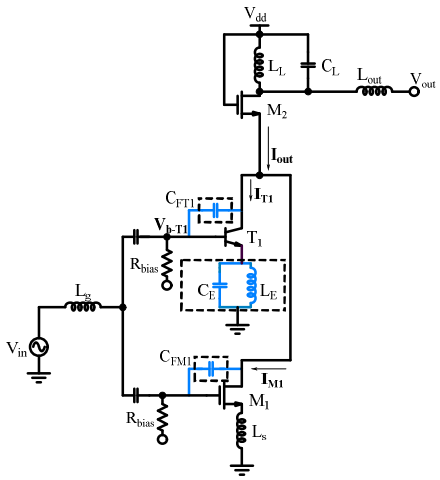


Fig. 1. Schematic of proposed LNA.

relationship is as follows:

$$i_{DS} = \beta_1 v_{gs} + \beta_2 v_{gs}^2 + \beta_3 v_{gs}^3 \quad (6)$$

$$i_{DS} = K\frac{x^2}{1+\theta x} \quad (7)$$

$$x = 2\eta\phi_t \, ln\left(1 + e^{\left(\frac{V_{gs}-V_{th}}{2\eta\phi_t}\right)}\right) \quad (8)$$

$$\beta_3 = -\frac{\theta K}{(1+\theta V_{eff})^4} \quad (9)$$

$$\begin{aligned} i_{out} = i_{DS} + i_{CE} &= (\alpha_1+\beta_1)v_{in} + (\alpha_2+\beta_2)v_{in}^2 \\ &+ (\alpha_3+\beta_3)v_{in}^3 \\ &= g_{m1}v_{in} + g_{m2}v_{in}^2 + g_{m3}v_{in}^3 \end{aligned} \quad (10)$$

where $K = 0.5\mu_o C_{ox} W/L$, μ_0 is the mobility, C_{ox} is the gate capacitance per unit area, θ is the normal field mobility degradation factor, $V_{eff} = V_{gs0} - V_{th}$, and V_{gs0} is the gate source dc bias voltage.

Fig. 1 shows schematic of proposed LNA using MBDS technique. As can be seen from Fig. 1, the bipolar current can be added to the MOS current at the output port to cancel out the g_{m3} of the entire LNA. From Eqs. (5-9) it appears that the sign of β_3 and α_3 is opposite. To get maximum cancelation of third-order term, the magnitude of β_3 and α_3 must be equal. The third-order term of bipolar transistor is usually more than β_3 of MOS transistor. At the resonance frequency, the emitter LC tank shows a resistance which is used to optimize the value of α_3 and hence to achieve high linearity. The phase and magnitude of g_{m3} in Eq. (10) are dependent on the biasing and the size of the transistors. By tuning the sizes and bias conditions of the transistors, the phase and magnitude of third-order nonlinear transconductance coefficient (g_{m3}) can be closed to zero.

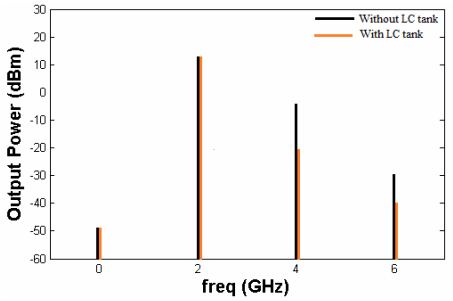


Fig. 2. Rejection of second and higher harmonics of the output power by using LC tank.

2. Nonlinear Base Capacitance in Bipolar Transistor

Although the bipolar transistor has power-handling capabilities, it has highly non-linear capacitance at the base junction [9]. This capacitor results in a large second-order harmonic, and it degrades the linearity performance.

A parallel LC tank (L_E, C_E) in Fig. 1 is used in the emitter of bipolar transistor (T_1) resonating at the second harmonic of fundamental tone to overcome the degradation of base capacitance. The LC network is employed as source degeneration circuit, and it decreases the current at 4 GHz. Since the L_E degenerates the fundamental tone, which results in a lower power, the inductor (L_E) should be chosen enough small. The L_E also should be small to have a high quality factor (Q), since the gain does not drop greatly. Thus, the values of the L_E and C_E are chosen to be 0.14 nH and 11.2 pF, respectively.

The second-order and higher harmonics are simulated with and without the LC tank and the results are shown in Fig. 2. As shown in Fig. 2, the LC tank attenuates the high-order harmonics of specially second-order harmonic.

3. Phase Adjustment by Feedback Capacitances

At high output powers, the nonlinear base-to-emitter capacitance (C_{BE}) of T_1 will change the phase of α_3 and β_3. The linearity performance will be degraded by this phase changing. By adding parallel feedback capacitances the phase of α_3 and β_3 can be adjusted. The values of C_{FM1} and C_{FT1} are 0.55 pF and 0.12 pF, respectively. Since there is nonlinear capacitance in the base of T_1, the currents i_{T1} and i_{M1} can be expressed as follows:

$$V_{b-T_1} = \rho_1 v_{in} + \rho_2 v_{in}^2 + \rho_3 v_{in}^3 \quad (11)$$

$$i_{T_1} = (v_0 - \rho_1 v_{in} - \rho_2 v_{in}^2 - \rho_3 v_{in}^3) C_{FT1} s + \alpha_1 v_{in} + \alpha_2 v_{in}^2 + \alpha_3 v_{in}^3 \quad (12)$$

$$i_{M_1} = (v_o - v_{in}) C_{FM1} s + \beta_1 v_{in} + \beta_2 v_{in}^2 + \beta_3 v_{in}^3 \quad (13)$$

$$v_o \approx -[(\alpha_1 + \beta_1) R_L] v_{in} \quad (14)$$

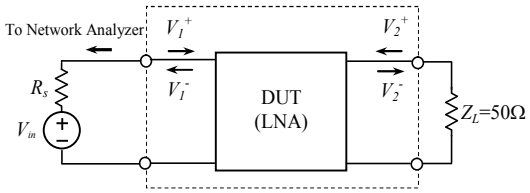
$$A_{IIP3} = \sqrt{\frac{4}{3}\left|\frac{j\omega(-(\alpha_1+\beta_1)R_L(C_{FM1}+C_{FT1}) - C_{FM1} - \rho_1 C_{FT1}) + (\alpha_1+\beta_1)}{-j\omega C_{FT1}\rho_3 + \alpha_3 + \beta_3}\right|} \quad (15)$$

where R_L is the resistor at the output port. As shown in Eq. (15), the phase difference between α_3 and β_3 can be compensated by using parallel feedback capacitances and the third-order intermodulation (IM_3) can be cancelled out.

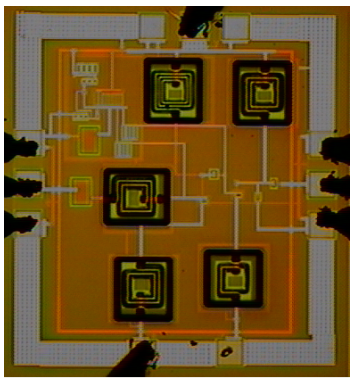
4. Design Considerations

In a receiver path, since the signal propagates from the antenna to digital back-ends, different blocks may introduce noise to the signal. The overall *NF* of the receiver depends on the *NF* of each block as well as the gain of preceding stages. Intuitively, larger signals are less susceptible to noise, and this is the reason that the large gain of one stage makes the noise of the following stage less important. Consequently the two major requirements for the LNA performance are low noise figure and high gain. The main contribution of the noise of an LNA is the first stage noise, and so a cascode topology with peaking technique (shunt technique) is chosen for the proposed LNA to achieve high gain and low noise figure.

The schematic of the whole LNA using MBDS technique is shown in Fig. 1. The MBDS technique consists of M_1 (MOSFET) and T_1 (BJT). By tuning the width of M_1 (W_1) and bias voltage of both transistors, the third-order nonlinear coefficient can be close to zero, and so the *IIP3* can be improved. To achieve good input return loss (S_{11}), series-gate inductance (L_g), source degeneration inductor (L_s) and parasitic capacitors make a LC ladder filter for resonance at the desired frequency. The current-reused topology is one of the suggestions to build an RF front-end, and it minimizes power dissipation [10, 11]. The second stage of M_2 is stacked on top of the first stage to achieve the goal of power saving. At the output, an inductor L_L is placed at the drain primarily for two reasons. The first reason is to resonate with the total drain capacitance to achieve the desired frequency range. The other reason is to provide high enough impedance to allow a good gain [12]. Furthermore, BJTs require less bias current than MOSFETs for the same amount of the third-order intermodulation. Therefore, the BJT contributes a small amount of noise to overall noise of LNA.



(a) Set-up



(b) Die probe

Fig. 3. Measurement setup for S-parameter of LNA.

5. Experimental Validation

Fig. 3 shows measurement setup for S-parameter of the LNA. Vector network analyzer and probe station measure the S-parameter by applying a known swept signal from a synthesized source. The S-parameter measurement has been used here which represent 2-port measurements. The powers of -20 dBm are applied from the synthesized sources at both port 1 and port 2. We applied the attentions of 0dB at both port 1 and port 2. The measured S-parameter was transferred to voltage gain, return losses and reverse isolation using conventional equations of ADS or MATLAB tool.

Let's consider Fig. 3 with the source (V_{in}) forming part of a network analyzer with a matched load (Z_L = 50Ω) at port 2 to measure transfer function (S_{21}) for the LNA. The S_{21} can be obtained by applying an incident wave at port 1, V_1^+, and by measuring the out-coming wave at

Table 1. Aspect ratio of transistors and the value of components

$(W/L)_1$	$(W/L)_2$	C_{FM1}	C_{FT1}	C_E
400μ/0.18μ	268μ/0.18μ	0.55pF	0.12pF	11.2pF
C_1	L_g	L_E	L_L	L_S
4.3pF	6.77nH	0.14nH	1.36nH	1.00nH

port 2, V_2^-. This is equivalent to the transmission coefficient from port 1 to port 2. Since S_{21} is a measurement of the gain at the network analyzer output, the transfer function $H(f)$ can be derived to be [1]

$$H(f) = S_{21} = \left.\frac{V_2^-}{V_1^+}\right|_{V_2^+=0}. \quad (16)$$

III. MEASUREMENT RESULTS

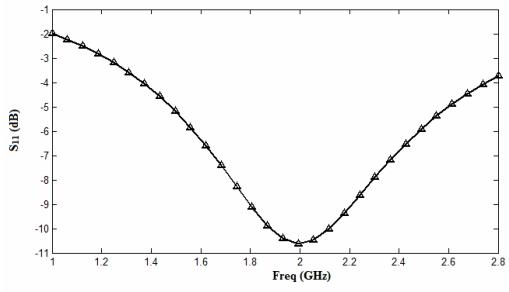
1. S-Parameter and Noise Figure Measurement

The proposed RF LNA is measured and fabricated in 0.18-μm Si-Ge BiCMOS process. The device dimensions and component values are given in Table 1. The linearity performance can be degraded by phase shift. This phase of α_3 and β_3 can be adjusted by adding parallel feedback capacitances. The values of C_{FM1} and C_{FT1} are 0.55 pF and 0.12 pF, respectively as shown in Table 1. Other values are selected to improve linearity from Eq. (15).

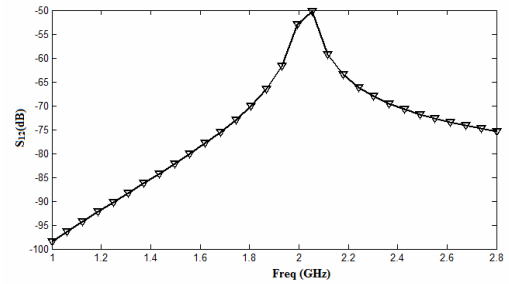
The S-parameter and *NF* of the proposed LNA is shown in Fig. 4. The voltage gain (S_{21}) is maximized at 2 GHz, while the input return loss (S_{11}) in the frequency of interest is -10.6 dB. The circuit showed very small output return loss (S_{22}) of -20.3 dB and the excellent reverse isolation (S_{12}) of -50 dB. The proposed LNA also showed the very small *NF* of 2.3 dB.

2. IIP3 and Stability Factor

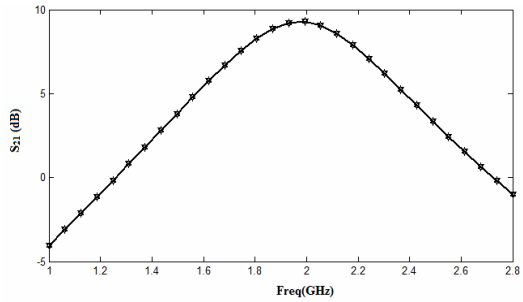
Fig. 5 shows *IIP3* and stability factor (K) of the LNA. Linearity in LNA is typically measured in terms of *IIP3* which is required to be maximized in [14]. Two-tone test was performed at 2 GHz with the spacing of 100 MHz. The *IIP3* of the LNA was maximized because of employing MBDS technique and using Eq. (15). In this paper, we analyze the effect of nonlinear capacitances such as gate-to-source (base-to-emitter) and gate-to-drain



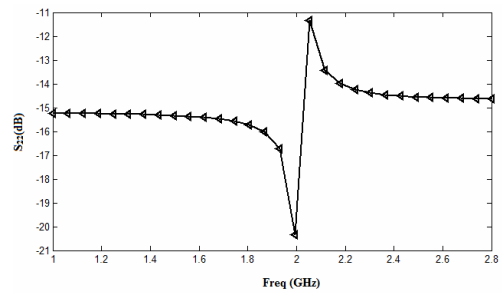
(a) Input return loss (S_{11})



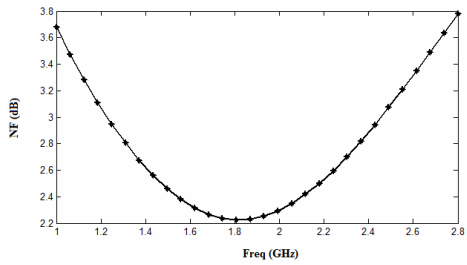
(b) Reverse isolation (S_{12})



(c) Voltage gain (S_{21})

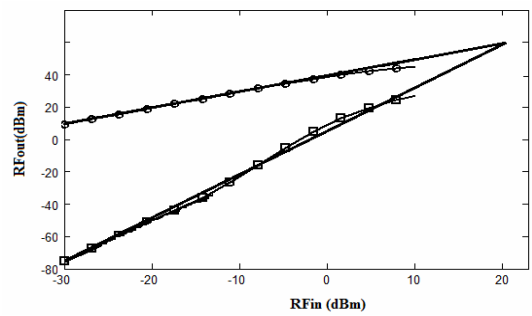


(d) Output return loss (S_{22})

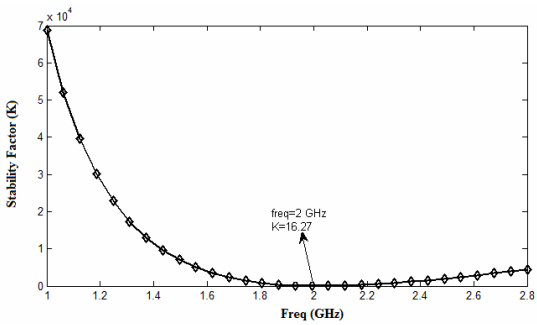


(e) Nose figure

Fig. 4. S-parameter and noise figure of the LNA.



(a) *IIP3*



(b) Stability factor (*K*)

Fig. 5. *IIP3* and stability factor of the LNA.

(base-to-collector) as well as transcoundactance, g_m (β_F) to improve the linearity. As shown in Fig. 4(a), the proposed LNA showed highest *IIP3* of 20 dBm as compared to conventional results [7, 8, 14].

In addition to all the major performance parameters, if the circuit operates as expected without undesirable oscillations which could practically destroy the active devices due to the voltage buildup, the stability of the LNA is a basic requirement [15]. The *K* and |Δ| are the popular parameters to measure the circuit stability. The values of *K* and |Δ| are obtained from Eqs. (17, 18) [16]. Since the *K* is greater than unity, and so the LNA is stable at the desired frequency as shown in Fig. 5.

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1 \quad (17)$$

$$K = \frac{1 - |S_{11}|^2 + |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} > 1 \quad (18)$$

The summary of the specifications of the proposed LNA as compared to recently published works is listed in Table 2. Using circuit analysis from Eq. (15) to achieve high linearity, the main transistor (NMOS) was biased in the strong inversion region while the auxiliary one (BJT) was biased in active region. The MBDS technique can be used to adjust the magnitude and phase of the third-order output current to ensure that they cancel each other out. A LC tank was used in the emitter of bipolar transistor to reduce the second-order nonlinear coefficient which degrades the linearity improvement. Two capacitances were used in parallel with the base-to-collector and gate-to-drain capacitances to adjust the phase of third-order nonlinear coefficient, respectively.

Table 2. Comparison summary of the recently published results

Performance	[7]	[8]	[14]	[15]	This work
Technology (μm)	0.18	0.13	0.18	0.18	0.18
Frequency (GHz)	1.35	3.66	5.5	2	2
S21 (dB)	9.36	14	20.5	26.25	9.3
NF (dB)	2.25	2	1.8-2.6	2.2	2.3
Power Consumption (mW)	13.5	2.43	1.98	0.96	5.14
IIP3 (dBm)	11.92	10.5	-6.2	NA	**20**

As shown in Table 2, the proposed LNA showed highest *IIP3* of 20 dBm as compared to recently reported results. This LNA also exhibited gain of 9.3 dB, noise figure of 2.3 dB, and power consumption of 5.14 mW at the power supply of 1 V at 2 GHz.

IV. CONCLUSIONS

The two-stage LNA for UMTS and 4G LTE applications was proposed to achieve high linearity by using MBDS technique. This technique was formed by two parallel transistors to improve the linearity performance. We achieved high linearity using the main transistor of NMOS biased in the strong inversion region and the auxiliary bipolar transistor biased in active region. To linearize MOS devices in CMOS technology, the usable possibility of BJT transistor was also explored. The proposed LNA showed excellent *IIP3* of 20 dBm as compared to recently reported results. This circuit also showed acceptable voltage gain of 9.3 dB, low noise figure of 2.3 dB, and low power consumption of 5.14 mW at the operation frequency of 2 GHz.

ACKNOWLEDGMENTS

This research was supported by Basic Science Research Program through the National Research

Foundation of Korea (NRF) funded by the Ministry of Education (2015R1D1A3A01015753).

REFERENCES

[1] W.-C. Choi and J.-Y. Ryu, "A Programmable Compensation Circuit for System-on-Chip Application", *Journal of Semiconductor Technology and Science*, Vol. 11, No. 3, pp.198-206, September 2011.

[2] B. Park, S. Choi, and S. Hong, "A Low-Noise Amplifier With Tunable Interference Rejection for 3.1- to 10.6-GHz UWB Systems", *IEEE Microwave and Wireless Components Letters*, Vol. 20, No. 1, pp.40-42, January 2010,.

[3] B. Guo and X. Li, "A 1.6–9.7 GHz CMOS LNA Linearized by Post Distortion Technique", *IEEE Microwave and Wireless Components Letters*, Vol. 23, No. 11, pp.608-610, November 2013.

[4] N. Nojima and T. Konno, "Cuber Predistortion Linearizer for Relay Equipment in 800 MHz Band Land Mobile Telephone System", *IEEE Transactions on Vehicular Technology*, Vol. VT-34, No. 4, pp. 169-177, November 1985.

[5] Y. Yang and B. Kim, "A New Linear Amplifier Using Low-Frequency Second-Order Intermodulation Component Feedforwarding", *IEEE Microwave and Guided Wave Letters*, Vol. 9, No. 10, pp. 419-421, October 1999.

[6] H. Rastegar and J.-Y. Ryu, "A Broadband Low Noise Amplifier with Built-In Linearizer In 0.13-μm CMOS Process", *Microelectron. Journal*, Vol. 46, No. 8, pp. 698-705, August 2015

[7] C. Xin and Sanchez-Sinencio, "A linearization technique for RF low noise amplifier", ISCAS, Vol. 4, pp.31-40, 313-16, May. 2004.

[8] H. Rastegar and A. Hakimi, "A High Linearity CMOS Low Noise Amplifier for 3.66 GHz Applications using Current-Reused Topology", *Microelectron Journal*, Vol. 44, No. 4, pp.301-306, April 2013.

[9] S. A. Maas, B. L. Nelson, and D. L. Tait, "Intermodulation in Heterojunction Bipolar Transistors", *IEEE Transactions on Microwave Theory and Techniques*, Vol. 40, No. 3, pp. 442-448, March 1992.

[10] T. Song, H.-S. Oh, S. Hong, and E. Yoon, "A 2.4-GHz Sub-mW CMOS Receiver Front-End for Wireless Sensors Network", *IEEE Microwave and Wireless Components Letters*, Vol. 16, No. 4, pp.206-208, April 2006.

[11] H.-H. Hsieh and L.-H. Lu, "A CMOS 5-GHz Micro-power LNA", 2005 IEEE RFIC Symposium, No. 1, pp.31-34, June 2005.

[12] S. Toofan, A. R. Rahmati, A. Abrishamifar, and G. R. Lahiji, "Low power and high gain current reuse LNA with modified input matching and inter-stage inductors", *Microelectronics Journal*, Vol. 39, No. 12, pp.1534-1537, December 2008.

[13] G. R. Karimi and S. B. Sedaghat, "Ultra low voltage, ultra low power low noise amplifier for 2 GHz applications", *International Journal of Electronics and Communications (AEU)*, Vol. 66, No. 1, pp.18-22, January 2012.

[14] G. Gonzalez, Microwave Transistor Amplifiers: Analysis and Design: Prentice-Hall, Inc., New Jersey, USA, 1997.

Habib Rastegar received the B.S. degree in electrical engineering from Hakim Sabzevari University, Mashhad, Iran, in 2009, and the M.S. degree in electrical and computer engineering from Bahonar University, Kerman, Iran, in 2013. He is currently working toward the Ph.D. degree in information and communications engineering at Pukyong National University. His research interests are design of RF/analog/mixed signal circuit/microwave and millimeter-wave integrated circuit and system design for wireless communication systems.

Jae-Hwan Lim received the BS degree in control and instrumentation engineering, MS degree in electronics engineering, and PhD degree in information and communications engineering from Pukyong National University, Busan, Korea, in 2001, 2003 and 2014, respectively. He is currently a senior researcher at Dongnam Institute for Regional Program Evaluation. His current research interests include MEMS technology, WLP, design of System-on-Chip, and the design of embedded system.

Jee-Youl Ryu received the BS and MS degrees in electronics engineering from Pukyong National University, Busan, Korea, in 1993 and 1997, respectively, and the PhD degree in electrical engineering from Arizona State University, Tempe, in December 2004. He is currently a professor at Pukyong National University. His current research interests include the design and testing of System-on-Chip, the design and testing of RF integrated circuits, and the design of embedded system.