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다중(multiple) TSV-to-TSV의 임피던스 해석

(The Impedance Analysis of Multiple TSV-to-TSV)

이 시 현*

(Sihyun Lee©)

요 약

본 논문에서는 기존의 2D IC의 성능을 개선하고 3D IC의 집적도와 전기적인 특성을 개선하기 위한 목적으로 연구되고 있는 TSV (Through Silicon Via)의 임피던스를 해석하였다. 향후 Full-chip 3D IC 시스템 설계에서 TSV는 매우 중요한 기술이며, 높은 집적도와 광대역폭 시스템 설계를 위해서 TSV에 대한 전기적인 특성에 관한 연구가 매우 중요하다. 따라서 본 연구에서는 Full-chip 3D IC를 설계하기 위한 목적으로 다중 TSV-to-TSV에서 거리와 주파수에 따른 TSV의 임피던스 영향을 해석하였다. 또한 이 연구 결과는 Full-chip 3D IC를 제조하기 위한 반도체 공정과 설계 툴에 적용할 수 있다.

Abstract

In this paper, we analyze the impedance analysis of vertical interconnection through-silicon vias (TSV) that is being studied for the purpose of improving the degree of integration and an electric feature in 3D IC. Also, it is to improve the performance and the degree of integration of the three-dimensional integrated circuit system which can exceed the limits of conventional two-dimensional a IC. In the future, TSV technology in full-chip 3-dimensional integrated circuit system design is very important, and a study on the electrical characteristics of the TSV for high-density and high-bandwidth system design is very important. Therefore, we study analyze the impedance influence of the TSV in accordance with the distance and frequency in a multiple TSV-to-TSV for the purpose of designing a full-chip three-dimensional IC. The results of this study also are applicable to semiconductor process tools and designed for the manufacture of a full-chip 3D IC.

Keywords : 3 Dimensional Integrated Circuit (3D IC), Through Silicon Via (TSV), Impedance

Ⅰ. Introduction

Recently, the chips have been developing as the ICs that having a high integration, low-power, high-speed, and economical efficiency in accordance with industries, markets, and technology trends[1].

This is made possible by the state-of-the-art semiconductor process technology, design tools, and SoC(System on a Chip) design technologies. In addition, they have been designed in 3D IC and is developed by a variety of techniques designed to increase the density and efficiency of the chip. In order to design the 3D IC, the TSV is used through the entire silicon layer(silicon substrate) for the purpose of connecting a signal among the layers. Among these coupling problems in multiple TSV-to-TSVs, it is emerging as the most difficult problem, and many studies have been made to solve them.

However, TSV-to-TSV coupling in full-chip 3D IC design is to be considered important in the design because it can be a cause to generate a large noise.

On the other hand, in order to design a 3D full-chip 3D IC for the low-power chip, high-density and high reliability, it must be analyzed and be guaranteed to be correctly interpreting elements in the multiple TSV-to-TSVs. These elements can be problems that consist of the coupling, thermal,

* 정회원, 동서울대학교 정보통신과 (Department of Information and Communication Engineering, Dong Seoul University)
© Corresponding Author (Email : lsh4185@du.ac.kr)
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electromagnetic, power delivery, and mechanical issues.

So, TSV-to-TSV related research for applications in 3D IC design has been working in the area that is coupling, thermal, electromagnetic, power delivery, and mechanical issues. In paper[2] and [3], coupling model in the multiple TSV-to-TSVs were analyzed by applying a multiple TSV coupling circuit models, a simplified circuit model. Also, in paper [2] and [3] they analyzed for the coupling analysis based on S-parameters, the termination condition of port, and the frequency analysis of the impedance of the three channels according to the frequency domain(low frequency region, middle frequency range, and high frequency region).

On the other hand, they interpreted the coupling effects in accordance with the gate size and crosstalk value corresponding to the distance between the TSVs. However, these interpretations were analyzed only in design tools.

Therefore, we performed an impedance analysis technique in the multiple TSV-to-TSV circuit models based on paper [2] and [3] for the purpose of applying it to the process and the design environment.

Also, the results of this study can be applied as parameters of the process and the design environment for designing and manufacturing a full-chip 3D IC.

Ⅱ. TSV-to-TSV Circuit Modeling of Full-Chip 3D IC

A. The TSV Structure in 3D IC

In order to design a 3D IC chip it must be designed in consideration of the number of problems that is, coupling, thermal, and electromagnetic etc. existing inside chip.

The TSV does not use in a 2D IC, but it mainly used in order to increase the degree of integration in 3D IC, and it present a lot of coupling among the TSVs. So the coupling should be considered as one of the most important elements in the 3D IC design.

Further, TSV-to-TSV coupling can cause a lot of noise. Also, metalized via in 3D IC is usually used copper($\sigma_c = 5.8\times10^7 S/m$), the metallic material of the insulator(dielectric) layer is used by a silicon oxide ($\sigma_{di} = 4$). Fig. 1 shows the structure of the TSV-to-TSV in 3D ICs, and Fig. 2 shows equivalent circuit of the multiple TSV-to-TSVs in 3D IC architecture.

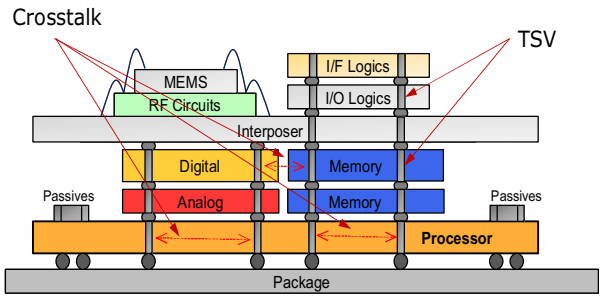


그림 1. 3D IC에서 TSV의 구조(예, 메모리, 프로세서, RF, MEMS 및 Interposers)[1~3]

Fig. 1. The structure of the TSV in 3D IC(for example memory, processor, RF, MEMS, and interposers))[1~3]

B. The Electrical Characteristics of the Multiple TSV-to-TSVs

In 3D IC, the impedance value of the TSV is influenced differently in each frequency range by the R, L, C value which exists between two TSV channels. Therefore, the impedance of the channel can be estimated by interpreting the circuit element(lumped circuit) at each frequency.

The impedance analysis among TSV-to-TSVs should be electrical characteristics based on physical structures which made of TSV insulator, the silicon layer, the bumps, and the I/O drive.

In Fig. 3, Eq. (1) is modeled to a silicon oxide insulation layer between the TSV and the silicon layer into the capacitor.

$$R_{tsv} = \frac{H}{2\pi}\sqrt{\frac{\pi f \mu_0}{\sigma_c}} \tag{1}$$

$$L_{ii} = \frac{\mu_0}{\pi} ln(\frac{P_{i0}}{R}), i = n \tag{2}$$

$$L_{ij} = \frac{\mu_0}{2\pi} ln(\frac{P_{i0}P_{j0}}{P_{ij}R}), i,j = n, i \neq j \tag{3}$$

Where, P_{i0} is the distance between the center to center and between the TSV #i and TSV #0, P_{ij} is the distance between the TSV#i and TSV #j.

$$C_{di} = \frac{\pi \epsilon_0 \epsilon_{di} H}{\ln[(R+T)/R]} \tag{4}$$

Where ε0 is the dielectric constant in free space, [Lsi] is a silicone matrix inductance, Lsi,ii is self-inductance loop, and Lsi,ij is mutual inductance-loop. This can be determined by formula (5).

$$L_{si,di} = \frac{\mu_0 H}{\pi} ln\left(\frac{P_{i0}}{R+T}\right) \tag{5}$$

Silicon capacitance that is Csi of Eq. (7) can be obtained from the relationship of Eq. (6).

$$L_{si,di} = \frac{\mu_0 H}{2\pi} ln\left[\frac{P_{i0}P_{j0}}{P_{ij}(R+T)}\right] \tag{6}$$

$$C_{si} = \mu_0 \epsilon_0 \epsilon_{si} H^2 [L_{si}]^{-1} \tag{7}$$

The C_{si} used here is defined by the Eq. (8).

$$[C_{si}] = \begin{bmatrix} \sum_{k=1}^{N} C_{1k} & -C_{12} \cdots & -C_{1N} \\ -C_{21} & \sum_{k=1}^{N} C_{2k} \cdots & -C_{2k} \\ -C_{N1} & -C_{N2} & \sum_{k=1}^{N} C_{Nk} \end{bmatrix} \tag{8}$$

When C_{si} calculated by Eq. (5) to Eq. (7), conductance matrix Gsi is calculated by the Eq. (9).

$$[G_{si}] = \frac{\sigma_{si}}{\epsilon_0 \epsilon_{si}} [C_{si}] \tag{9}$$

Ⅲ. The Impedance of the Multiple TSV-to-TSVs

In a multiple TSV-to-TSV circuit models of the 3D IC structure, TSV around is composed of the silicon layer, the bumps, and an insulator and TSV channel is a very high impedance to form a channel.

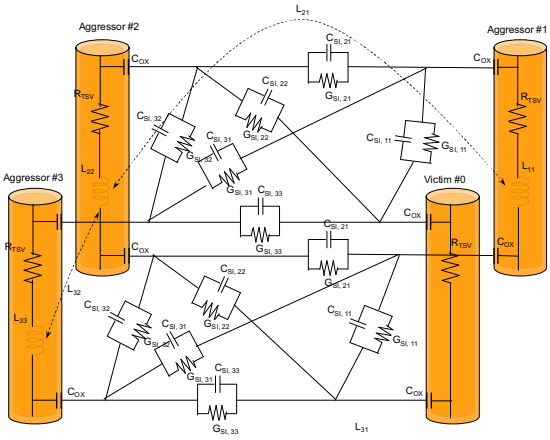


그림 2. 3D IC 구조에서 다중 TSV-to-TSV의 등가회로[1~3]

Fig. 2. Multiple TSV-to-TSVs equivalent circuit in a 3D IC architecture[1~3].

Fig. 3(a) is impedance model of TSV-to-TSV circuit that have four ports, and Fig. 3(b) is to analyze impedance between TSV-to-TSVs. In Fig. 3(b), when applying Kirchhoff's Law to interpret the impedance of the circuit can be obtained a relational expression for V_1 and V_2. Relationship of current i_1, i_2, and i_3 in Fig. 3(b) is the same as Eq. (10) through Eq. (14).

$$i_3 + i_2 = i_1 \tag{10}$$

$$i_3 = \frac{V_1 - V_2}{Z_5} \tag{11}$$

$$i_2 = \frac{V_1}{Z_2} \tag{12}$$

$$i_1 = \frac{V_{in} - V_1}{Z_1} \tag{13}$$

$$\frac{V_1 - V_2}{Z_5} + \frac{V_1}{Z_2} = \frac{V_{in} - V_1}{Z_1} \tag{14}$$

Also, the impedance Z_5 can be described by Eq. (15) and Eq. (16) in the Fig. 3(b). In a multiple TSV-to-TSVs circuit model of the 3D IC structure, TSV around is composed of the silicon layer.

$$Z_5 = \frac{Z_{CBump}(Z_{Csi} // Z_{Rsi} + 2Z_{C_{TSV}})}{Z_{Csi} // Z_{Rsi} + Z_{CBump} + 2Z_{C_{TSV}}} \tag{15}$$

$$\left(\frac{1}{Z_5} + \frac{1}{Z_2} + \frac{1}{Z_1}\right) V_1 - \frac{1}{Z_5} V_2 = \frac{V_{in}}{Z_1} \tag{16}$$

On the other, Relationship of current i_3, i_4, and i_5 in Fig. 3(b) can be described as Eq. (17) through Eq. (21). Eq. (22) is relationship between V_1 and V_2 for current i_3, i_4, and i_5.

$$i_4 + i_5 = i_3 \tag{17}$$

$$i_4 = -\frac{V_2}{Z_3} \tag{18}$$

$$i_5 = \frac{V_2}{Z_4} \tag{19}$$

$$i_3 = \frac{V_1 - V_2}{Z_5} \tag{20}$$

$$\therefore\ -\frac{V_2}{Z_3} + \frac{V_2}{Z_4} = \frac{V_1 - V_2}{Z_5} \tag{21}$$

$$-\frac{1}{Z_5} V_1 + \left(-\frac{1}{Z_3} + \frac{1}{Z_4} + \frac{1}{Z_5}\right) V_2 = 0 \tag{22}$$

When multiplied by $\frac{1}{Z_5}$ clean up on both sides of Eq. (22), it is as in Eq. (23) with respect to V_1 and V_2.

$$-V_1 + \left(-\frac{Z_5}{Z_3} + \frac{Z_5}{Z_4} + 1\right) V_2 = 0 \tag{23}$$

When expressing the Eq. (14) and (23) in the matrix is as Eq. (24).

$$\begin{bmatrix} \frac{1}{Z_1} + \frac{1}{Z_2} + \frac{1}{Z_5}, & -\frac{1}{Z_5} \\ -1 & 1 - \frac{Z_5}{Z_3} + \frac{Z_5}{Z_4} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} \frac{V_{in}}{Z_1} \\ 0 \end{bmatrix} \tag{24}$$

When write the Eq. (23) again, it is as shown in Eq. (25).

$$V_1 = \left(-\frac{Z_5}{Z_3} + \frac{Z_5}{Z_4} + 1\right) V_2 \tag{25}$$

Substituting the Eq. (23) in Eq. (16) and organized by the V_2 is the Eq. (26).

$$\left(\frac{1}{Z_1} + \frac{1}{Z_2} + \frac{1}{Z_3}\right)\left(-\frac{Z_5}{Z_3} + \frac{Z_5}{Z_4} + 1\right) V_2 - \frac{1}{Z_5} V_2 = \frac{V_{in}}{Z_1} \tag{26}$$

Eq. (27) is a summary of Z_1 by multiplying the both sides of Eq. (26) and Eq. (29) provides a summary of the Eq. (27). Here, in order to simplify the Equation, it leaves a and b as in Eq. (30) and Eq. (31), V_2 may finally be written as Eq. (31). Where Z_5 is the impedance of the TSV channels of the simplified model, this is the same with Eq. (31). Also we can be seen that Eq. (3.20) can be describe the impedance as a function of between the TSV terminal impedance(Z_2, Z_3, Z_4) and the driver condition(Z_1) as well as the channel(Z_5). Eq. (31) is a simplified Eq. (30) for Z_5.

$$Z_1\left(\frac{1}{Z_1} + \frac{1}{Z_2} + \frac{1}{Z_3}\right)\left(-\frac{Z_5}{Z_3} + \frac{Z_5}{Z_4} + 1\right) V_2 - \frac{Z_1}{Z_5} V_2 = V_{in} \tag{27}$$

$$\left(Z_1\left(\frac{1}{Z_1} + \frac{1}{Z_2} + \frac{1}{Z_3}\right)\left(-\frac{Z_5}{Z_3} + \frac{Z_5}{Z_4} + 1\right) - \frac{Z_1}{Z_5}\right) V_2 = V_{in} \tag{28}$$

$$\left(Z_1\left(\frac{Z_2Z_3 + Z_1Z_3 + Z_1Z_2}{Z_1Z_2Z_3}\right)\left(\frac{-Z_4Z_5 + Z_3Z_5}{Z_3Z_4} + Z_3Z_4\right) - \frac{Z_1}{Z_5}\right) V_2 = V_{in} \tag{29}$$

$$Z_1\left(\frac{Z_2Z_3 + Z_1Z_3 + Z_1Z_2}{Z_1Z_2Z_3}\right)\left(\frac{-Z_4Z_5 + Z_3Z_5}{Z_3Z_4} + Z_3Z_4\right) \equiv a,$$

$$\frac{Z_1}{Z_5} \equiv b \tag{30}$$

$$V_2 = V_{in} \times \frac{1}{(a-b)} \tag{31}$$

The following Eq. (32) through Eq. (35) are a formula for calculating the impedance respectively in the port of Fig. 3(a).

$$Z_A = R_{tsv} + jX_{L\_tsv} = R_{tsv} + j2\pi f L_{tsv} = \sqrt{R_{tsv}^2 + X_{L\_tsv}^2}$$

$$\text{where, } X_L = 2\pi f L_{tsv} \tag{32}$$

$$Z_B = 2\left(\frac{1}{2\pi f C_{tsv}}\right) + \frac{R_{si} X_{C\_si}}{\sqrt{R_{si}^2 + X_{C\_si}^2}} + 2\left(\frac{1}{2\pi f C_{tsv}}\right)$$

$$\text{where, } X_{C\_si} = \frac{1}{2\pi f C_{si}} \tag{33}$$

$$Z_C = R_{tsv} + jX_{L\_tsv} = R_{tsv} + j2\pi f L_{tsv} = \sqrt{R_{tsv}^2 + X_{L\_tsv}^2}$$

$$\text{where, } X_L = 2\pi f L_{tsv} \tag{34}$$

$$Z_T = Z_A + Z_B + Z_C \tag{35}$$

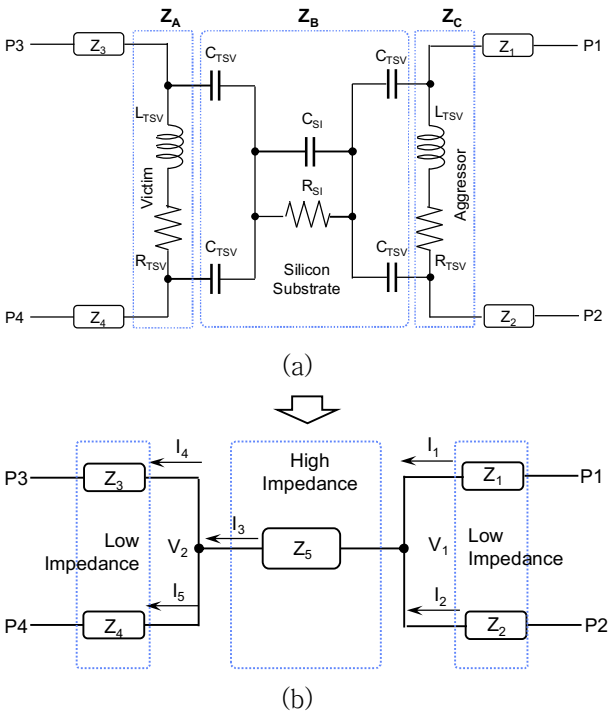


그림 3. 4개 포트를 갖는 TSV-to-TSV 회로모델 ((a) TSV-to-TSV 회로의 임피던스 모델, (b) 4개 포트에서 TSV-to-TSV 사이의 임피던스 해석))[1~3]

Fig. 3. TSV-to-TSVs circuit model with four port ((a) Impedance model of TSV-to-TSV circuit, (b) impedance analysis between TSV-to-TSV in the four port))[1~3].

IV. Simulations and Results

A. Simulation Environments and methods

The simulation was performed to calculate the impedance between the channels in accordance with the conditions of Table 1 in the circuit model of Fig. 3.

B. Channel Impedance Analysis

Interpreting the channel impedance with respect to frequency is calculated a change in the impedance value according to the change in frequency to a high frequency region in the low frequency region.

Fig. 4 is the detail dimensions in a cross-sectional view of the 3D IC that applied our simulation condition.

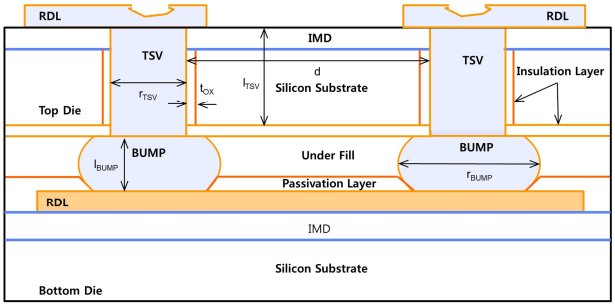


그림 4. 3D IC의 절단면에서 세부적인 Dimensions[9]

Fig. 4. The detail dimensions in a cross-sectional view of the 3D IC[9]

표 1. 시뮬레이션을 위한 3D IC 파라메타

Table 1. 3D IC parameters for simulation.

Parameters	Values
r_{TSV}(TSV radius)	$2.5\mu m$
l_{TSV}(TSV height)	$75\mu m$
ϵ_0(dielectric constant of in air)	$8.854187\times10^{-12}F/m$
$\epsilon_{si}(\epsilon_{si}=11.9\epsilon_0)$	$11.9\times8.854187\times10^{-12}F/$
r_{bump}(bump radius)	$5.0\mu m$
l_{bump}(bump height)	$10\mu m$
ϵ_r(dielectric constant of linear)	4
α(scaling factor)	$24\mu m$
d(pitch between TSVs)	$10\mu m$
t_{ox}(insulator thickness)	$0.5\mu m$
ρ_{si}(conductivity of silicon)	$11.9\Omega m$
L_{TSV}	$10pH$
R_{TSV}	$50m\Omega$
μ_0(permeability in free space)	$4\pi\times10^{-7}H/m$
σ_c(copper conductivity)	$5.8\times10^{7}S/m$

C. Simulation Results

Simulations were performed to analyze the impedance according to the distance and the frequency change between two TSVs using the parameters in Table 1. Table 2 is a variation of the impedance with respect to the frequency change, and Table 3 is an impedance changes according to the distance between the TSV-to-TSVs.

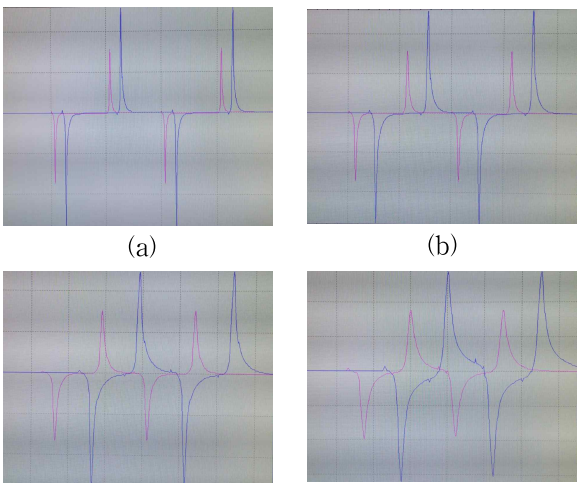
Fig. 5 shows result of performing in each $1GHz$, $2GHz$, $4GHz$, $8GHz$, $10GHz$. Also, the value of components are $L_{TSV}=10pH$, $R_{TSV}=0.05\Omega$, $C_{TSV}=100fF$, $C_{si}=200pF$, $R_{si}=100\Omega$, $C_{Bump}=0$. The distance between TSV-to-TSV is $10\mu m$, $20\mu m$, $40\mu m$, $80\mu m$, and $100\mu m$.

As the frequency increases, the simulation results shown in Fig. 4 can be seen that the noise of victim increased. Impedance can be seen that give more influence on the high frequency domain.

In addition, C_{si} is a factor determined by the distance change. The distance change between the TSVs at a low frequency range(under $1GHz$) does not have a significant effect on the impedance. This key element of the coupling is C_{TSV} and C_{TSV} is due to the TSV distance hardly changes.

In an intermediate frequency range($2GHz$, $4GHz$), impedance in accordance with the distance between two TSVs changes little effect on the impedance of the aggressor. This is because C_{si} and R_{si} are factors affecting C_{TSV}. In the high frequency region($8GHz$, $10GHz$) a distance change between the TSV showed the greatest effect on the impedance of the other channel. This is because it is a major factor in the channel impedance effect.

In addition, the impedance variation with frequency change has a value higher impedance at higher frequency range in the low frequency region, And impedance according to the distance between the TSV-to-TSVs showed that the smaller the distance value is smaller impedance.



(a) (b) (c) (d)

그림 5. 주파수에 대한 임피던스((a) $1GHz$, (b) $2GHz$, (c) $4GHz$, (d) $8GHz$)

Fig. 5. Impedance according to the frequency((a) $1GHz$, (b) $2GHz$, (c) $4GHz$, (d) $8GHz$)

표 2. 주파수 변화에 따른 임피던스 변화

Table 2. Impedance changes according to the frequency change.

Freq.	×1	×2	×4	×8	×10
$Zb(K\Omega)$	0.95	1.91	3.81	7.73	9.53

표 3.

Table 3. Impedance changes in TSV-to-TSV distance.

Dist.	×1	×2	×4	×8	×10
$Zb(K\Omega)$	10.49	11.44	13.35	17.16	19.07

VII. CONCLUSIONS

In this paper, on the basis of a result of the paper [2] and [3] for the purpose of applying the full-chip 3D IC design, we analyzed the impedance effect among the TSVs according to input frequency and analyzed impedance of the TSV-to-TSV in a multiple TSV-to-TSVs in order to use as parameter of 3D IC design.

In the simulation results, impedance of aggressor TSV in a multiple TSV-to-TSVs increased the impedance among the TSV-to-TSVs at a higher frequency range rather than at a low frequency region. Also, impedance of the victim TSV increased impedance depending on the distance among the TSV-to-TSVs at the same conditions.

Therefore, the results of this study also are applicable to the semiconductor process tools and the manufacture of a full-chip 3D IC.

Based on the studied results so far, in the future, we'll be carried out more research on the coupling, the thermal, the electromagnetic, the power delivery, and the mechanical issues in a full-chip 3D IC design. And they can use as the design parameters of the full-chip 3D IC.

References

[1] Sung Kyu Lim, Design for High Performance, Low Power, and Reliable 3D Integrated Circuit, Springer Press, 2013, ch. 1.

[2] Taigon Song et al. Lim. Analysis of TSV-to-TSV Coupling with High-Impedance Termination in 3D ICs. IEEE, 2011.

[3] Taigon Song, Chang Liu, Yarui Peng, and Sung Kyu Lim, Full-Chip Multiple TSV-to-TSV Coupling Extraction and Optimization in 3D ICs. DAC'13, May 29-June 07 2013.
[4] Yu-Jen Chang, Hao-Hsiang Chuang, Yi-Chang Lu, Yih-Peng Chiou, and Tzong-Lin Wu, Novel Crosstalk Modeling for Through-Silicon Vias (TSV) ON 3-D IC: Experimental Validation and Application to Faraday Cago Design, IEEE, 2012.
[5] Jonghyun Cho et al. Active circuit to through silicon via (TSV) noise coupling. In IEEE Electrical Performance of Electronic Packaging and Systems, 2009.
[6] Kihyun Yoon et al. Modeling and analysis of coupling between TSVs, metal, and RDL interconnects in TSV-based 3D IC with silicon interposer. In Proc. IEEE Electronics Packaging Technology Conf., 2009.
[7] B. Curran, I. Ndip, S. Guttovski, and H. Reichl. The impacts of dimensions and return current path geometry on coupling in single-ended Through Silicon Vias. In IEEE Electronic Components and Technology Conference, 2009.
[8] L. Cadix et al. Integration and frequency dependent electrical modeling of Through Silicon Vias (TSV) for high density 3D ICs. In International Interconnect Technology Conference, 2010.
[9] Kim, Joohee, High-frequency Scalable Modeling of a Through Silicon Via (TSV) and Proposal of a Failure Detection Method of 3D ICs, Ph.D Dissertation, KAIST, 2013.

저 자 소 개

Sihyun Lee

1991. 2: Dept. of Electronic Engineering (M.S.), Kon-Kuk University, Seoul, Korea
1998. 2 : Dept. of Electronic Engineering (Ph.D.), Kon-Kuk University, Seoul, Korea
1998. 3-2016. 6 : Up to now, Dept. of Information and Communication Engineering, Dong Seoul University, Seongnam, Gyeonggi, Korea
1991. 1-1995. 12 : Chief Researcher, Hyundai Co. Ltd, Industrial Electronic(Current:SKhynix) R&D Center, Multimedia R&D Center, and Information and Communication R&D Center
2014. 8-2015. 7: Visiting Scholar(Georgia Institute of Technology)

<Research Focus>
3D IC Design Methodology, SoC Design for Low Power and High Speed Processor, SoC Design Methodology with Multiple Core