Journal of The Institute of Electronics and Information Engineers Vol.53, NO.7, July 2016 http://dx.doi.org/10.5573/ieie.2016.53.7.011
ISSN 2287-5026(Print) / ISSN 2288-159X(Online)

논문 2016-53-7-2

이중 필드플레이트 기술을 이용한 4H-SiC 쇼트키 장벽 다이오드

(4H-SiC Schottky Barrier Diode Using Double-Field-Plate Technique)

김 태 완*, 심 슬 기*, 조 두 형*, 김 광 수**

(Taewan Kim, Seulgi Sim, Dooyoung Cho, and Kwangsoo Kim©)

요 약

탄화규소(Silicon Carbide)는 와이드 밴드 갭 물질로써 실리콘(Si)에 비해 고전력, 고주파, 고온 소자용 반도체 물질로서 각광받고 있다. 탄화규소를 이용하여 만든 반도체 소자 중 특히 쇼트키 배리어 다이오드는 현재 가장 많이 사용되는 전력반도체 소자로써 스위칭 속도가 매우 빠르고 낮은 온저항 특성을 가지는 소자이다. 하지만 컨택 엣지에서의 전계집중으로 인해 항복전압이 낮아지는 단점이 있다. 이를 해결하기 위해 다양한 엣지 터미네이션 기술이 제안되고 있는데, 본 논문에서는 최적의 항복전압을 갖기 위한 이중 필드 플레이트(Double Field Plate) 소자 구조를 제안하였다. 측정결과 제작한 소자는 온저항을 유지한 채 38% 향상된 항복전압을 나타내었다. 제안한 소자 특성 검증을 위해 소자를 설계 및 제작한 후 전기적 특성을 측정하였으며, 이중 필드 플레이트 구조는 길이와 두께가 서로 다른 필드 플레이트를 겹쳐 올림으로써 구현하였다.

Abstract

Silicon carbide (SiC) has received significant attention over the past decade because of its high-voltage, high-frequency and high-thermal reliability in devices compared to silicon. Especially, a SiC Schottky barrier diode (SBD) is most often used in low-voltage switching and low on-resistance power applications. However, electric field crowding at the contact edge of SBDs induces early breakdown and limits their performance. To overcome this problem, several edge termination techniques have been proposed. This paper proposes an improvement in the breakdown voltage using a double-field-plate structure in SiC SBDs, and we design, simulate, fabricate, and characterize the proposed structure. The measurement results of the proposed structure, demonstrate that the breakdown voltage can be improved by 38% while maintaining its forward characteristics without any change in the size of the anode contact junction region.

Keywords : 4H-SiC, Schottky barrier diode, Edge Terminations, Breakdown Voltage, On-resistance

* 학생회원, ** 정회원, 서강대학교 전자공학과 (Dept. of Electronic Engineering, Sogang University)
© Corresponding Author (E-mail : kimks@sogang.ac.kr)
※ This research was supported by the KIAT(Korea Institute for the Advancement of Technology), supervised by the MOTIE(Ministry of Trade, Industry and Energy)(N0001594), and the IDEC(IC Design Education Center).
Received ; January 19, 2016 Revised ; June 17, 2016
Accepted ; July 1, 2016

Ⅰ. Introduction

Silicon carbide (SiC) exhibits excellent electrical characteristics in terms of its use in high-power, high-frequency, and high-temperature operations[1~3]. Thus, it is clear that SiC will become the preferred material because of its superiority over silicon. The advantages of SiC over silicon are as follows. First,

its energy bandgap is three times larger, which gives the advantage of an extremely low leakage current. Second, its breakdown field is ten times greater, which allows power devices to withstand stronger high-voltage current. Its higher doping concentration and 1/10 thinner epi-layer provide low on-resistance. In addition, its saturation drift velocity is 2.7 times faster, indicating that SiC devices have low on-resistance in high-field applications[4~6]. For high-voltage Schottky barrier diodes (SBDs), edge termination around an active region is essential to reduce electric field crowding at the diode edge. The Experimentally obtained breakdown voltage of SiC SBDs is considerably lower than the other SiC SBDs when edge termination technic is not applied.

Several edge termination methods for SiC SBDs have been investigated, including field-plate extensions, junction termination extensions, and field rings[7]. This paper proposes the use of a double-field-plate structure. The proposed structure induces an electric field distribution that improves the device's breakdown voltage. To analyze the performance of conventional and proposed structures, we used a device simulator called the Sentaurus TCAD tool suite by Synopsys. Physic models for simulation that were used are barrier tunneling, barrier-lowering and impact ionization model. Impact ionization is an important physic component in measuring the breakdown voltage. The Hatakeyama model is best suited for 4H-SiC.

Ⅱ. Main Subject

1. Device Structure

Figure 1-(a) shows a schematic of a conventional field-plate SBD, Figure 1-(b) shows the proposed structure, and Table 1 lists the parameters of both. The proposed double field plate uses two field plates of different widths, but the overall field-plate thickness is the same; the locations of these two field plates are as follows:

Field plate 1(FP1):

Located just above the substrate

Field plate 2(FP2):

Located on field plate 1 and in contact with the contact edge

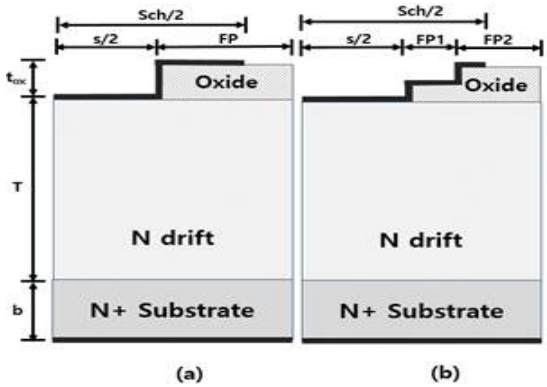

그림 1. (a) 일반적인 필드 플레이트를 갖는 SBD, (b) 이중 필드 플레이트를 갖는 SBD의 단면도

Fig. 1. Cross-section of the (a) conventional field-plate -SBD and (b) double-field-plate SBD.

표 1. 구조 변수

Table 1. Structure parameters.

Name	Symbol	Value
Drift Thickness	a	20um
Schottky Contact	s	250um
Total Oxide Thickness	t_{ox}	6000Å
Substrate Thickness	T	130um
Device Width	w	450um
Field-Plate Width	FP (FP1+FP2)	100um
Schottky Contact Width	Sch	370um

Field plate 1 touches the Schottky contact open edge, and field plate 2 abuts the Schottky contact metal edge. These structures spread electric field crowding by shielding the edge. This causes an increase in the breakdown voltage while maintaining forward characteristics.

2. Fabrication Process

Before deposition of the oxide layer, a cleaning process is carried out in three steps for degreasing and natural oxide removal. For degreasing, we used acetone, TCE, acetone, and methanol for 5 min each in a regular sequence. Then, we used an H_2SO_4: H_2O_2 = 1:1 solution (SPM) for 15 min at room temperature. Lastly, we used a 49% HF solution for 2 min at room temperature to remove natural oxide.

To form the oxide layer, we used the STS PECVD system in ISRC for 20 min to deposit oxide at a 0.6um thickness. Specific patterns were used to achieve different purposes, as follows:

1. pattern 1: classification of each region
2. pattern 2: sorting the field plate 1 layers
3. pattern 3: sorting the contact open layers
4. pattern 4: forming the contact metal layer

Patterns 1, 2, and 3 are used in a regular sequence after oxide deposition (STS PECVD). During patterns 1 and 3, over-etching is carried out for 7 min. To control the thickness of field plate 1, pattern 2 is used for 2 min, 3 min, 5 min, and 7 min each. After the formation of the field plate, the Ni electrode is sputtered at 300Å on top of the wafer. The Ni anode is then patterned with mask pattern 4 and etched to define the anode area. Ni is then deposited again to form the bottom electrode at a thickness of 0.03um on the underside of the wafer. Finally, a Ni alloy process is carried out for the ohmic contacts.

3. Results and Discussion

가. Reverse Characteristics

To analyze the effect of the double field plate, there are two variation points:

1. Field plate 1 width
2. Field plate 1 thickness

These were simulated and analyzed for each structure before fabrication.

(1) Electric field distribution (Simulation result)

To investigate the breakdown voltage (BV) characteristics, we first analyzed the electric field distribution for each condition. Fig. 2 shows the electric field distribution of each condition. And the case of oxide thickness 0.4um of field plate is specified in Fig 3, which shows the electric field distribution.

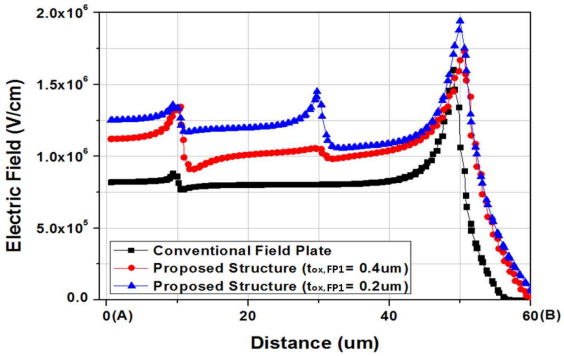

그림 2. 항복전압 상황에서 각 조건에 따른 전계분포
Fig. 2. Electric field distribution of each condition at the breakdown voltage.

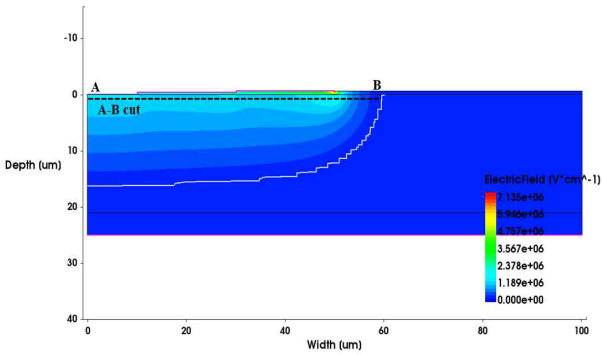

그림 3. FT1의 oxide두께가 0.4um 일 때의 전계분포
Fig. 3. Electric field distribution at the breakdown voltage.

The conventional field plate has two peaks in the electric field—one at the contact open edge (x = 10 um) and another at the contact edge (x = 50 um). The BV of the field plate is generated due to the peak electric field here. Therefore, field-plate thickness and contact length are important parameters. We then compared the effect of the width of field plate 1 (FP1) of the proposed structure with a 20um width. The electric field distribution of the proposed structure was similar to that of a conventional field plate, but at the edge of FP1 we can see an increase once more. FP1 also has peak electric field values at each edge, which increase when the field plate is thinner. As such, thickness is also an important parameter. As the tox,FP1 becomes thinner, the peak electric field value is increased. However, because of the higher BV in the distribution graph of Fig. 2, we can also see those with optimum values.

This data was measured following fabrication.

(2) Measurement results and analysis

The measurement values of the fabricated devices are shown in Fig. 4. These results represent the average results from 24 samples. As demonstrated in the previous section, there is an optimum width and thickness of field plate 1 such that the device achieves the highest breakdown voltage. The reason for the different optimum breakdown voltage levels at varying thicknesses is that the effects on the electric field distribution are not the same in every case. However, an improved breakdown voltage level was observed for samples of every thickness in comparison to that of the conventional field-plate device. These results demonstrate that the double field plate yields the best reverse characteristics at a field plate 1 thickness of 0.18 um and width of 20 um. There was a 38% increase in the breakdown voltage. Specifically, the conventional field-plate structure shows a BV of 810 V and the proposed structure shows a BV of 1120 V.

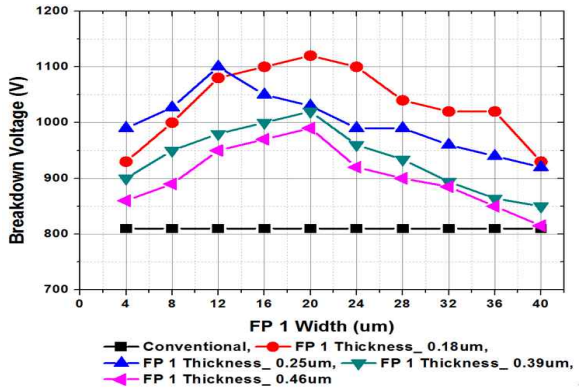

그림 4. FP1 두께를 변수로 한 FP1 너비에 따른 항복전압 분포

Fig. 4. Breakdown voltage distribution of each conditions.

Fig. 5 shows the simulation and measurement results, which were extracted for a field plate 1 thickness of 0.46um. The analysis results indicate that the tendency of the overall breakdown voltage is similar, but the breakdown voltage of measurement result is about 10% lowered compare to that of simulation result.

There are two possible reasons for the reduction in these breakdown voltages. First, a breakdown can occur when the PECVD oxide quality is not good. Secondly, substrate defects can incur current crowding, which can induce an increase in the electric field, which can then lead to breakdown. To solve these problems, we can use either low- or no-defect wafers. In addition, using an oxide growth process rather than PECVD or a proper passivation process will realize a better oxide layer.

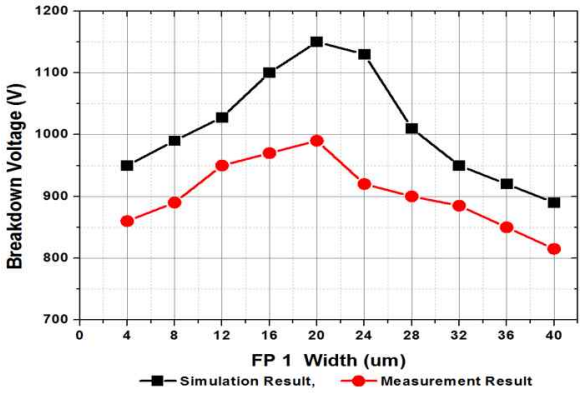

그림 5. FP1의 너비 변화에 따른 시뮬레이션 값과 측정값의 역방향 특성 비교

Fig. 5. Comparison of simulation and measurement results for the reverse characteristics of the double-field-plate SBD (FP1 thickness 0.46 um).

Fig. 6 shows the reverse I-V curves from the measurement and simulation results when width of FP1 is 20um and FP1 thickness is 0.46um. To analyze the characteristics of the fabricated device, we defined the reverse leakage current of SBDs as follows:.

$$J_L = A T^2 \exp\left(-\frac{q\Phi_b}{kT}\right) \quad (1)$$

Value A is Richardson's constant. In the case of 4H-SiC, the Richardson's constant is $146 A^0 K^{-2} cm^{-2}$. Leakage current is dependent on the height of schottky barrier and temperature. Then the leakage current is calculated to $3.34 \times 10^{-9} A/cm^2$. This value indicates that the value of measurement and simulation have same tendency. From the result of the measurement, the leakage current increases gradually. It is the effect of the barrier lowering, the schottky barrier decreases with the increase of the cathode voltage.

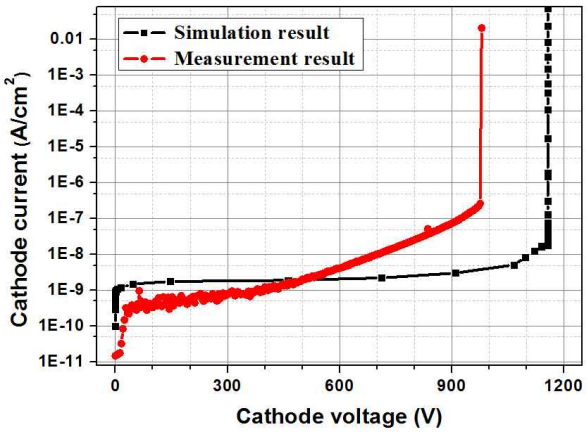

그림 6. FP1의 너비가 20um일 때 역방향 I-V특성
Fig. 6. Reverse I-V characteristic(FP1 width 20um, FP1 oxide thickness 0.46 um).

나. Forward Characteristics

To analyze the characteristics of the fabricated device, we defined the on-state voltage drop of SBDs as follows:.

$$V_f = \frac{kT}{q} ln\left(\frac{J_F}{J_S}\right) + (R_{drift} + R) \quad (2)$$

The forward current density J_F is related to Φ_b, as follows:

$$J_S = A T^2 \exp\left(-\frac{q\Phi_b}{kT}\right) \quad (3)$$

To analyze the forward characteristics, we considered on-resistance as a parameter. The specific on-resistance of the drift region is given by:

$$R_{on} \approx \rho_{epi} t_{epi} = \frac{t_{epi}}{q\mu_n N_D} = \frac{4V_B^2}{q\mu_n N_D} = \frac{4V_B^2}{\mu_n \varepsilon_s E_{CR}^3} \quad (4)$$

In this research, Ni is used as the Schottky contact metal. The V_F, R_{on} values can then be calculated as 1.74 V and 0.36 mΩ · cm^2, respectively, based on the known parameters of Ni[8].

Fig. 7 shows the I-V curves from the measurement and simulation results, which represent the average results from 24 fabricated device samples. The measured V_F, R_{on} values were 1.8 V and 0.42 mΩ · cm^2, respectively, which represent an increase of 3.45%, 16%. This difference can be explained by two factors. First, the intrinsic resistance of Ni may affect the on-resistance measurement results. Secondly, substrate defects can increase on-resistance, thus causing a drop in the on-state voltage. To reduce these effects, we suggest using a no-defect wafer or an alternate Schottky metal in which the resistance is low.

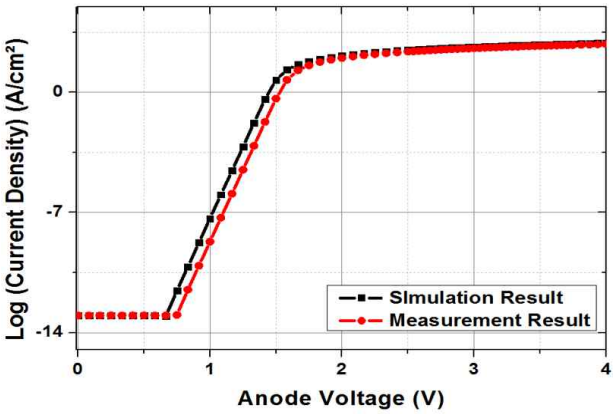

그림 7. 애노드 전압에 따른 시뮬레이션 값과 측정값의 순방향 특성 비교
Fig. 7. Comparison of forward characteristics of the simulated and fabricated double-field-plate SBDs.

Ⅲ. Conclusion

In this paper, we improved the breakdown voltage of the SiC SBD with a proposed double-field-plate structure, which we designed, simulated, fabricated, and characterized. The proposed structure consists of two field plates while maintaining the same overall thickness. The two field plates have different thicknesses and widths to distribute the electric field. Using this structure, we can improve the breakdown voltage while maintaining the forward characteristics, because the anode contact junction region remains unchanged.

The proposed structure was fabricated with a wafer from Cree Inc. and was processed in ISRC. The measured V_F, R_{on} values were 1.8 V, 0.42 mΩ · cm^2, respectively, which represent an increase of 3.45%, 16% over the simulation results. The best field

plate 1 parameters with respect to the reverse characteristics are a thickness of 0.18 um and a width of 20 um. In this condition, the breakdown voltage of the conventional field-plate structure is 810 V and that of the double field plate is 1120 V, which represents a 38% increase.

With this edge termination technique, it is possible to develop a high doping concentration in the substrate while retaining the same breakdown voltage. As such, this technique can be applied to devices that are smaller in size and increases the availability of Schottky barrier diodes for low on-resistance and high voltage applications.

REFERENCES

[1] Rohm, SiC Power Devices and Modules, Ukyo, Tokyo, 2013.

[2] S. Dimitrijev and P. Jamet, “Advances in SiC power MOSFET technology”, Microelectron. Reliab., vol. 43(2), pp. 225-233, 2003.

[3] T. P. Chow, N. Ramungul, and M. Ghezzo, “Wide bandgap adsemiconductor power devices”, in Proc. Power Semiconductor Materials and Devices Symposium, Mater. Res. Soc., S. J. Pearton, R. J. Shul, E.Wolfgang, F. Ren, and S. Tenconi, Eds., 1997, pp. 89-102

[4] M. Marinella, “The Silicon Carbide MOS Capacitor”, Saarbrucken, Germany: *VDM Publishing*, pp. 3-22, 2008.

[5] M. Bhatnagar and B. J. Baliga, “Comparison of 6H-SiC, 3C-SiC, and Si for power devices”, IEEE Trans. Electron Devices, vol. 40, pp. 645-655 , 1993.

[6] J. W. Palmour and L. A. Lipkin, “High-temperature power devices in silicon carbide”, in Trans. 2nd Int. High Temp. Elec. Conf., vol. 1, pp. (XI-3)-(XI-8), 1994.

[7] B. J. Baliga, “Fundamentals of Power Semiconductor Devices”, NY, USA: Springer, pp. 91-166, 2010.

[8] B. J. Baliga, “Silicon Carbide Power Devices”, NY, USA: World Scientific, pp. 83-96, 2005.

저 자 소 개

김 태 완(학생회원)

2015년 충남대학교 전자공학과 학사 졸업

2015년～현재 서강대학교 전자공학과 석사과정

<주관심분야: 전력반도체소자, SiC Schottky barrier diode, Super-junction MOSFET>

심 슬 기(학생회원)

2014년 서강대학교 전자공학과 학사 졸업

2016년 서강대학교 전자공학과 석사 졸업

<주관심분야: 전력반도체소자, SiC Schottky barrier diode>

조 두 형(학생회원)

2011년 단국대학교 전기전자공학과 학사 졸업

2013년 서강대학교 전자공학과 석사 졸업

2013년～현재 서강대학교 전자공학과 박사과정

<주관심분야: 전력반도체소자, SiC Schottky barrier diode, SiC MOSFET,>

김 광 수(정회원)

1981년 서강대학교 전자공학과 학사 졸업

1983년 서강대학교 전자공학과 석사 졸업

1998년 서강대학교 전자공학과 박사 졸업

1983년～1997년 한국전자통신연구원 책임연구원

1998년～2005년 정보통신연구진흥원 책임연구원

2005년～2008년 대구경북과학기술원 책임연구원

2008년～현재 서강대학교 전자공학과 교수

<주관심분야: 전력반도체소자, SiC Schottky barrier diode, Super-junction MOSFET, SiC MOSFET>