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An Energy-Efficient Matching Accelerator Using Matching Prediction for Mobile Object Recognition

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***Abstract*—An energy-efficient object matching accelerator is proposed for mobile object recognition based on matching prediction scheme. Conventionally, vocabulary tree has been used to save the external memory bandwidth in object matching process but involved massive internal memory transactions to examine each object in a database. In this paper, a novel object matching accelerator is proposed based on matching predictions to reduce unnecessary internal memory transactions by mitigating non-target object examinations, thereby improving the energy-efficiency. Experimental results show a 26% reduction in power-delay product compared to the prior art.**

***Index Terms*—Object recognition, object matching, vocabulary tree, matching prediction, matching accelerator**

I. INTRODUCTION

Recently, object recognition becomes wide spread in mobile multimedia applications and plays a key role in augmented reality and autonomous robots [1]. Object matching is one of the major parts in this object recognition process [1] and selects the closest item with input object from the object database (DB). It involves massive accesses to external memory containing the DB [1], and therefore, energy efficient design of this object matching is of the most importance in mobile vision applications [2]. A variety of object matching algorithms have been studied, and recently, the vocabulary tree (VT) is gaining attentions for its efficient use of external memory bandwidth [3, 4]. However, its energy dissipation is still demanding as it involves considerable transactions to internal memory. In this paper, we propose a novel object matching accelerator based on our proposed matching prediction scheme to reduce its internal memory transactions triggered by the investigations on non-target objects. The proposed matching prediction scheme exploits the temporal coherence of consecutive image frames. Therefore, we can match the input object by utilizing the previous matching result, which is based on the similarity between consecutive frames. As a result, our object matching accelerator shows 26% improvement in power-delay product (PDP) from the previous art [4].

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II. MATCHING PREDICTION SCHEME

One of the most challenging issues in object matching is its huge external memory bandwidth required in accessing object DB [1]. Vocabulary tree (VT) is well known for its efficient use of memory bandwidth by quantizing the key points of objects in the DB, which makes the entire DB fit in the on-chip memory [1, 4]. However, the VT-based object matching incurs considerable transactions to internal memory as it compares input object with the entire DB. Therefore, we present a matching prediction scheme to find the target object without going through the entire DB by exploiting the temporal coherence associated with consecutive frames. Our scheme matches the input object if it is close enough to the object from previous frame. In this way,

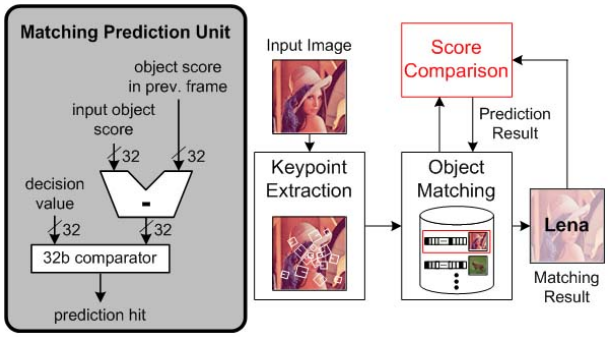


Fig. 1. The proposed matching prediction scheme (a) Block diagram, (b) Flow diagram.

Table 1. Misprediction rates for ukbench dataset [4]

Object Categories	Size of Dataset	Misprediction rate (%)
Doll	220	1.7
Fruit	60	2.9
Kitchen Supplies	52	1.9
Book	980	3.5
Office Supplies	36	3.2

we can reduce the internal memory transactions significantly by removing the examinations to non-target objects.

Fig. 1(a) shows the proposed matching prediction unit. In the VT framework, each object in the DB is scored based on its difference with input object. In this architecture, the prediction gets hit when the scores of the input object and the matched one from previous frame are close enough, as shown in Fig. 1(b). In the hit case, input object is matched using the previous matching result without examining the non-target objects. On the other hand, when the prediction does not get hit, input object is scored by going through the entire DB. Scoring of the input object is carried out periodically for the entire DB as the false matching can arise repeatedly when a misprediction happens. We set the period to 15 frames as the false matching for such a short term is unnoticeable to human visual system. The misprediction rate of this matching prediction scheme is as low as 2.6% as shown in Table 1, thus input object can be matched with a very high accuracy without scoring the non-target objects in the DB. Therefore, the proposed matching prediction scheme reduces internal memory transactions by 65.9% compared to the conventional object matching strategy.

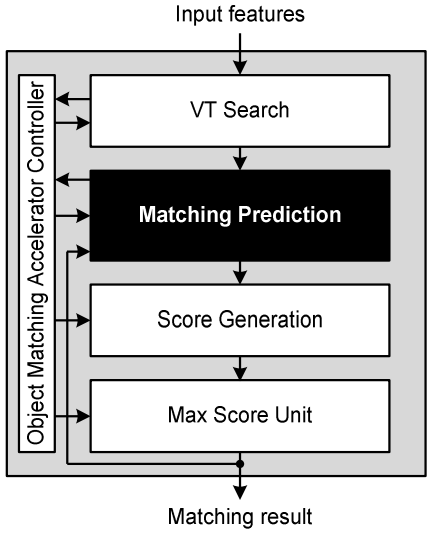
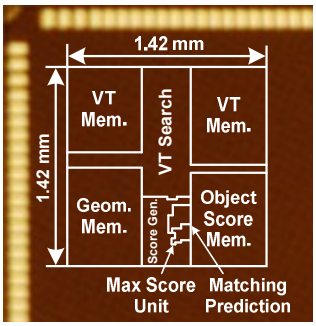


Fig. 2. Overall block diagram of the proposed object matching accelerator.

The overall architecture of the proposed object matching accelerator is illustrated in Fig. 2. It consists of four major components; VT search, matching prediction, score generation, and max score unit. The VT search unit finds several matching candidates with the smallest distance to the input, and then the score generation unit scores these matching candidates compared to the input based on their geometry information such as coordinates and orientation. Finally, the max score unit chooses the object with the highest score as the final matching result. The proposed prediction unit is placed between the VT search and score generation unit and gates the score generation of non-target objects to reduce on-chip bandwidth based on the prediction result.

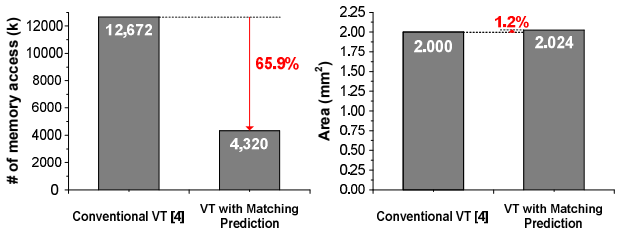
III. Experimental Results

The proposed object matching accelerator exploiting the matching prediction scheme is fabricated using 65 nm CMOS process. A die photograph and chip characteristics are described in Fig. 3. The experimental results demonstrate 6.8 mW average power and 6.7 ns critical path delay. The proposed prediction scheme reduces internal memory transactions by 65.9% at a 1.2% increase in area compared to conventional object matching scheme, as illustrated in Fig. 4. Table 2 presents the PDP comparison to the state-of-the-art object matching accelerator. The proposed object



Technology	65 nm CMOS
Area	2.024 mm^2
Supply Voltage	1.2 V
Operating Frequency	150 MHz
Power Consumption	6.8 mW

Fig. 3. Die photograph and chip characteristics.



(a) (b)

Fig. 4. Memory access and area comparison in score generation stage (a) Memory access comparison, (b) Area comparison.

Table 2. Comparison with previous work

	Conventional VT [4]	VT with Matching Prediction
Technology (nm)	65	65
Supply Voltage (V)	1.2	1.2
Frame Rate (fps)	30	30
Power (mW)	9.2	6.8
Delay (ns)	6.7	6.7
Area (mm^2)	2.000	2.024
PDP (pJ)	61.6	45.6

matching accelerator achieves a 26% reduction in PDP from the prior art [4].

IV. Conclusions

A novel object matching accelerator exploiting matching prediction is presented for mobile object recognition applications. The proposed object matching accelerator demonstrates a 26% reduction in PDP from state-of-the art.

Acknowledgments

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