JOURNAL OF SEMICONDUCTOR TECHNOLOGY AND SCIENCE, VOL.16, NO.2, APRIL, 2016
http://dx.doi.org/10.5573/JSTS.2016.16.2.226
ISSN(Print) 1598-1657
ISSN(Online) 2233-4866

Efficient Pre-Bond Testing of TSV Defects Based on IEEE std. 1500 Wrapper Cells

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***Abstract*—The yield of 3D stacked IC manufacturing improves with the pre-bond integrity testing of through silicon vias (TSVs). In this paper, an efficient pre-bond test method is presented based on IEEE std. 1500, which can precisely diagnose any happening of TSV defects. The IEEE std. 1500 wrapper cells are augmented for the proposed method. The pre-bond TSV test can be performed by adjusting the driving strength of TSV drivers and the test clock frequency. The experimental results show the advantages of the proposed approach.**

***Index Terms*—TSV defect, IEEE std. 1500 wrapper cell, load capacitance, delay test, pre-bond test**

I. INTRODUCTION

The 3-dimentional stacked integrated circuit (3D SIC) based on through silicon via (TSV) improves silicon area, power consumption, speed and form factor. However, the fabrication process of TSV occasionally causes defects related to their conductor and insulator, e.g., voids and pin-holes [1-3] A void increases the resistance of the corresponding TSV and a pin-hole reduces the resistance between the corresponding TSV and the substrate [3-5]. These defects cause variations in the resistance and equivalent capacitance of TSVs those can be modeled as a propagation delay fault [4].

To increase the yield of 3D SIC fabrication, each die is equipped with pre-bond test infrastructure through which a die is sorted as known good die (KGD) [6, 7]. After stacking process some defects on the bumper connecting KGDs are tested through a mid-bond or post-bond test [8, 9].

Ample research has been published to perform detecting TSV defects at pre-bond test stage. Po-Yuan et al. [2] have presented a novel pre-bond testing scheme for TSVs, which is based on sense amplification technique that is commonly seen in DRAM. This scheme can test TSVs at the wafer level and the faulty TSVs can be identified before bonding. The work in [3] proposed a TSV pin-hole detection method by exploring four analog test circuits; however, it can only detect a leakage current through PMOS or NMOS by determining the resistance between the TSV and the substrate. Deutsch et al. [4] have proposed a method using ring oscillators, which considers TSVs as their load to detect the TSV defects. Its precision can be improved by applying various voltage levels. However, since it tests TSVs in a group, it impedes the diagnosis process and requires additional control signals for managing a group of TSVs.

The above-mentioned work requires customized circuitry for implementation. However, the basic principle for detecting TSV defects is based on the propagation time of a transition through TSVs.

TSV defects depend on the fabrication processes, which may render different defects. The information related to these process dependent defects is very confidential and cannot be shared among system designers. Thus, without knowing the reasons of these defects, implementation of an efficient test method at system design level is forbidden. However, even these reasons are known, integration of a test method at the system design level may increase the design time.

Manuscript received Jun. 30, 2015; accepted Nov. 10, 2015
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Moreover, the manufacturers can wrap the die with IEEE std. 1500 wrapper, as in [7], that allows further modifications according to certain process dependent faults. This flexibility at the manufacturing level is viable even though the functional registers that are connected to TSVs cannot be shared with boundary wrapper cells.

Since the resistance and capacitance corresponding to a TSV are very small, a high precision testing method is required. However, the existing at-speed tests with conventional wrapper cells cannot detect small changes in the capacitance and resistance values of TSVs, especially at the pre-bond test stage. In this paper, a conventional IEEE std. 1500 wrapper cell is augmented with a controlled driver to test TSV defects. The proposed method has been verified to be able to improve the detecting efficiency during the pre-bond test. The main contributions of this paper are as follows:

1) Modifications in IEEE std. 1500 wrapper cells are proposed for precise diagnosis of individual TSV,
2) The testing accuracy is enhanced by adjusting the driving strength of TSV driver and the test clock frequency.
3) The experimental results show an improved detecting efficiency with significant test time reduction as compared to the previous work.

The remainder of this paper is organized as follows. The background of this work is presented in Section 0. Section 0 presents the proposed modification in IEEE std. 1500 wrapper cells and a novel TSV test method. The experimental setup and experimental results are presented in Sections 0 and 0, respectively. The conclusion of this work follows in Section 0.

II. BACKGROUND

1. Electrical Model of a TSV

In a 3D SIC, the resistance and capacitance of a cylindrical shaped TSV can be estimated using the following equations [10-13]:

$$R = \frac{4\rho_{Cu} l}{\pi(d-2t)^2} \quad (1)$$

$$C = \frac{2\pi\varepsilon_{SiO_2} l}{\ln(\frac{d}{d-2t})} \quad (2)$$

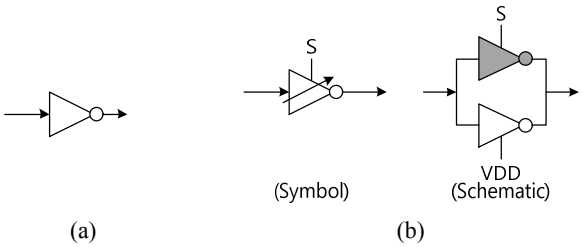


Fig. 1. TSV driver (a) standard, (b) tunable [11, 15, 16].

wherein, *l, d* and *t* represent the length, diameter and insulator thickness of a TSV, respectively. In (1), ρ_{Cu} is the resistivity constant of copper and in (2), ε_{SiO2} is the dielectric constant. Eq. (2) shows that a longer length and wider diameter of a TSV would result in higher capacitance, which slows the transition.

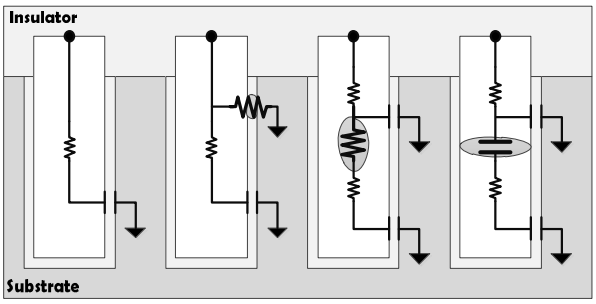
A TSV can be either output, input or both (input-output) of a die. In this paper, for simplicity, the terms tx-TSV and rx-TSV are used to stand for output or transmit-TSV and input or receive-TSV, respectively. These TSVs are connected with the output and input wrapper cells of the IEEE std. 1500. The bidirectional TSV is connected with the bidirectional wrapper cell, which is comprised of input, output and control wrapper cells [14]. The bidirectional cell is not discussed separately in this paper because it can be easily modified according to the proposed test technique.

In order to drive a signal through a TSV at higher frequencies, a driver (buffer/inverter) is required. As a functional requirement, the tx-TSVs are equipped with a driver but the rx-TSVs are not. Thus, a test-dedicated driver is required for an rx-TSV [4].

The driver of a tx-TSV can be reused while testing it and the driving strength can be tuned by the tunable driver [11, 15, 16], as shown in Fig. 1. The tunable driver's driving strength can be controlled by a signal "S" to select a desired driver strength. To avoid timing penalty, both drivers should be active in normal mode.

2. TSV Fault Models

There are three TSV defects: pin-hole, void and open [1-4] and can be modelled using resistive and capacitive components, as shown in Fig. 2. In a pin-hole defect, the insulation between the TSV and substrate is opened, which causes leakage. The void in a TSV increases resistance at the defect location and the open defect



(a) No defect (b) Pin-hole (c) Void (d) Open

Fig. 2. TSV fault models [1-4].

causes a physical disconnection between two extremes of a TSV. At pre-bond test stage, both extremes cannot be sensed unless physical probing is performed. However, the probing may damage the surface of a TSV because it is fragile to physical touch. Noia et al. [17] have presented a method to enable physically touch on a group of TSVs. This method cannot locate the faulty TSV unless the physical probing is performed multiple times, which may consequently damage the surface of bumps. Therefore, without probing the opened terminal of TSV, it can be controlled and observed through the circuitry that is connected to its dipped terminal.

The defect detection techniques for a TSV through its single terminal are different from that through both terminals. The characteristics of TSV defects for pre-bond testing with a single terminal are summarized in Table 1. Depending on the fault type, either charging or discharging, or even both transitions are required for TSV testing.

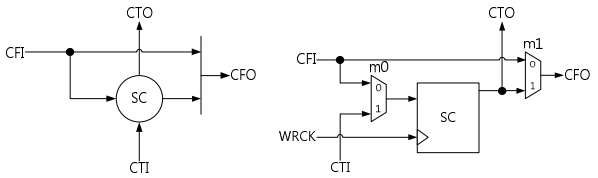
3. IEEE Std. 1500 Wrapper Cells

There are several types of IEEE std. 1500 wrapper cells [18, 19], which include a shift path to load and unload the test data. Input wrapper cells capture and unload data through the shift path, and output wrapper cells update the data shifted in and drive the data towards the output of the wrapper cell. Fig. 3 shows the bubble diagram and schematic of a basic wrapper cell with a single flip-flop [20, 21].

In this paper, the proposed modifications in the basic wrapper cell design are detailed; however, the key concepts of modifying other wrapper cells are briefly described. The proposed modifications in the wrapper cells preserve the compatibility with the IEEE std. 1500,

Table 1. The effects of TSV defects on charging and discharging time during pre-bond testing through its single terminal

	Insulator Defect	Conductor Defects	
	Pin-hole	Void	Open
Charging time	Increase	Decrease	Decrease
Discharging time	Decrease	Decrease	Decrease



(a) (b)

Fig. 3. IEEE std. 1500 basic wrapper cell (WC_SD1_CII) (a) bubble diagram, (b) schematic [18-21].

which allows adopting conventional test techniques.

III. PROPOSED TEST TECHNIQUE

1. Proposed Test Method

The variations in the resistance and/or capacitance of a TSV are caused by its defects. These defects can be detected by observing the effect of a fast transition (between 0 and 1) at a terminal of TSV. A fast transition can be produced by applying two consecutive cycles of a high frequency clock after shifting the stimuli into the wrapper cells.

Fig. 4 shows an inter-die signal path between two different logics, which passes through the corresponding wrapper cell and a TSV. For the post-bond TSV delay test, the system clock can be used in a similar way as it is used for the conventional intra-die at-speed test. However, for pre-bond TSV delay test, the path is shortened (i.e., only one wrapper cell and a TSV), as shown in Fig. 5. Therefore, a faster clock than the system clock is required.

Since the upper bound for generating a faster clock is technology-dependent, this work aims to decrease the driving strength of the drive buffer by using a tunable driver. The tunable driver allows reducing the required test clock frequency for testing a TSV without incurring a charging timing penalty.

The wrapper cells of IEEE std. 1500 require modifications to implement the proposed test scheme.

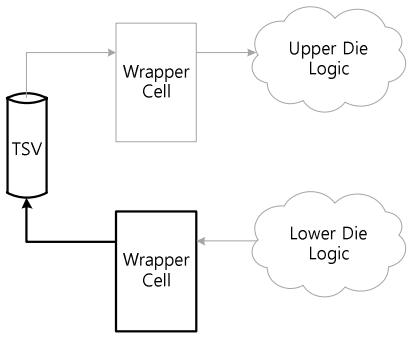


Fig. 4. A signal path between two inter-die logic blocks and a TSV delay test path (bold line).

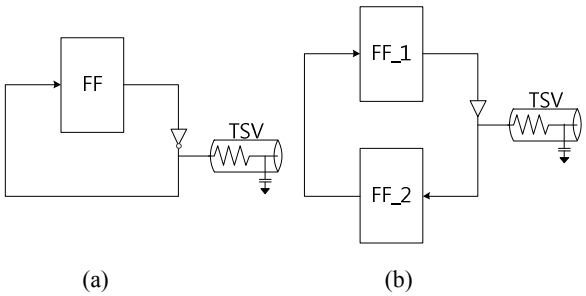


Fig. 5. Simplified TSV delay test models with IEEE std. (a) basic wrapper cell, (b) other wrapper cells.

The modifications depend on the number of storage elements in the wrapper cell and the type of TSV (i.e., tx- or rx-TSV).

2. TSV Test via IEEE std. 1500 Wrapper Cell

The IEEE std. 1500 defines many types of wrapper cells, which have one or more storage elements. For the wrapper cells that have more than one storage elements, two storage elements can be used to launch and capture a signal, as shown in Fig. 5(b). However, for a wrapper cell with a single storage element, it is proposed to embed an inverter to produce a transition for fault detection, as shown in Fig. 5(a). The proposed wrapper cell modification preserves the compatibility with their actual functions.

To perform pre-bond test for a TSV, the test vector is launched at a TSV terminal and is captured from the same terminal, as shown in Fig. 6(a) and (b). In both cases, the tx-TSV is connected to the CFO port of the wrapper cell and the rx-TSV is connected to the CFI port, and the TSV stimulus signal goes through a driver. The driver can be reused in case of a tx-TSV but for an rx-

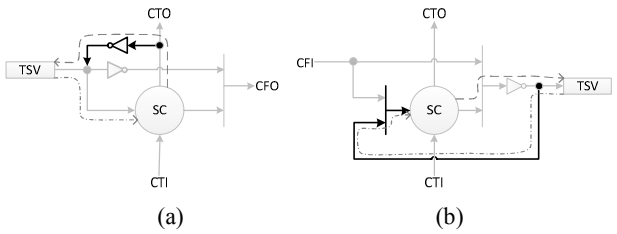


Fig. 6. The bubble diagrams of the modified basic wrapper cells for TSV testing (a) input TSV wrapper cell, (b) output TSV wrapper cell.

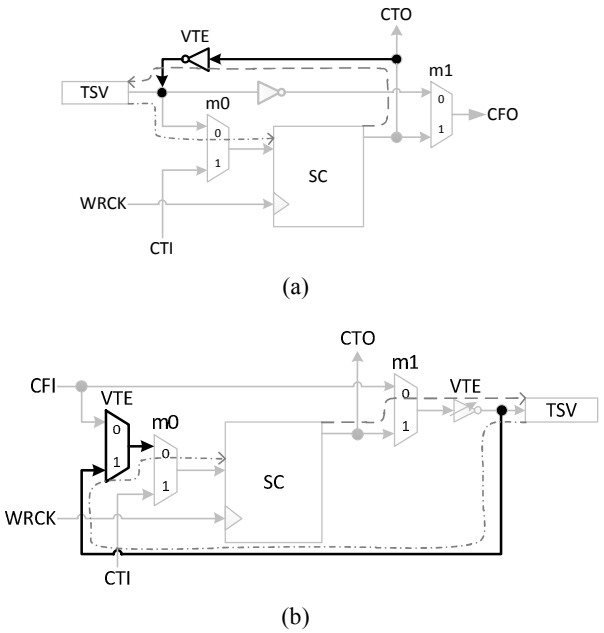


Fig. 7. The schematics of modified basic wrapper cells for TSV testing (a) input TSV wrapper cell, (b) output TSV wrapper cell.

TSV, a test-dedicated driver needs to be embedded.

In order to test a TSV, both the launch path and the capture path are needed. However, as the standard basic cell only provides either of the two paths, the other path needs to be added. In particular, as the tx-TSV and rx-TSV have different connections with the wrapper cell, different modifications are proposed for both cases. Fig. 6(a) and (b) highlight the proposed modifications in a basic wrapper cells for both the rx-TSV and tx-TSV, respectively. The bold path depicts the proposed modification, which feeds the output of the storage element back to its input. At this feedback path, it is proposed to attach the TSV-under-test in parallel. In Fig. 6 and 7, the dashed and chained lines show the driving and capturing paths, respectively. Usually, an inverter is used as a driver for tx-TSVs [11, 13, 15, 22], thus it is

Table 2. A Guideline for Modifying the Wrapper cells with more than one storage elements

1.	Select a flip-flop (*F0*), which is connected to *CTI* port;
2.	Select a flip-flop (*F1*), which is connected to *CFO* port;
3.	**IF** (input wrapper cell) **{**
4.	*CFI* = *VTE* **?** *F1* **:** high-z;
	// The output of *F1* is connected to the *CFI* port
	// through a tri-state buffer (or inverter)
5.	*F0* = *SHIFT* **?** *CTI* **:** (*VTE* **?** *CFI* **:** …); **}**
	// Either *CFI* or *CTI* value is stored to *F0*
	// if (*SHIFT*, *VTE*) = (1, X) then *F0* = *CTI*
	// else if (*SHIFT*, *VTE*) = (0, 1) then *F0* = *CFI*
6.	**ELSE IF** (output wrapper cell) **{**
7.	*CFO* = *VTE* **?** (weak) *F1* **:** (strong) *F1*;
	// The output of *F1* is connected to *CFO*
	// through a tunable buffer (or inverter)
8.	*F0* = *SHIFT* **?** *CTI* **:** (*VTE* **?** *CFO* **:** …); **}**
	// Either *CTI* or *CFO* value is stored in *F0*
	// if (*SHIFT*, *VTE*) = (1, X) then *F0*=*CTI*
	// else if (*SHIFT*, *VTE*) = (0, 1) then *F0*=*CFO*

reused for testing a tx-TSV.

Fig. 7 shows the schematic of the proposed basic wrapper cells. The via test enable (VTE) signal controls the TSV test. The test patterns for generating the charging and discharging transitions are 1 and 0, respectively. The value of SC is applied at the launch cycle, which goes through the inverter back to the SC. Subsequently, the capture cycle captures the output of the inverter. In case the charging/discharging time of a defective TSV is changed, it can be observed by capturing operation at specific speed of clock frequency.

For example, if the TSV-under-test has pin-hole defect then its charging time is increased. The test vector, '1', is shifted into the wrapper cell, which is then inverted back to its input. Two consecutive cycles of the fast clock are applied at WRCK. At the first cycle, '0' is stored into SC, which is traversed through the feedback path. The value of SC, i.e., '0', again follows the feedback path, however, due to a higher charging time caused by the defective TSV, the inverted value will not be captured at the second cycle of the fast clock. Similarly, all other types of wrapper cells that have more than one flip-flop can be augmented for the proposed testing scheme, as advised in Table 2.

3. Test Sequence for TSV Defects

We adopt the delay test technique with two consecutive fast clock cycles to test TSVs [23]. A new instruction, "TSV_TEST", is decoded to assert the VTE signal. The pre-bond test is performed according to Table 3, which is fully compatible with the IEEE std. 1500. Two test patterns are needed to test the TSV faults those disturb the charging and discharging time of a TSV. This method concurrently tests multiple TSVs after the initial pattern is loaded into the wrapper cells through serial wrapper scan chains; thus, this method results in a fast test time.

Table 3. The test sequence for TSV delay test

1.	LOAD "*TSV_TEST*" instruction;
	// VTE = '1' from instruction decoder
2.	LOAD the test patterns for charging sequence;
3.	APPLY two fast clock cycles;
4.	UNLOAD the results and LOAD test patterns for discharging sequence;
5.	APPLY two fast clock cycles;
6.	UNLOAD the results

Although, the TSV defects result in a variation in charging and discharging time [16], for simplicity, this paper only demonstrates the detection of the faults those slow down the charging time. However, it can also be used for testing the defects that decrease the charging and discharging time.

There is an acceptable time interval to capture a transition [2] for a fault-free TSV between t_L and t_H. At these two time intervals, the test must be performed to check for the occurrence of the desired transitions.

IV. EXPERIMENTAL SETUP

For HSPICE simulations, a 50-nm technology BSIM4 library with the Electric waveform viewer tool is used. The following assumptions are made for the experiments. The length (l), diameter (d) and the SiO_2 insulator thickness (t) depend on the TSV technology; current studies report the following values: 30 μm, 2 μm and 120 nm, respectively [24]. According to (1) and (2), the resistance (R) and capacitance (C) are calculated as 207 mΩ and 50.9 fF, respectively. A 1.14 GHz test clock frequency and a driver with x2 driving strength are used. To build an x2 driver, the selected length/width of the NMOS and PMOS transistors are 50 nm/100 nm and 50 nm/200 nm, respectively. The test clock frequencies capable of detecting the TSV delay defects according to different driving strengths are shown in Table 4. Since higher frequencies may cause timing problems, lower driving strength with slower test clock frequency is

Table 4. Test clock Frequencies at different driving strengths with charging transition

Driving Strength	Length/Width (nm/nm)		Test Clock Freq. (MHz)
	PMOS	NMOS	
(Std.)x1	50/100	50/50	400
x2	50/200	50/100	1,140
x4	50/400	50/200	1,850
x8	50/800	50/400	2,650
x16	50/1,600	50/800	3,250

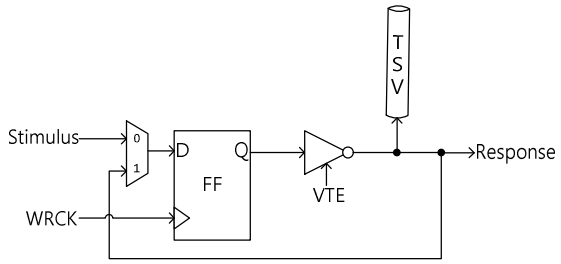


Fig. 8. The schematic for TSV delay test simulation.

preferred. However, these values depend on the process technology, and additionally depend on the type of wrapper cell because the load on the launch and capture path may vary among different wrapper cell types. Thus, the test engineers may choose an appropriate test clock frequency for the TSV test by considering these factors.

V. EXPERIMENTAL RESULTS

Fig. 8 shows HSPICE simulation model for TSV test with the proposed method. For the TSV capacitances of 50-70 fF, the test data for the input of FF are applied at every positive edge of WRCK clock, which is driven by the system clock. The simulation results in Fig. 9 show the captured data at FF for TSV capacitance of 50, 55, 60, 65 and 70 fF with a test clock frequency of 1.14 GHz. It can be observed from Fig. 9 that for a 50 fF TSV load capacitance, the transition can be captured at FF. However, it cannot be captured for TSV capacitances of 55-70 fF, which reflect the defect detection.

In a CMOS design, different driving strengths result in different charging times, as illustrated in Fig. 10. A capacitance of 50 fF, a resistance of 200 mΩ and a range of driving strengths (given in Table 4) were selected. In accordance with the expectation, the driver of x16 strength charged the TSV capacitance at the earliest time and the charging time slows down with a weaker driving strength.

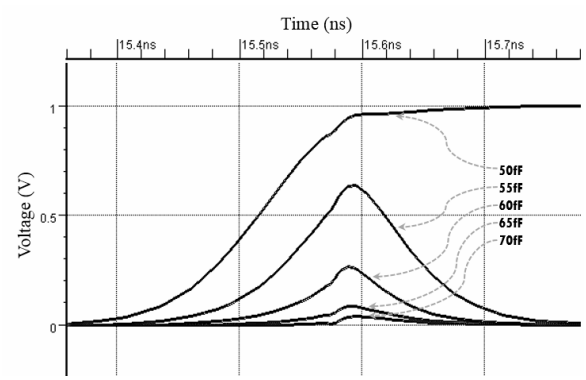


Fig. 9. The voltage with different capacitances at 1.14 GHz clock frequency.

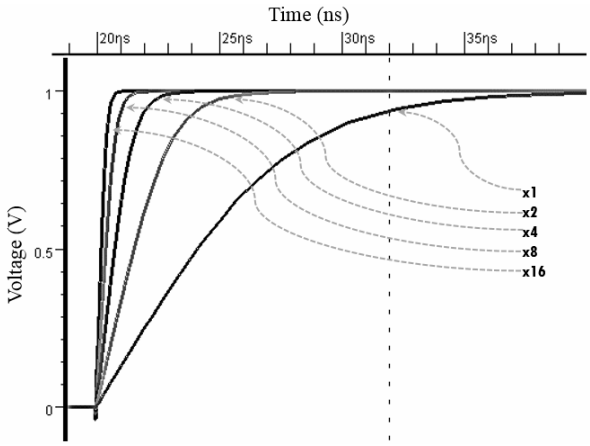


Fig. 10. Charging times with different driving strength.

We performed Monte Carlo (MC) simulations to show the robustness of the proposed method with respect to process variations. The factors affecting the delay in a circuit are the threshold voltage (V_{th}) variation (during CMOS fabrication), power supply (V_{DD}) variation (during test stages at the wrapper cell), wear-out time and temperature. Since the proposed method only considers the pre-packaging stage, wear-out can be ignored and the temperature can be controlled. Therefore, only V_{th} and V_{DD} are dealt with in these simulations, which show the effects of these parameters through the test results.

For simulations, the following example values were used. According to recent studies [25, 26], the variation in V_{th} is approximately 7% ~ 8% and the variation in V_{DD} is between -10% ~ +10%. A similar V_{DD} variation is observed in the wrapper cell components that are geometrically close to each other. However, in the same case V_{th} may vary significantly [25, 26] because different fabrication-changes affect the transistors in different

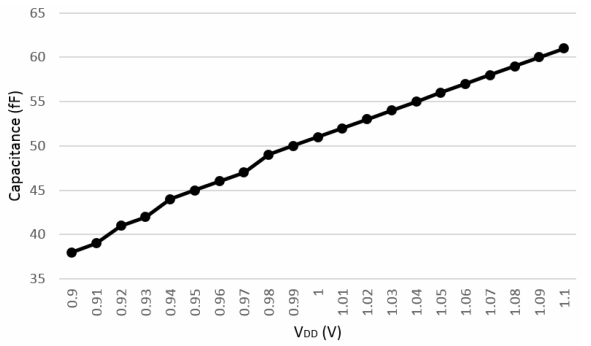


Fig. 11. MC simulation results for power supply variation.

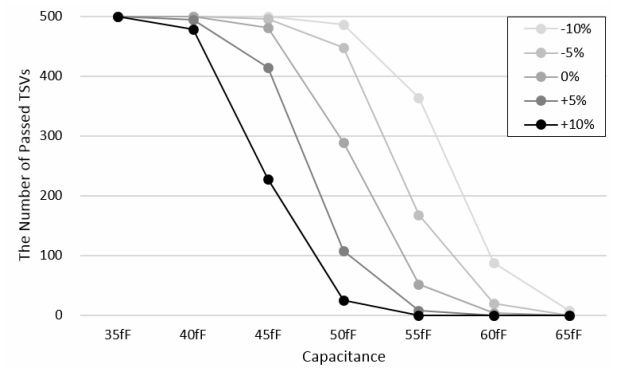


Fig. 12. MC simulation results for threshold voltage variation.

ways. Therefore, for the following simulations, the same V_{DD} variation value is used among all transistors, whereas different V_{th} variations are used, as in the probability model given in [25, 26].

Fig. 11 shows the results of the power supply variation. The x-axis indicates the values of V_{DD} ranging from 0.9V to 1.1V and the y-axis represents the acceptable capacitance that can pass through the proposed test scheme under the corresponding V_{DD}. In brief, a lower V_{DD} increases the charging/discharging time and causes a timing delay, and vice versa. In addition, the "false negative" for a low V_{DD} and a "false positive" for a high V_{DD} should also be taken into account during system design level.

Since a TSV is a load on a driver, the V_{th} variations in the driver transistors have more influence on the testing results than the V_{th} variation in the wrapper cell transistors. Therefore, for simulations, the V_{th} variations in the wrapper cell transistors are applied according to the probability model [25, 26], and then the effect of the V_{th} variations (i.e., -10% ~ +10 %) of the driver transistors is observed.

Fig. 12 shows the simulation of 500 TSVs under V_{th} variation in the transistors of wrapper cells. The x-axis indicates the capacitances of TSVs and the y-axis represents the number of TSVs that have passed the test. The most impact value on the test is the variation of a TSV driver, so there are five kinds of lines (i.e., -10%, -5%, 0%, 5%, 10%). A lower V_{th} results in a "false positive" and a higher V_{th} value may cause a "false negative". This line graph shows the effect of the V_{th} variation and the TSV capacitance variation. It is clear that the number of passed TSVs decreases when the TSV capacitance gets higher. Moreover, a higher V_{th} variation also causes a decrease in the number of passed TSV. The acceptable margin of the process variation can be applied for the filtration of TSVs.

Table 5. Area Overhead of modified wrapper cells

Wrapper Cell Type	Original Area (μm^2)	Proposed (μm^2)			
		Input		Output	
		Area	Δ (%)	Area	Δ (%)
WC_SD1_CII (basic)	12.2	17.3	41.8	23.0	88.5
WC_SD2_CIO (transfer)	34.6	41.4	19.7	42.5	22.8
WC_SF2_CIO	27.0	36.0	33.3	36.0	33.3
WC_SD2_CII	16.2	24.1	48.8	25.2	55.6
WC_SD1_CII_UD	25.6	33.5	30.9	34.6	35.2
WC_SD2_CIU_UF	34.6	44.3	28.0	45.7	32.1
WC_SD3_CII_UD	47.2	55.1	16.7	56.2	19.1
WC_SD1_CN	12.6	22.0	74.6	23.0	82.5
WC_SD1_CBI_UD	12.2	17.3	41.8	23.0	88.5

To estimate the area overhead of the proposed method, Design Compiler with a TSMC 65 nm low power library is used. To use the proposed method, the wrapper cells need to be modified requiring a phased-lock-loop (PLL) to provide a high frequency test clock. In general the PLL is commonly used for memory built-in self-test circuitry [27, 28], and it can be reused for TSV testing as well. Hence, only the area of wrapper cell and driver are considered, excluding the silicon area for PLL. Table 5 shows the area overhead for different types of IEEE std. 1500 wrapper cells. For an input wrapper cell, the area overhead is from 16.7% to 74.6%, and it is from 19.1% to 88.5% for an output wrapper cell.

It deserves noting that no extra driver is required for output cells because the driver is embedded with the wrapper cell for the normal operation. Since the area of wrapper cells is negligible with respect to the entire integrated circuit [7] and the proposed augmentation is only applied for TSV wrapper cells, a negligibly small

area overhead is required to implement this technique.

VI. CONCLUSIONS AND FUTURE WORK

A pre-bond TSV test technique is presented based on IEEE std. 1500. For that, modifications in IEEE std. 1500 wrapper cells are proposed without any test-dedicated pin. The proposed modifications comply with the conventional testing schemes. The simulation results show that the sensitivity of the proposed method for detecting small TSV defects can be improved by appropriately adjusting the driving strength and the test clock frequency. The proposed method also supports diagnosis and shortens the test time at the cost of trivial area overhead.

As a future work, the proposed method can be used to characterize TSV defects using technology dependent practical TSVs. This work only targets at defects that are associated with a single TSV; however, that of with multiple TSVs (e.g. cross-talk, bridge) [29-31] can also be targeted using the proposed method by manipulating test patterns. In addition, the manipulation can also be helpful in handling false-positive and false-negative issues because simultaneous charging and discharging of multiple TSVs may cause IR-drop. The proposed method is also envisioned to be utilized for mid-bond and post-bond TSV test stages.

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