# Normally-Off Operation of AlGaN/GaN Heterojunction Field-Effect Transistor with Clamping Diode

Sang-Woo Han<sup>1</sup>, Sung-Hoon Park<sup>1</sup>, Hyun-Seop Kim<sup>1</sup>, Jongtae Lim<sup>1</sup>, Chun-Hyung Cho<sup>2</sup>, and Ho-Young Cha<sup>1,\*</sup>

Abstract—This paper reports a new method to enable the normally-off operation of AlGaN/GaN heterojunction field-effect transistors (HFETs). A capacitor was connected to the gate input node of a normally-on AlGaN/GaN HFET with a Schottky gate where the Schottky gate acted as a clamping diode. The combination of the capacitor and Schottky gate functioned as a clamp circuit to downshift the input signal to enable the normally-off operation. The normally-off operation with a virtual threshold voltage of 5.3 V was successfully demonstrated with excellent dynamic switching characteristics.

*Index Terms*—AlGaN/GaN heterojunction field-effect transistor, clamp circuit, normally-off operation, Schottky gate

#### **I. INTRODUCTION**

Due to the excellent material characteristics such as high breakdown field and high mobility, GaN has been receiving great attention for a next generation power semiconductor with high conversion efficiency and fast switching speed [1, 2]. In addition, the strong polarization effects at AlGaN/GaN heterojunction interface create a two-dimensional electron gas channel

Fundamentals and Applications of Advanced Semiconductor Devices <sup>1</sup>School of Electrical and Electronic Engineering, Hongik University, Mapo-gu, Seoul 121-791, Korea with very high carrier concentration. Despite these outstanding material properties, the normally-on operation characteristics of typical AlGaN/GaN heterojunction field-effect transistors (HFETs) make it difficult for them to be commercialized because the normally-off operation is strongly desired for circuit simplification and safety issues [3].

Several methods have been reported to achieve the normally-off operation of AlGaN/GaN HFETs, including fluorine plasma treatment [4], p-GaN gate [5], recessed MIS gate [6, 7], and cascode configuration [8]. However, most normally-off technologies reported previously exhibited relatively higher on-resistance values due to the limited carrier density in comparison with conventional normally-on AlGaN/GaN HFETs. It should be noted that the cascode configuration requires an additional Si MOSFET for normally-off switching operation, which not only enlarges the chip size and production cost but also increases the parasitic inductance caused by connection. In our previous work, we proposed a new concept for normally-off AlGaN/GaN HFETs where a clamp circuit was integrated into a normally-on AlGaN/GaN MOS-HFET [9]. The integrated clamp circuit consisting of a MIM capacitor and an AlGaN/GaN Schottky barrier diode (SBD) shifted the input signal downward enabling the normally-off operation.

In this work, we proposed another method to mimic the clamping operation using an AlGaN/GaN HFET with a Schottky gate structure. The clamping operation is illustrated in Fig. 1. Unlike a MOS gate in our previous work [9], the Schottky gate of an HFET itself serves as a clamping diode. With a capacitor connected to the gate

Manuscript received Aug. 29, 2015; accepted Oct. 26, 2015 A part of this work was presented in Asia-Pacific Workshop on

<sup>&</sup>lt;sup>2</sup> Department of Electronic & Electrical Engineering, College of Science and Technology, Hongik University, Sejong, 339-701, Korea E-mail : hcha@hongik.ac.kr



Fig. 1. Configuration of clamping AlGaN/GaN HFET.

node, the input signal level is downshifted allowing the normally-on AlGaN/GaN HFET with a negative threshold voltage to be operated as a normally-off device with a positive threshold voltage.

# **II. DEVICE FABRICATION**

The epitaxial structure consisted of a 2 nm undoped GaN layer, a 22.5 nm Al<sub>0.25</sub>Ga<sub>0.75</sub>N barrier layer, a 330 nm GaN channel layer, and a 4 µm buffer layer on a Si (111) substrate. The device fabrication started with Ohmic contact formation using Ti/Al/Ni/Au (= 20/100/25/50 nm) metallization annealed at 800°C for 1 min in N<sub>2</sub> ambient. After Ohmic contact formation, the active regions were isolated by low damage dry etching using Cl<sub>2</sub>/BCl<sub>3</sub>-based inductively coupled plasma reactive ion etching. A 30 nm SiO<sub>2</sub> film was deposited as a passivation layer at 350°C using plasma-enhanced chemical vapor deposition. The SiO<sub>2</sub> layer for the Schottky gate contact region was etched by low damage  $SF_6/O_2/Ar$ -based reactive ion etching. A Ni/Au (= 20/200 nm) metal stack was evaporated after a following patterning process to form the Schottky gate and pad



Fig. 2. Cross-sectional schematic of a fabricated AlGaN/GaN-on-Si HFET.

electrodes simultaneously. The source-to-gate distance, gate length, and gate-to-drain distance of the HFET were 3, 2, and 15  $\mu$ m, respectively. A post-metallization annealing was carried out at 400°C for 20 min in O<sub>2</sub> ambient to improve the interface quality between SiO<sub>2</sub> passivation and GaN surface [6]. Lastly, a source-connected field plate was fabricated by 200 nm SiN<sub>x</sub> deposition and Ni/Au metallization in order to suppress the high electric field at the gate edge. The gate overhang length and the field plate extension from the gate edge were 1 and 3  $\mu$ m, respectively. The cross-sectional schematic of a fabricated device is illustrated in Fig. 2.

#### **III. RESULTS AND DISCUSSION**

The typical current-voltage characteristics of the fabricated AlGaN/GaN-on-Si HFETs are shown Fig. 3. The device exhibited the normally-on characteristics with a gate threshold voltage of -4 V and a maximum transconductance of 175 mS/mm at the drain voltage of 5 V. The maximum drain current density was ~650 mA/mm at the gate voltage of 1 V and the calculated on-resistance was 1.61 m $\Omega$ -cm<sup>2</sup> where the active channel area was used for calculation. The breakdown voltage was > 900 V under the pinch-off condition. The typical diode characteristics between the Schottky gate and source electrodes are shown in Fig. 3(c).

In order to demonstrate the normally-off switching operation of the proposed device, a capacitor was connected to the gate input electrode of the device for clamping function. It should be noted that the time constants for charging and discharging modes must be taken into account with the operation switching frequency when determining the capacitance value. The



**Fig. 3.** (a) Typical transfer, (b) output and breakdown characteristics of a fabricated AlGaN/GaN-on-Si HFET, (c) diode forward characteristics between gate and source electrodes.

capacitance value used in this work was 5 nF.

As shown in Fig. 4(a), a hard switching method was used to evaluate the switching characteristics. The switching frequency was 10 kHz with a 50% duty cycle.



**Fig. 4.** (a) Hard switching test circuit, (b) measured oscillation waveforms, (c) dynamic on-resistance characteristics.

The voltage waveforms measured at three nodes confirmed successful normally-off operation of the proposed device (see Fig. 4(b)). The input driving signal was downshifted from (+10 V, 0 V) to (+0.7 V, -9.3 V) by the clamp circuit and the device exhibited stable

switching characteristics. The off-set voltage of 0.7 V was associated with the Schottky turn-on characteristics  $(V_D)$  shown in Fig. 3(c). The virtual threshold voltage was 5.3 V taking account of the downshifted off-state voltage of -9.3 V and the threshold voltage of HFET (= -4 V).

The dynamic on-resistance characteristics were investigated up to the drain voltage of 200 V. The off-state drain bias stress was increased from 50 V to 200 V by a 50 V step. As shown in Fig. 4(c), the dynamic on-resistance increased by only 9% at the drain voltage of 200 V.

## **IV. CONCLUSIONS**

We proposed a clamping AlGaN/GaN HFET to achieve stable normally-off operation with easy device processing. With a capacitor connected to the gate input node, the Schottky gate functioned as a clamping diode in a clamp circuit. As a result, the input driving signal was downshifted enabling the normally-off switching operation. In comparison with other conventional normally-off GaN based FETs, higher current (i.e. low on-resistance) and higher threshold voltage can be achieved with easy device processing. The prototype device exhibited an on-resistance of 1.61 m $\Omega$ ·cm<sup>2</sup> with a maximum current density of ~650 mA/mm and a breakdown voltage of > 900 V. The virtual threshold voltage was 5.3 V under the clamping operation.

#### ACKNOWLEDGMENTS

This work was supported by Basic Science Research Program (No. 2015R1A6A1A03031833) and grant (2012M3A7B4035274) through the National Research Foundation of Korea (NRF) funded by the Ministry of Education and the IT R&D program of MOTIE/KEIT (10048931, the development of epi-growth analysis for next semiconductor and power semiconductor fundamental technology).

### REFERENCES

 B.-R. Park, et al, "High-quality ICPCVD SiO<sub>2</sub> for normally off AlGaN/GaN-on-Si recessed MOSHFETs," *IEEE Electron Device Lett.*, Vol. 34, No. 3, pp. 354-356, Mar. 2013.

- [2] J.-G. Lee, et al., "State-of-the-art AlGaN/GaN-on-Si heterostructure field effect transistors with dual field plates," *Appl. Phys. Exp.*, Vol. 5, No. 6, pp. 066502-066502-3, May. 2012.
- [3] F. Medjdoub, et al., "Low on-resistance highbreakdown normally off AlN/GaN/AlGaN DHFET on Si substrate." *IEEE Electron Device Lett.*, Vol. 31, No. 2, pp. 111-113, Feb. 2010.
- [4] W. Chen, et al, "High performance AlGaN/GaN lateral field-effect rectifiers compatible with high electron mobility transistors," *Appl. Phys. Lett.*, Vol. 92, No. 25, p. 253501, Jun. 2008.
- [5] Y. Uemoto, et al., "Gate injection transistor (GIT)-A normally-off AlGaN/GaN power transistor using conductivity modulation," *IEEE Trans. Electron Devices*, Vol. 54, No. 12, pp. 3393–3399, Dec. 2007.
- [6] S.-W. Han, et al, "Dynamic on-resistance of normally-off recessed AlGaN/GaN-on-Si metaloxide-semiconductor heterojunction field-effect transistor," *Appl. Phys. Exp.*, Vol. 7, No. 11, p. 111002, Nov. 2014.
- [7] X. Zhe, et al, "Demonstration of Normally-Off Recess-Gated AlGaN/GaN MOSFET Using GaN Cap Layer as Recess Mask," *IEEE Electron Device Lett.*, Vol. 35, No. 12, pp. 1197-1199, Dec. 2014.
- [8] X. Huang, et al, "Evaluation and application of 600V GaN HEMT in cascode structure," *Applied Power Electronics Conference and Exposition* (APEC), pp.1279-1286, 2013.
- [9] S.-W. Han, et al, "AlGaN/GaN Metal-Oxide-Semiconductor Heterojunction Field-Effect Transistor Integrated with Clamp Circuit to Enable Normallyoff Operation," *IEEE Electron Device Lett.*, Vol. 36, No. 6, pp. 540-542, Jun. 2015.



**Sang-Woo Han** received the B.S. and M.S. degrees in the school of electronic and electrical engineering from Hongik University, Seoul, Korea, in 2013 and 2015, respectively. His interests include fabrication of high power wide bandgap

semiconductor where include AlGaN/GaN heterojunction field-effect transistor and monolithic integration for power IC.



**Sung-Hoon Park** received the B.S. degree in the school of electronic and electrical engineering from Hongik University, Seoul, Korea, in 2014. He is currently pursuing the M.S. degree at Hongik University. His research intersets include the fabrication and

the analysis of gallium nitride devices.



**Hyun-Seop Kim** received the B.S. degree in electronic and electrical engineering from Hongik University, Seoul, Korea, in 2014. He is currently pursuing the M.S. degree at Hongik University. His research interests include the characterization

of gallium nitride devices.



Jongtae Lim received the B.S. and M.S. degrees in Electronics Engineering from Seoul National University, Seoul, Korea in 1989 and 1991, respectively, and received the Ph.D. degree from the Department of Electrical Engineering and Computer

Science, University of Michigan, Ann Arbor, in 2001. In September 2004, he joined Korea Aerospace University, Goyang, Korea. Since March 2008, he has been with Hongik University, Seoul, Korea, where he is now Associate Professor of the School of Electronic & Electrical Engineering. His research interest are in digital communication systems, signal processing & semiconductor simulation.



**Chun-Hyung Cho** received the B.S. degree in Electrical Engineering from the Seoul National University, Seoul, South Korea, in 1997, and the M.S. and ph.D. degrees in Electrical and Computer Engineering from Auburn University, Auburn, AL, in 2001 and

2007, respectively. In 2009, he joined Hongik University, Sejong where he is currently an assistant professor in the Department of Electronic & Electrical engineering. His research interests include the application of analytical and experimental methods of piezoresistive sensors to problems in electronic packaging.



**Ho-Young Cha** received the B.S. and M.S. degrees in electrical engineering from Seoul National University, Seoul, Korea, in 1996 and 1999, respectively, and the Ph.D. degree in electrical and computer engineering from Cornell University,

Ithaca, NY, in 2004. He was a Postdoctoral Research Associate with Cornell University until 2005, where he focused on the design and fabrication of SiC and GaN electronic devices and GaN nanowires. He was with the General Electric Global Research Center, Niskayuna, NY, from 2005 to 2007, developing wide- bandgap semiconductor sensors and high power devices. Since 2007, he has been with Hongik University, Seoul, where he is currently an Associate Professor in the School of Electronic and Electrical Engineering. His research interests include wide bandgap semiconductor devices. He has authored over 70 publications in his research area.