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Effect of Bottom Electrode on Resistive Switching Voltages in Ag-Based Electrochemical Metallization Memory Device

Sungjun Kim[1], Seongjae Cho[2], and Byung-Gook Park[1,*]

Abstract—**In this study, we fabricated Ag-based electrochemical metallization memory devices which is also called conductive-bridge random-access memory (CBRAM) in order to investigate the resistive switching behavior depending on the bottom electrode (BE). RRAM cells of two different layer configurations having Ag/Si_3N_4/TiN and Ag/Si_3N_4/p^+ Si are studied for metal-insulator-metal (MIM) and metal-insulator-silicon (MIS) structures, respectively. Switching voltages including forming/set/reset are lower for MIM than for MIS structure. It is found that the workfunction different affects the performances.**

Index Terms—**Electrochemical metallization memory, conductive-bridge random-access memory, silicon nitride, metal-insulator-metal, metal-insulator-silicon**

I. INTRODUCTION

In recent days, resistive random-access memory (RRAM) has attracted attention as a promising candidate for the next-generation non-volatile memory (NVM) due to its superior scalability, high-speed operation, and low power consumption [1-13] in order to overcome the limitations such as scaling issues of conventional memories [14, 15]. There can be a number of resistive switching mechanisms classified into thermo-chemical, valence-change, and electro-chemical effects depending on the material properties of electrode and resistive switching layer [1]. Also, it has been reported that RRAM device based on electrochemical metallization mechanism is particularly suitable for embedded NVM applications by adopting 1-transistor 1-resistor (1T1R) configuration due to its fast switching speed and low switching voltage [12, 13]. RRAM devices based on conventional metal-insulator-metal (MIM) structure have been widely researched, whereas metal-insulator-silicon (MIS) structure which can be integrated with CMOS circuits (the easiness is improved if 1T1R structure is adopted) has been seldom studied so far [5, 6, 9]. In this work, in order to further study RRAM device in the MIS structure, we discuss different resistive switching behaviors between RRAM cells having TiN and p^+ Si.

II. EXPERIMENTAL

Fig. 1(a) and (b) show the schematic of RRAM cells having MIM structure, Ag/Si_3N_4/TiN, and MIS structure, Ag/Si_3N_4/Si, respectively. For the MIM device, a 100-nm-thick TiN bottom electrode (BE) was deposited using a thermal evaporator after SiO_2 deposition on the Si substrate. On the other hand, the BE of MIS device was formed in the Si substrate by ion implantation of BF_2^+ (an acceleration energy of 40 keV and with a dose of 5×10^{15} cm^{-2}). The doping concentration and junction depth are approximately 1×10^{20} cm^{-3} and 1 μm,

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[1] Department of Electrical and Computer Engineering and the Inter-university Semiconductor Research Center (ISRC), Seoul National University, Seoul 08826, Republic of Korea.
[2] Department of Electronic Engineering, Gachon University, 1342 Seongnam-daero, Sujeong-gu, Seongnam-si, Gyeonggi-do 13120, Republic of Korea.
E-mail : bgpark@snu.ac.kr

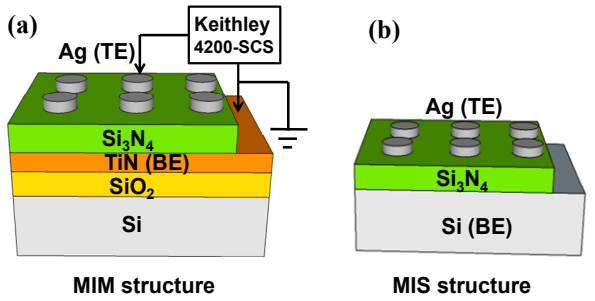

Fig. 1. Device schematics (a) Ag/Si_3N_4/TiN, (b) Ag/Si_3N_4/p^+ Si RRAM devices.

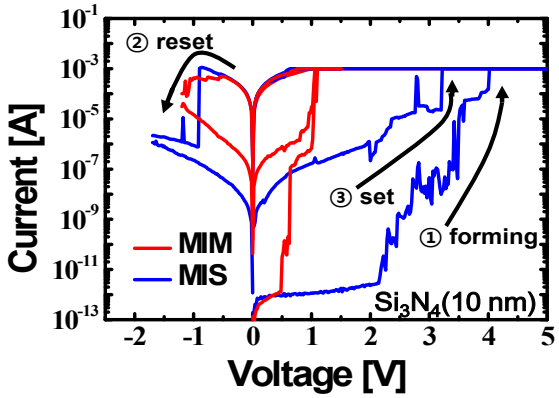

Fig. 2. *I-V* characteristics of Ag/Si_3N_4/TiN and Ag/Si_3N_4/p^+ Si RRAM cells.

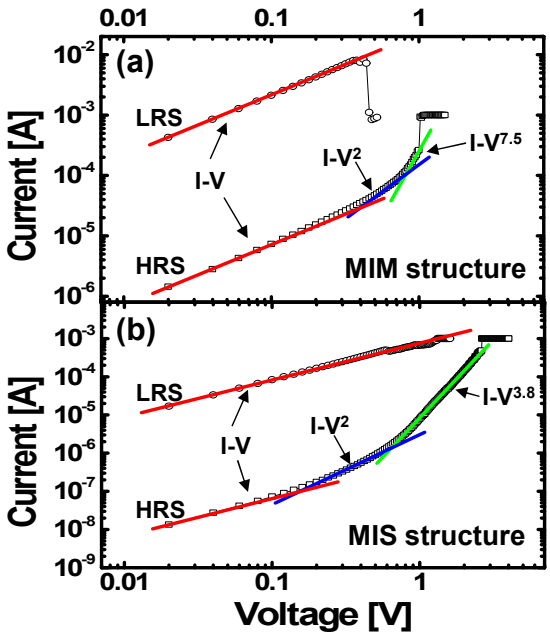

Fig. 3. Logarithmic *I-V* plots of (a) Ag/Si_3N_4/TiN, (b) Ag/Si_3N_4/p^+ Si RRAM cells.

respectively [9]. Subsequently, Si_3N_4 switching layer (SL) with different thicknesses of 5, 10, 20, and 30 nm were deposited by a plasma-enhanced chemical vapor deposition (PECVD) at 300˚C using 5% SiH_4/N_2 (800 sccm), NH_3 (10 sccm), and N_2 (1200 sccm) as the mixture precursor for both devices. Finally, Ag top electrode (TE) with a thickness of 100 nm was constructed via thermal evaporator using a shadow mask with circular patterns with 100-μm radii for both structures. All the electrical measurements were carried out by Keithley 4200-SCS semiconductor parameter analyzer (SPA) in the DC voltage sweep mode as illustrated in Fig. 1(a). For the RRAM operations, BEs were grounded and the control bias was applied to TEs.

III. Results and Discussion

Fig. 2 exhibits the typical bipolar *I-V* curves from the fabricated RRAM cells with Ag/Si_3N_4/TiN and Ag/Si_3N_4/p^+ structures. Initial electrical forming process was performed under a high enough positive voltage to activate the pristine RRAM cell and to prepare low-resistance state (LRS), which reached 1 V and 4 V, respectively for MIM and MIS cells, as shown in the figure. Subsequently, the RRAM cells are switched from LRS to high-resistance state (HRS) by backward sweep down to certain negative voltages for the reset process. The devices return to LRS over the positive sweeps for set process. For the MIS RRAM cell, the magnitude of forming voltage was larger than that of set voltage. For the forming and set processes, the compliance current limit was set to 1 mA to avoid damage of the Si_3N_4 layer. In order to investigate the conduction mechanisms via the conducting filaments in SLs, *I-V* curves are depicted in the logarithmic scale for the devices with MIM and MIS structures as shown in Fig. 3(a) and (b), respectively. Ohmic transport with the slope of 1 is observed in the LRS curves from both devices. However, the *I-V* curves in the HRS are divided into three different linear regions for both devices: low-voltage region demonstrating Ohmic conduction having slope of 1, higher-voltage region with the slope of 2, and more drastically changing current region with slopes of more than 3 before soft breakdown occurs for set switching. The experimental results show good agreements with space-charge-limited current (SCLC) mechanism for both devices [16, 17]. It is widely believed that the resistive switching behavior of RRAM devices with Ag TE with high diffusivity in

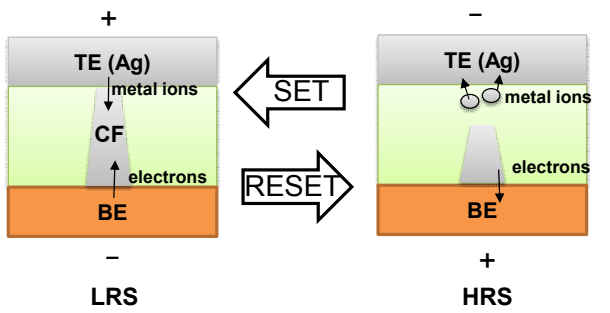

Fig. 4. Schematic showing the formation and rupture of conducting filament in Ag-based RRAM device.

electrolyte and inert BE is strongly related to the formation and dissolution of Ag-rich conducting filament [18, 19]. Examples of electrolyte materials for SL are chalcogenides, metal oxide, and nitride [20, 21]. In one of our previous works, it was demonstrated that the conducting filaments in the Si_3N_4 RRAM using Ag TE had metallic properties by series of temperature-controlled experiments [9].

Therefore, resistive switching in both devices attributes to the diffusion of Ag ions as the result of oxidation and reduction processes as schematically shown in Fig. 4. Ag ions migrate toward BE when a positive bias is applied to Ag TE acting as the conducting filament source. Then, Ag-rich conducting filament is formed between TE and BE through Si_3N_4 layer, which leads to LRS. Conversely, over the reset process with a negative bias on the TE, Ag-rich filament near the BE is electrochemically dissolved, which results in HRS. Fig. 5 shows the distributions of (a) forming, (b) set, and (c) reset voltages with different Si_3N_4 thicknesses of 5, 10, 20, and 30 nm. MIM cells with a 5-nm-thick Si_3N_4 layer show no switching operation at 1-mA compliance current due to the initially high leakage level as shown in Fig. 5(a). Forming voltage increases with Si_3N_4 thickness since a higher electric field is needed for forming conducting filament bridges through the thick dielectric. For instance, 15 V or higher forming voltage is required for MIS devices as shown in Fig. 5(a). On the other hand, set and reset voltages are less affected by Si_3N_4 thickness. It is due to the fact that the conducting filaments are not totally ruptured by partially disconnected in the vicinity of TE. Thus, although forming voltage is largely determined by the thickness of SL since the initial connection by conducting filament between BE and TE takes place through the SL, the set and reset voltages are

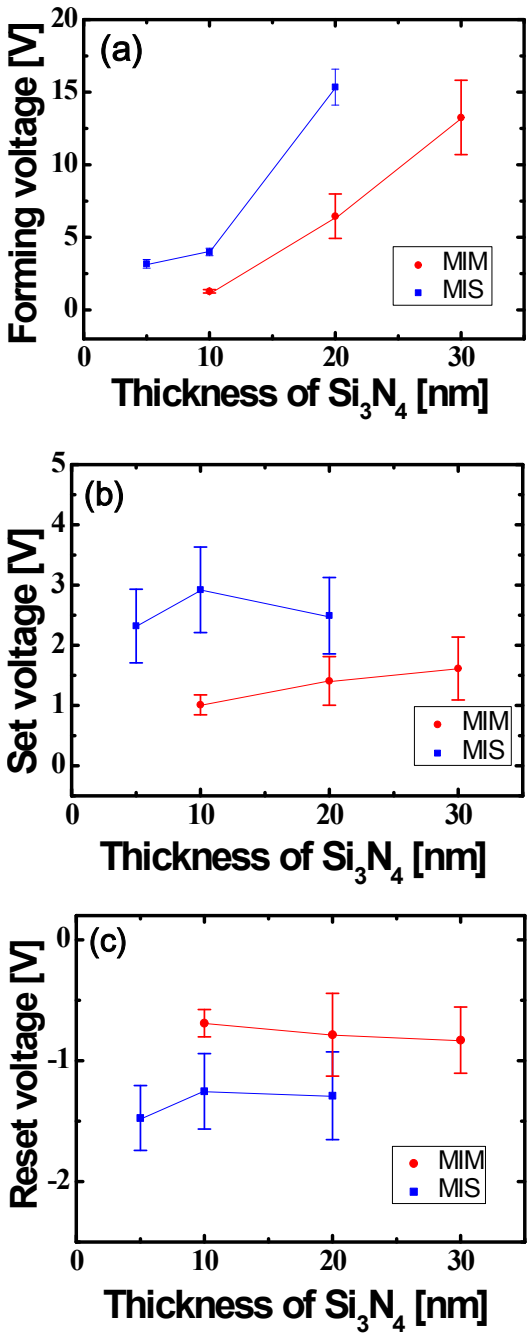

Fig. 5. Statistical distributions of (a) forming, (b) set, (c) reset voltages as a function of Si_3N_4 thickness for RRAM devices with Ag/Si_3N_4/TiN and Ag/Si_3N_4/p^+ Si structures.

lower than forming voltage. Forming-less LRS can be also obtained when Si_3N_4 thickness is below 5 nm and 10 nm for MIM and MIS devices, respectively. All the forming/set/reset voltages of MIM device have smaller magnitudes compared with those of MIS device, Fig. 6(a) and (b) show the energy-band diagrams of MIM and MIS structures, respectively, under the flat-band

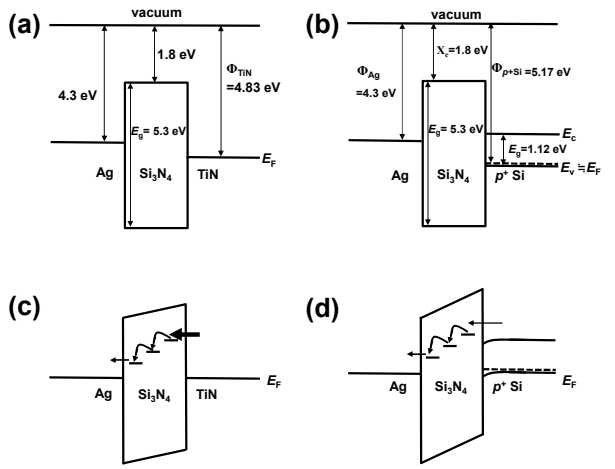

Fig. 6. Energy-band diagrams (a) MIM, (b) MIS structures under flat-band conditions, (c) MIM, (d) MIS structures under equilibrium.

conditions fully considering the material parameters [9, 22]. Fig. 6(c) and (d) show the band diagrams of MIS and MIS structures, respectively, under thermal equilibrium with no electrical bias. As can be implied by the figures, the electric field across the Si_3N_4 switching layer is determined by the workfunction difference between BE and TE (Φ_{BE} - Φ_{TE}). Although higher electric field is induced in the Si_3N_4 layer of the MIS structure, tunneling from the Si conduction band is much smaller than that of MIM device, since the Si substrate is high *p*-type doped. Therefore, a higher voltage is required to conduct forming process in the MIS structure than in the MIM device. Also, it is known that the roughness of BE has a substantial effect on switching voltage [23]. The surface roughness of TiN BE should be much more uneven than that of Si-substrate BE since TiN was deposited by a physical vapor deposition (PVD) process. The rough surface of MIM-structure device can generate more traps between BE and SL. The electric fields are not uniformly distributed but can be focused on the field-concentrating local spots over the surface, by which the switching voltages are reduced in effect.

IV. CONCLUSIONS

In this work, RRAM devices having Ag/Si_3N_4/TiN and Ag/Si_3N_4/p^+ Si structures were fabricated their resistive switching characteristics have been studied. MIM device showed lower operation voltages compared with MIS device. It is concluded that workfunction difference and surface roughness play an important role in determining the switching voltages of RRAM cell. By the results, it is assured that the layer configuration in the RRAM device is also crucial for achieving the low-power operation capability.

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Sungjun Kim received the B.S. degree in electronic engineering from Hanyang University, Seoul, Korea, in 2011. He is currently working toward Ph.D. degree in the Department Electrical and Computer Engineering, Seoul National University, Seoul, Korea. His research interests include design, fabrication, and characterization of low-power resistive-switching random-access memory (RRAM) devices.

Sungjae Cho received the B.S. and Ph.D. degrees in electrical engineering from Seoul National University, Seoul, Korea, in 2004 and 2010, respectively. He worked with the National Institute of Advanced Industrial Science and Technology (AIST) as an Exchange Research in 2009. He worked as a Postdoctoral Research at Seoul National University in 2010, and at the Department of Electrical Engineering, Stanford University from 2010-2013. He is currently working as an Assistant Professor at the Department of Electronic Engineering and at the Department of IT Convergence Engineering, Gachon University, Seongnam-si, Korea. His research interests include nanoscale CMOS devices, emerging technologies, optical devices, and CMOS-photonics integrated circuits.

Byung-Gook Park received the B.S. and M.S. degrees in electronic engineering from Seoul National University in 1982 and 1984, respectively, and the Ph.D. degree in electrical engineering from Stanford University, Stanford, CA, in 1990. From 1990 to 1993, he was with AT&T Bell Laboratories, where he contributed to the development of 0.1-μm CMOS and its characterization. From 1993 to 1994, he was with Texas Instruments, developing 0.25-μm CMOS. In 1994, he joined Seoul National University as an Assistant Professor in the School of Electrical Engineering (SoEE), where he is currently a Professor. He led the Inter-university Semiconductor Research Center (ISRC), Seoul National University, as the Director from June 2008 to June 2010. His current research interests include the design and fabrication of nanoscale CMOS, Si quantum devices, emerging memory technologies, and neuromorphic systems. He has authored and co-authored more than 950 research papers in journals and conferences. Prof. Park has served as a committee member on several international conferences including Microprocesses and Nanotechnology, International Electron Devices Meeting (IEDM), Conference on Solid State Devices and Materials (SSDM), and IEEE Silicon Nanoelectronics Workshop (SNW) and served as an Editor of IEEE Electron Device Letters. He received Best Teacher Award from SoEE of Seoul National University in 1997, Doyeon Award from Creative Research from ISRC in 2003, Haedong Paper Award from the Institute of Electronic Engineers of Korea (IEEK) in 2005, and Educational Award from College of Engineering, Seoul National University, in 2006. Also, he received Haedong Academic Research Award from IEEK in 2008.