

# Microwave Negative Group Delay Circuit: Filter Synthesis Approach

Junsik Park · Girdhari Chaudhary · Junhyung Jeong · Yongchae Jeong\*

---

## Abstract

---

This paper presents the design of a negative group delay circuit (NGDC) using the filter synthesis approach. The proposed design method is based on a frequency transformation from a low-pass filter (LPF) to a bandstop filter (BSF). The predefined negative group delay (NGD) can be obtained by inserting resistors into resonators. To implement a circuit with a distributed transmission line, a circuit conversion technique is employed. Both theoretical and experimental results are provided for validating of the proposed approach. For NGD bandwidth and magnitude flatness enhancements, two second-order NGDCs with slightly different center frequencies are cascaded. In the experiment, group delay of  $5.9 \pm 0.5$  ns and insertion loss of  $39.95 \pm 0.5$  dB are obtained in the frequency range of 1.935–2.001 GHz.

**Key Words:** Bandstop Filter, Frequency Transformation, Filter Approach, Low Pass Filter Prototype, Negative Group Delay.

---

## I. INTRODUCTION

Most media exhibit a normal propagation characteristic called subluminal velocity, where the speed of propagation of individual time-harmonic components is slower than the speed of light,  $c$ , in vacuum at all frequencies. However, in a specific and narrow frequency band of signal attenuation or at an anomalous dispersion frequency, the group velocity is observed to be greater than  $c$ . This abnormal wave propagation is called superluminal velocity or negative group velocity [1, 2]. At first, the concept of superluminal velocity seems to defy causality. However, many practical experiments have shown that the concept of superluminal velocity does not violate the definition of a causal system [3–5].

One example of the concept of superluminal velocity is the negative group delay (NGD); this refers to the phenomenon whereby an electromagnetic wave traverses a medium in such a

manner that its amplitude envelope is advanced rather than delayed [6]. Recently, many studies have designed negative group delay circuits (NGDCs) and used them in practical applications such as enhancing the efficiency of a feed-forward amplifier [7], shorting delay lines [8], realizing non-Foster reactive elements [9], and minimizing beam-squint problems in series-fed antenna arrays systems [10].

The conventional design method of active and passive NGDCs is based on only single *RLC* resonators [11–18]. The NGD bandwidth and magnitude flatness should be as wide as possible for applications in RF circuits and systems. However, conventional NGDCs suffer from smaller NGD bandwidth and poor magnitude flatness. To overcome these problems, some studies have attempted to design NGDCs using different methods such as cascading the number of resonators with slightly different center frequencies [16] and cross-coupling between resonators [17].

---

Manuscript received September 25, 2015 ; Revised November 23, 2015 ; Accepted November 24, 2015. (ID No. 20150925-052J)

Division of Electronics and Information Engineering, IT Convergence Research Center, Chonbuk National University, Jeonju, Korea.

\*Corresponding Author: Yongchae Jeong (e-mail:ycjeong@jbnu.ac.kr)

---

This is an Open-Access article distributed under the terms of the Creative Commons Attribution Non-Commercial License (<http://creativecommons.org/licenses/by-nc/3.0>) which permits unrestricted non-commercial use, distribution, and reproduction in any medium, provided the original work is properly cited.

© Copyright The Korean Institute of Electromagnetic Engineering and Science. All Rights Reserved.

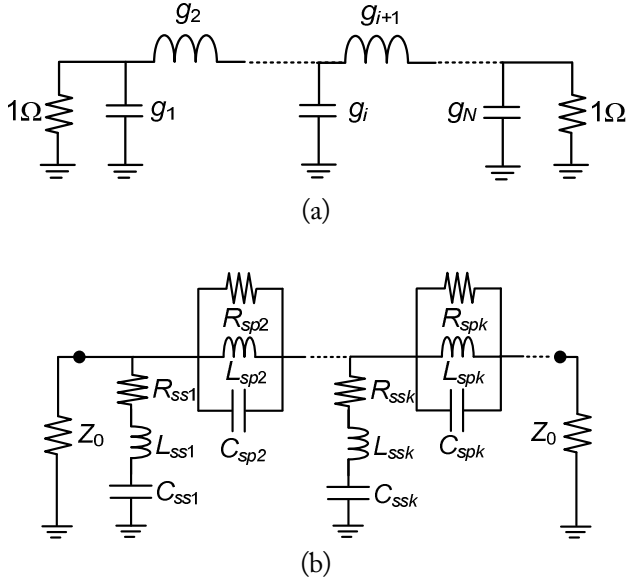


Fig. 1. (a) Low-pass filter prototype and (b) proposed structure of a negative group delay circuit.

Table 1. Specifications of negative group delay circuits

$N$	LPF prototype element values	$f_0$ (GHz)	$\Delta$ (%)	Maximum GD @ $f_0$ (ns)
2	$g_1 = g_2 = 1.4142$	1.962	10	-6.0
3	$g_1 = g_3 = 1$ $g_2 = 2$	1.962	10	-6.0

LPF=low-pass filter, GD=group delay.

In this study, a filter synthesis approach is applied to design an NGDC. In this proposed method, circuit element values are obtained from low-pass filter (LPF) prototypes by applying a frequency transformation.

## II. DESIGN EQUATIONS ANALYSIS

Fig. 1(a) shows the Butterworth LPF prototype. The element values of the LPF are obtained as follows [19].

$$g_k = 2 \sin \frac{(2k-1)\pi}{2N}, \quad k = 1, 2, \dots, N \quad (1)$$

where  $N$  is the order of the filter. Fig. 1(b) shows the structure of the proposed NGDC. The lumped elements of the proposed

NGDC are easily obtained from the LPF by applying the following frequency transformation [19].

$$\frac{1}{\omega'} \leftarrow \Delta \left( \frac{\omega}{\omega_0} - \frac{\omega_0}{\omega} \right) \quad (2)$$

where  $\Delta$  and  $\omega_0$  are the 3-dB fractional bandwidth (FBW) and center frequency of the NGDC, respectively. The element values of the shunt-series branch ( $L_{ssk}, C_{ssk}$ ) are given as follows.

$$L_{ssk} = \frac{Z_0}{g_k \Delta \omega_0} \quad (3a)$$

$$C_{ssk} = \frac{g_k \Delta}{Z_0 \omega_0} \quad (3b)$$

where  $Z_0$ ,  $g_k$ , and  $\omega_0$  are the port impedance,  $k$ -th prototype element value, and center frequency of the NGDC, respectively. Similarly, the element values of the series-parallel branch ( $L_{spk}, C_{spk}$ ) are given as follows.

$$L_{spk} = \frac{Z_0 g_k \Delta}{\omega_0} \quad (4a)$$

$$C_{spk} = \frac{1}{Z_0 g_k \Delta \omega_0} \quad (4b)$$

The resistors are inserted into the shunt and series resonators to obtain the required NGD. The values of these resistors are obtained by analyzing the shunt-series and series-parallel branch elements [18], respectively. The resistances in the shunt-series branch of the NGDC for the required NGD are given as follows.

$$R_{ssk} = \frac{-Z_0/2 + \sqrt{(Z_0/2)^2 - 4Z_0 L_{ssk}/\alpha\tau}}{2} \quad (5)$$

where  $\tau$  and  $\alpha$  are the GD and correction factor, respectively. Similarly, the resistance in the series-parallel branch of the NGDC is given as follows.

$$R_{spk} = \frac{-\alpha\tau/2C_{spk} + \sqrt{(\alpha\tau/2C_{spk})^2 - 4Z_0\alpha\tau/C_{spk}}}{2} \quad (6)$$

A correction factor  $\alpha$  is substituted into (5) and (6) to consider the fact that each resonator contributes to GD and increases the overall GD so that it is higher than the required value for the overall circuit as  $N$  increases. Substituting  $\alpha$  into

Table 2. Element values of negative group delay circuits (NGDCs) with GD=-6 ns

$N$	Element values of the proposed NGDC								
	$L_{ss1}$	$C_{ss1}$	$R_{ss1}$	$L_{sp2}$	$C_{sp2}$	$R_{sp2}$	$L_{ss3}$	$C_{ss3}$	$R_{ss3}$
2	14.34	0.4588	8.18	1.147	5.736	305.5			
3	20.28	0.3245	15.14	1.622	4.056	279.2	20.28	0.324	15.14

Unit:  $L_{ssk}, L_{spk}$  (nH);  $C_{ssk}, C_{spk}$  (pF);  $R_{ssk}, R_{spk}$  ( $\Omega$ ).

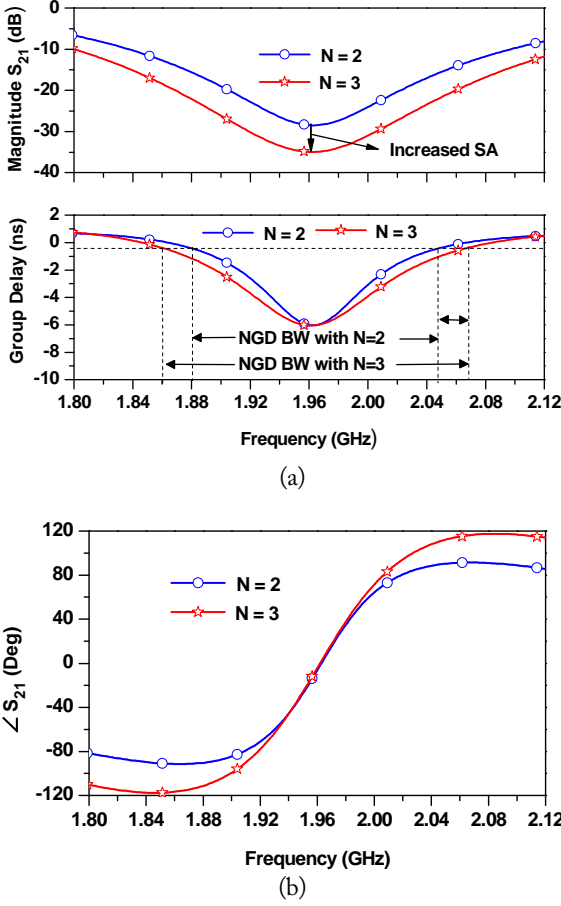


Fig. 2. Synthesized results of proposed negative group delay circuit (NGDC) with different numbers of stages  $N$ : (a) group delay/magnitude and (b) phase characteristics.

Table 3. Calculated NGD BW and  $SA_{\max}$  for different numbers of filter stages

$N$	$GD_{\max}$ (ns)	NGD ( $GD < 0$ ) BW (MHz)	$SA_{\max}$ (dB)
2	-6	200	24.48
3	-6	240	34.96

NGD=negative group delay, BW=bandwidth,  $GD_{\max}$ =maximum achieved group delay,  $SA_{\max}$ =maximum signal attenuation.

these equations compensates for the deviation from the required value.

Fig. 2 shows the synthesized results of the NGDC with different numbers of stages  $N$ . The specifications and calculated

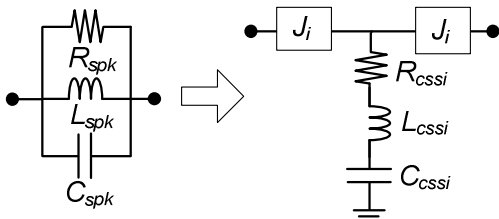


Fig. 3. Series-parallel to shunt-series circuit transformation.

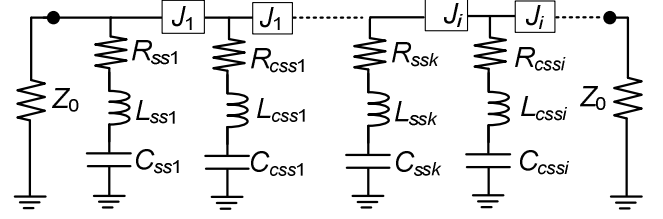


Fig. 4. Proposed negative group delay circuit with  $J$ -inverters and shunt-series  $RLC$  circuits.

circuit element values of the proposed NGDC are shown in Tables 1 and 2, respectively. As shown in Fig 2(a), the NGD bandwidth increases slightly with  $N$ . However, the signal attenuation (magnitude of  $S_{21}$ ) also increases for the same maximum achievable GD, which can be compensated using general purpose gain amplifiers. Therefore, the signal attenuation (SA) of the proposed NGDC should be as small as possible so that the number of gain amplifiers can be reduced. The NGD bandwidth and maximum SA of the simulated circuits are shown in Table 3. From Table 3, it is clear that a trade-off between the NGD, insertion loss (magnitude of  $S_{21}$ ), NGD-bandwidth, and number of stages  $N$  should be considered. Fig. 2(b) shows the phase characteristics of the NGDC with  $N=2$  and  $N=3$ . As seen from Fig. 2(b), the phase of  $S_{21}$  increases with frequency (positive slope) in the case of an NGDC, indicating the presence of NGD.

The proposed NGDC shown in Fig. 1(b) consists of both shunt-series ( $R_{ssk}, L_{ssk}, C_{ssk}$ ) and series-parallel ( $R_{spk}, L_{spk}, C_{spk}$ ) lumped elements. A series parallel-resonator is difficult to implement at the microwave frequencies owing to the limited feasibility of the designed lumped elements.

To overcome this problem, the circuit conversion technique can be applied to convert the series-parallel lumped elements ( $R_{spk}, L_{spk}, C_{spk}$ ) into shunt-series lumped elements ( $R_{cssi}, L_{cssi}, C_{cssi}$ ) using admittance inverters ( $J$ -inverters), as shown in Fig. 3. The corresponding conversion relations are given as follows.

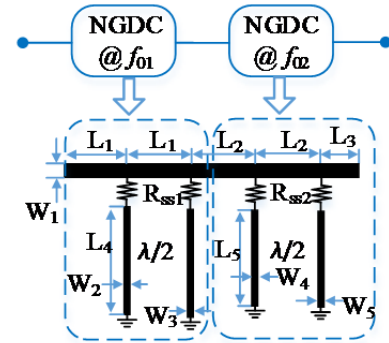


Fig. 5. Structure of cascaded two-stage negative group delay circuit (NGDC) for NGD bandwidth and magnitude flatness enhancements. Physical dimensions:  $L_1=22.90, L_2=26.10, L_3=5, L_4=55.2, L_5=57.36, W_1=3.54, W_2=0.32, W_3=0.54, W_4=0.36, W_5=0.58$  (unit: mm).

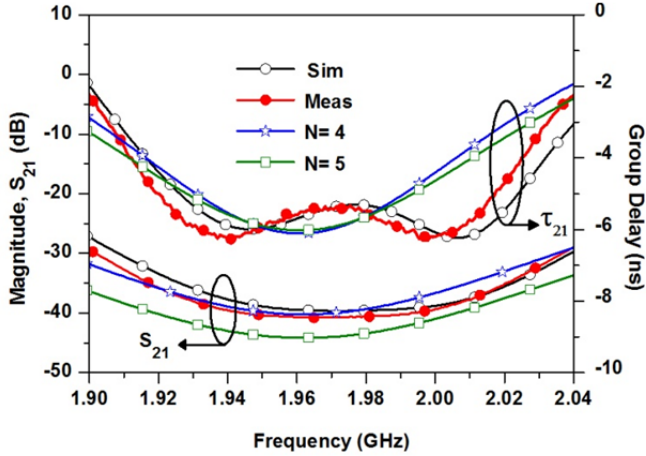


Fig. 6. Simulated and measurement results of cascaded two-stage negative group delay circuit.



Fig. 7. Photograph of fabricated negative group delay circuit.

$$R_{cssi} = \frac{1}{J_i^2 R_{spk}} \quad (7a)$$

$$L_{cssi} = \frac{C_{spk}}{J_i^2} \quad (7b)$$

$$C_{cssi} = J_i^2 L_{spk} \quad (7c)$$

Theoretically, the value of the  $J$ -inverter can be chosen arbitrary. However, in practice,  $J$ -inverters should be chosen carefully because their physical dimensions must be realizable without any difficulties. Fig. 4 shows the overall structure of proposed NGDC; it consists of  $J$ -inverters and shunt-series  $LC$  resonators. The  $J$ -inverters can be implemented using quarter-wavelength transmission lines. The shunt-series  $LC$  resonators can be implemented using either short-circuited half-wavelength or open-circuited quarter-wavelength resonators [19].

### III. SIMULATION AND EXPERIMENTAL RESULTS

To validate the proposed design method, a second order NGDC was designed and fabricated on a substrate with dielectric constant ( $\epsilon_r$ ) of 2.2 and thickness ( $h$ ) of 31 mils. The goal was to design an NGDC with GD of  $-6$  ns at a center frequency of 1.97 GHz. In this work,  $J$ -inverters and shunt-series  $LC$  resonators are implemented with  $\lambda/4$  transmission line and

short-circuited  $\lambda/2$  transmission lines, respectively.

As shown by the results in the previous sections, the NGD bandwidth of the proposed circuit is narrow. One of the ways to increase the NGD bandwidth is to increase  $N$ . However, increasing  $N$  cannot provide a large increase in the NGD bandwidth, as shown in Fig. 2; however, the insertion loss is increased. Another way to employ an NGDC with a wider NGD bandwidth is to cascade NGDCs operating at slightly different center frequencies as shown in Fig. 5. Therefore, in this study, to enhance the NGD bandwidth and magnitude flatness, two-stage NGDCs with center frequencies of 1.932 and 2 GHz and FWB of 10% are cascaded. Fig. 5 shows the physical dimensions of the designed NGDC.

Fig. 6 shows the simulation and measurement results of the fabricated cascaded two-stage NGDC and comparison with NGDCs with  $N=4$  and  $N=5$ . The measurement results agreed well with the simulation results. The measured GD time and insertion loss were  $-5.9 \pm 0.5$  ns and  $39.95 \pm 0.5$  dB, respectively, in the frequency range of 1.935–2.001 GHz.

These results also show that the NGD bandwidth and magnitude flatness are wider than those of NGDCs with  $N=4$  and  $N=5$  and conventional NGDCs [11–17]. However, the trade-off among the NGD, bandwidth and magnitude flatness should be considered. The small fraction of NGD and insertion loss differences between the simulation and the measurement are due to the parasitic components of the resistors. Fig. 7 shows a photograph of the fabricated NGDC.

Table 4 shows a performance comparison of the proposed NGDC with those in previous works. Owing to the trade-off among the maximum achieved GD ( $GD_{max}$ ), maximum SA ( $SA_{max}$ ) and NGD bandwidth (NGD-BW), the figure of merit (FOM) of NGD circuits can be defined as follows.

$$FOM = -\frac{GD_{max} \times NGD - BW}{\sqrt{SA_{max, dB}}} \quad (8)$$

As seen from Table 4, the proposed NGDC provides the

Table 4. Performance comparison of the proposed NGDC with those in previous works

Ref.	$GD_{max}$ (ns)	$SA_{max}$ (dB)	$GD_{max} \pm 0.5$ ns BW (MHz)	FOM
[7]	-9.0	64.2	30	0.089
[13]	-7.9	16.9	10	0.078
[16]	-5.8	26.8	60	0.112
[17]	-1.1	29.3	350	0.083
[18]	-1.7	16	60	0.043
<b>This work</b>	<b>-5.9</b>	<b>39.95</b>	<b>70</b>	<b>0.131</b>

NGDC=negative group delay circuit,  $GD_{max}$ =maximum achieved group delay,  $SA_{max}$ =maximum signal attenuation, BW=bandwidth, FOM=figure of merit.

highest FOM and best performance in terms of GD/magnitude flatness even though the SA is higher than of some previously proposed NGDCs [13, 16-18].

#### IV. CONCLUSION

In this paper, a filter synthesis approach is applied to design a NGDC. The circuit elements of the proposed filter can be obtained from LPF prototype elements. The proposed circuit was implemented with a distributed transmission line using a circuit conversion technique. An experiment was performed to validate the proposed design method. The measurement results agreed well with the simulation results. The proposed NGDC shows the highest FOM, large negative group delay, good magnitude flatness, and wider negative group delay-bandwidth.

This work was supported by the Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education, Science and Technology (No. 2013006660).

#### REFERENCES

- [1] L. Brillouin, *Wave Propagation and Group Velocity*. New York, NY: Academic Press, 1960.
- [2] E. L. Bolda, R. Y. Chiao, and J. C. Garrison, "Two theorems for the group velocity in dispersive media," *Physics Review A*, vol. 48, no. 5, pp. 3890–3894, Nov. 1993.
- [3] A. H. Dorrah, L. Kayili, and M. Mojahedi, "Superluminal propagation and information transfer: a statistical approach in the microwave domain," *Physical Letters A*, vol. 378, no. 44, pp. 3218–3224, Oct. 2014.
- [4] L. J. Wang, A. Kuzmich, and A. Dogariu, "Gain-assisted superluminal light propagation," *Nature*, vol. 406, no. 6793, pp. 277–279, Jul. 2000.
- [5] W. Withayachumnankul, B. M. Fischer, B. Ferguson, B. R. David, and D. Abbott, "A systemized view of superluminal wave propagation," *Proceedings of IEEE*, vol. 98, no. 10, pp. 1775–1786, Oct. 2010.
- [6] C. M. Hymel, M. H. Skolnick, R. A. Stubbers, and M. E. Brandt, "Temporally advanced signal detection: a review of the technology and potential applications," *IEEE Circuits and Systems Magazine*, vol. 11, no. 3, pp. 10–25, Aug. 2011.
- [7] H. Choi, Y. Jeong, C. D. Kim, and J. S. Kenney, "Efficiency enhancement of feedforward amplifiers by employing a negative group delay circuit," *IEEE Transactions on Microwave Theory and Techniques*, vol. 58, no. 5, pp. 1116–1125, May 2010.
- [8] H. Noto, K. Yamauchi, M. Nakayama, and Y. Isota, "Negative group delay circuit for feed-forward amplifier," in *Proceedings of IEEE International Microwave Symposium*, Honolulu, HI, 2007, pp. 1103–1106.
- [9] H. Mirzaei and G. V. Eleftheriades, "Realization of non-Foster reactive elements using negative group delay networks," *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 12, pp. 4322–4332, Dec. 2013.
- [10] H. Mirzaei and G. V. Eleftheriades, "Arbitrary-angle squint free beamforming in series-fed antenna arrays using non-Foster elements synthesized by negative group delay networks," *IEEE Transactions on Antennas and Propagation*, vol. 63, no. 5, pp. 1997–2010, May 2015.
- [11] B. Ravelo, A. Perennec, M. Le Roy, and Y. G. Boucher, "Active microwave circuit with negative group delay," *IEEE Microwave and Wireless Components Letters*, vol. 17, no. 12, pp. 2177–2180, Dec. 2007.
- [12] M. Kandic and G. E. Bridges, "Asymptotic limit of negative group delay in active resonator-based distributed circuits," *IEEE Transactions on Circuits and Systems I*, vol. 58, no. 8, pp. 1727–1735, Aug. 2011.
- [13] G. Chaudhary and Y. Jeong, "Distributed transmission line negative group delay circuit with improved signal attenuation," *IEEE Microwave and Wireless Components Letters*, vol. 24, no. 1, pp. 20–22, Jan. 2014.
- [14] G. Chaudhary, Y. Jeong, and J. Lim, "Miniaturized dual-band negative group delay circuit using dual-plane defected structures," *IEEE Microwave and Wireless Components Letters*, vol. 24, no. 8, pp. 521–523, Aug. 2014.
- [15] G. Chaudhary, Y. Jeong, and J. Lim, "Microstrip line negative group delay filters for microwave circuits," *IEEE Transactions on Microwave Theory and Techniques*, vol. 62, no. 2, pp. 234–243, Feb. 2014.
- [16] G. Chaudhary, J. Jeong, P. Kim, and Y. Jeong, "Negative group delay circuit with improved signal attenuation and multiple pole characteristics," *Journal of Electromagnetic Engineering and Science*, vol. 15, no. 2, pp. 76–81, Apr. 2015.
- [17] G. Chaudhary and Y. Jeong, "A design of compact wide-band negative group delay network using cross-coupling," *Microwave and Optical Technology Letters*, vol. 56, no. 11, pp. 2495–2497, Nov. 2014.
- [18] H. Choi, K. Song, C. D. Kim, and Y. Jeong, "Synthesis of negative group delay time circuit," in *Proceedings of IEEE Asia-Pacific Microwave Conference (APMC)*, Hong Kong, 2008, pp. 1–4.
- [19] G. Mathaei, L. Young, and E. M. T. Jone, *Microwave Filters: Impedance Matching Networks and Coupling Structures*. Dedham, MA: Artech House, 1964.

### Junsik Park



amplifiers.

received the B.E. degree in Electronics Engineering from Chonbuk National University, Jeonju, Republic of Korea, in 2014. He is currently working toward a Master's degree at Division of Electronics and Information Engineering, Chonbuk National University, Republic of Korea. His research interests include RF energy harvesting, high-efficiency power amplifiers, and pre-distortion techniques for linearizing power

### Junhyung Jeong



high-efficiency power amplifiers and RF transmitters.

was born in Seoul, Republic of Korea, in 1956. He received the B.E. and M.E. degrees in Electronics & Information Engineering from the Chonbuk National University, Jeonju, Republic of Korea, in 2012 and 2014, respectively. He is currently working toward a Ph.D. at the Division of Electronics Engineering, Chonbuk National University, Republic of Korea. His research interests include RF filters,

### Girdhari Chaudhary



received the B.E. and M.Tech. degrees in Electronics and Communication Engineering from Nepal Engineering College (NEC), Kathmandu, Nepal and Malaviya National Institute of Technology (MNIT), Jaipur, India in 2004 and 2007, respectively, and a Ph.D. in Electronics Engineering from Chonbuk National University, Republic of Korea in 2013. From 2013 to 2015, he worked as a Postdoctoral Researcher at Chonbuk National University, Korea. He is currently working as a Contract Professor at HOPE-IT Human Resource Development Center-BK21 PLUS, Division of Electronics Engineering, Chonbuk National University, Korea. He is a recipient of a Korean Research Fellowship through the National Research Foundation (NRF) of Korea funded by the Ministry of Education. He is also recipient of the BK21 PLUS Research Excellence Award 2015 from the Ministry of Education, Republic of Korea. He is a reviewer of IEEE Microwave and Wireless Component Letters (MWCL), IEEE Transactions on Microwave Theory and Techniques (T-MTT), Journal of Electromagnetic Waves and Applications (JEWA), and International Journal of RF and Microwave Computer-Aided Engineering. He has authored and co-authored over 48 papers in international journals and conference proceedings. His research interests include multi-band tunable passive circuits, negative group delay circuits and its applications, RF energy harvesting systems and high-efficiency power amplifiers.

### Yongchae Jeong



received B.S.E.E. and M.S.E.E. degrees and a Ph.D. in Electronics Engineering from Sogang University, Seoul, Republic of Korea in 1989, 1991, and 1996, respectively. From 1991 to 1998, he worked as a Senior Engineer with Samsung Electronics. From 1998, he joined the Division of Electronics Engineering, Chonbuk National University, Jeonju, Republic of Korea. From July 2006 to December 2007, he joined Georgia Institute of Technology as a visiting professor. Now, he is a professor, member of the IT Convergence Research Center, and director of the HOPE-IT Human Resource Development Center of BK21 PLUS at Chonbuk National University. He is currently teaching and conducting research in the area of microwave passive and active circuits, mobile and satellite base-station RF systems, design of periodic defected transmission lines, and RFIC design. He is a Senior Member of IEEE and a member of the Korea Institute of Electromagnetic Engineering and Science (KIEES). He has authored and co-authored over 170 papers in international journals and conference proceedings.