



Performance of Non Punch-Through Trench Gate Field-Stop IGBT for Power Control System and Automotive Application

Ey Goo Kang[†]

Department of Energy Semiconductor Engineering, Far East University, Eumseong 27601 korea

Received January 22, 2016; Accepted February 8, 2016

In this paper, we have analyzed the electrical characteristics of 1200V trench gate field stop IGBT and have compared to NPT planar type IGBT and NPT planar field stop IGBT. As a result of analyzing, we obtained superior electrical characteristics of trench gate field stop IGBT than conventional IGBT. To begin with, the breakdown voltage characteristic was showed 1,460 V and on state voltage drop was showed 0.7 V. We obtained 3.5 V threshold voltage, too. To use these results, we have extracted optimal design and process parameter and designed trench gate field stop IGBT. The designed trench gate IGBT will use to inverter of renewable energy and automotive industry.

Keywords: IGBT, Trench, Planar, Field-stop, NPT, Power Devices, High Efficiency, High Breakdown Voltage, On-state Voltage drop

1. INTRODUCTION

As energy saving becomes a major social issue, adoption of inverters for distributed power generation, such as photovoltaic, wind, or fuel cell devices, new renewable energy, and energy saving has garnered tremendous interest. This power semiconductor module is a core component of Power Conditioning Units (PCU), industrial inverters, Uninterruptible Power Supplies (UPS), and large-capacity Power This paper investigates a high-efficiency high-voltage Trench Gate Field Stop IGBT, a core component of industrial inverters to raise the energy consumption efficiency of power conditioning unit and motor for distributed power generation photovoltaic, wind, and fuel cell devices.

2. EXPERIMENT METHOD

2.1 Basic design of a 1,200 V Planar type NPT IGBT

The primary matters to consider in designing a 1,200 V Planar type NPT IGBT are (1) the resistivity of wafer and (2) the drift layer thickness of the device to design. For this, an IGBT with a structure as in Fig. 1 was designed with the process conditions found in Table 1.

Table 1. Basic process parameters.

| Area | Process condition |
|-------------------|------------------------------|
| P-base | dose 8.0e13 cm ⁻² |
| P+ Emitter | dose 3.0e15 cm ⁻² |
| N JFET | dose 7.0e11 cm ⁻² |
| N+ Emitter | dose 1.0e16 cm ⁻² |
| P+ collector | dose 1.0e17 cm ⁻² |
| Wafer resistivity | 60 Ωcm |

[†] Author to whom all correspondence should be addressed:
E-mail: keg@kdu.ac.kr

Copyright ©2016 KIEEME. All rights reserved.

This is an open-access article distributed under the terms of the Creative Commons Attribution Non-Commercial License (<http://creativecommons.org/licenses/by-nc/3.0>) which permits unrestricted noncommercial use, distribution, and reproduction in any medium, provided the original work is properly cited.

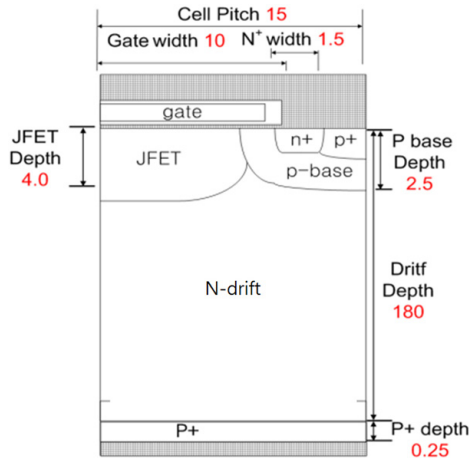


Fig. 1. The structure of Planar NPT IGBT.

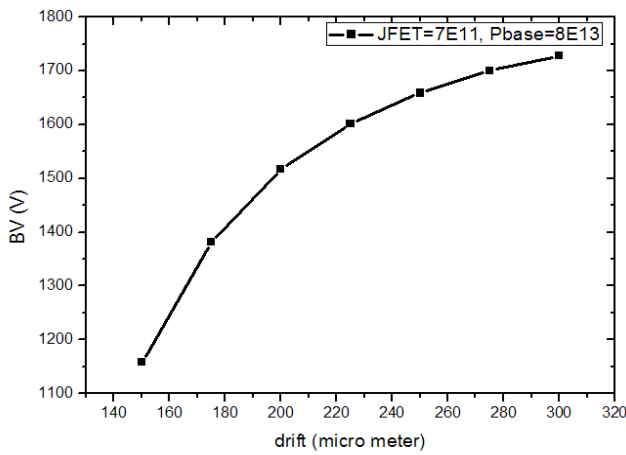


Fig. 2. The Breakdown Characteristics according to Drift lengths of Planar NPT IGBT.

2.2 Breakdown voltage simulation according to drift thickness

As the drift layer thickness increases, the breakdown voltage increases, but at over 200 μm the increase width reduces dramatically. Here, the maximum length of a depletion layer is 157 μm , so smaller lengths a punch-through phenomenon occurs. Besides, as the drift thickness increases, the on-state resistance increases, and can be viewed as a reasonable trade-off.

In order to avoid the punch-through phenomenon and achieve the target breakdown voltage, the ideal drift thickness was determined as 180 μm and the wafer resistivity was determined as 60 Ωcm . At these conditions the target breakdown voltage and low on-state voltage drop, which is suitable for the design of a 1,200 V Planar NPT IGBT. In addition, the structure holds only when the Field-Stop IGBT design has a less than 157 μm drift thickness.

2.3 The electrical characteristics according to dose of P-base and JFET region

A simulation was carried out while adjusting the N JFET and P base dose to $1\text{e}11 \sim 4\text{e}11 \text{ cm}^{-2}$ and $5\text{e}13 \sim 8\text{e}13 \text{ cm}^{-2}$, respectively, in order to optimize the Planar type NPT IGBT after setting the wafer resistivity and drift layer thickness. With the threshold volt-

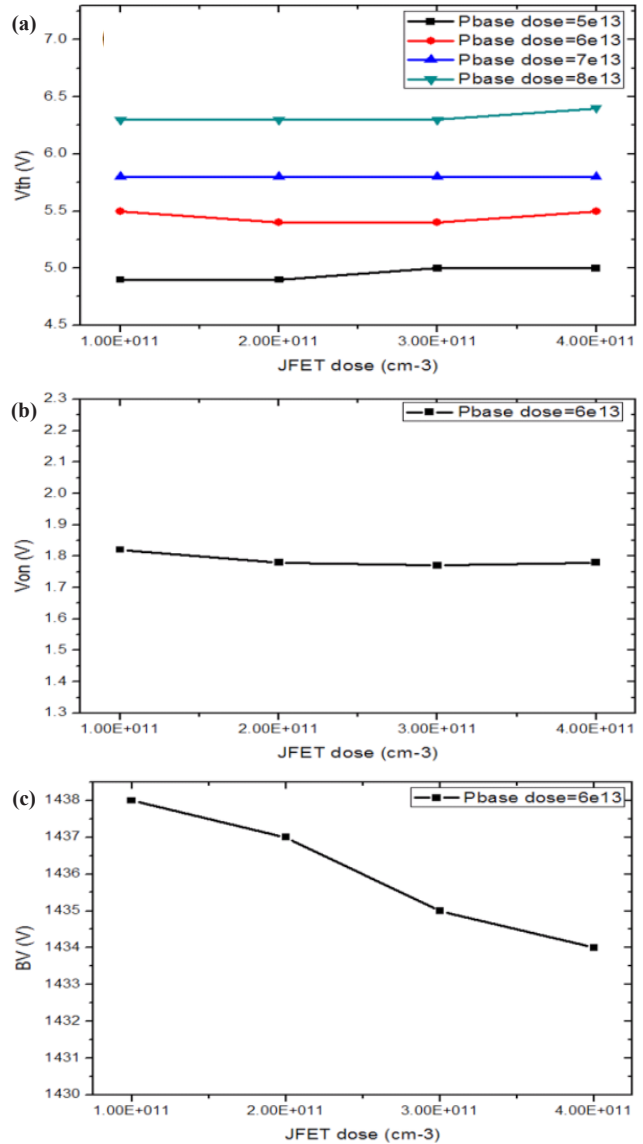


Fig. 3. The electrical characteristics of planar NPT Field Stop IGBT according to JFET dose (a) V_{th} , (b) V_{ce-sat} , and (c) BV .

Table 2. Planar NPT IGBT Final process parameters.

| Area | Process condition |
|------------------|--|
| Wafer | Resistivity 60 Ωcm , Depth 180 μm |
| Cell pitch(half) | 15 μm |
| P-base | Dose 6.5e13cm ⁻² , Depth 2.5 μm |
| P+ Emitter | Dose 5.0e14cm ⁻² , Width 4.9 μm |
| N JFET | Dose 1.0e12cm ⁻² , Depth 4.0 μm |
| N+ Emitter | Dose 5.0e15cm ⁻² , Width 1.5 μm |
| P+ collector | Dose 1.0e17cm ⁻² , Depth 0.5 μm |
| Poly Gate | width 10 μm |

age aimed at about 5.5V, for which the threshold voltage varied according to the JFET and the P-base dose, which was determined as $6\text{e}13 \text{ cm}^{-2}$.

As the JFET dose increases, the resistance in the JFET area decreases, so the on-state voltage drop is expected to reduce, but was found to have a little to no effect. This is due to the JFET resistance is very low since the concentration in the JFET area is high enough. The optimized process variables were set through

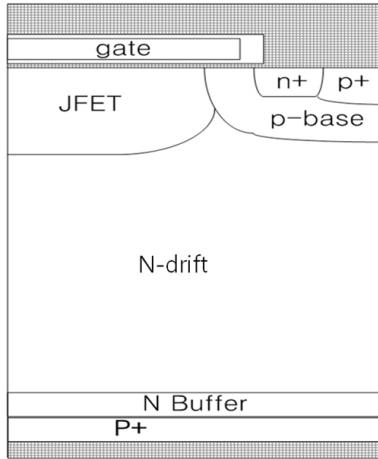


Fig. 4. The structure of planar NPT Field Stop IGBT.

Table 3. Planar NPT IGBT Final process parameters.

| Area | Process parameter |
|--------------|-----------------------------------|
| N Buffer | Depth 2.5 μm |
| | Resistivity 1 Ωcm^2 |
| P+ collector | Dose 8.0e14 cm^{-2} |
| | Depth 0.5 μm |

a simulation on the variables related to the P-base dose, and was confirmed that the threshold voltage was 5.5 V, the on-state voltage drop was 2.35 V (for 100 A), and the breakdown voltage was 1,425 V.

2.4 Basic design of a 1,200 V planar Field Stop IGBT

Based on the 1,200 V Planar type NPT IGBT design technology, the design of a Planar type FS IGBT was executed. The generation of punch-through was hindered by induces the punch-through to occur and induce a sudden drop of electric fields through insertion of N buffer layers via reducing the drift layer thickness of an optimized Planar type NPT IGBT. The inserted N buffer layer was assumed to have a uniform concentration in the simulation, rather than a wafer back process with the thickness was found to be 2.5 μm .

2.5 The electrical characteristics of planar NPT FS IGBT according to N drift thickness

The thickness of the spare drift layer of the previously designed NPT IGBT was 22 μm , thus the thickness of the drift layer was determined to be 157 μm or less to observe an increase in breakdown voltage pursuant to the insertion of N buffers. A trade-off relationship was confirmed so that the breakdown voltage and on-state voltage drop reduce together as the thickness of the N drift layer decreases in concentration and length of the preferably assumed N buffer, and the drift thickness was determined as 110 μm to achieve the target.

2.6 The electrical characteristics of planar NPT FS IGBT according to N buffer thickness and dose and p+ collector dose

The result value of the previous experiment was fixed, and then the thickness of the N buffer was adjusted. As shown in Fig.

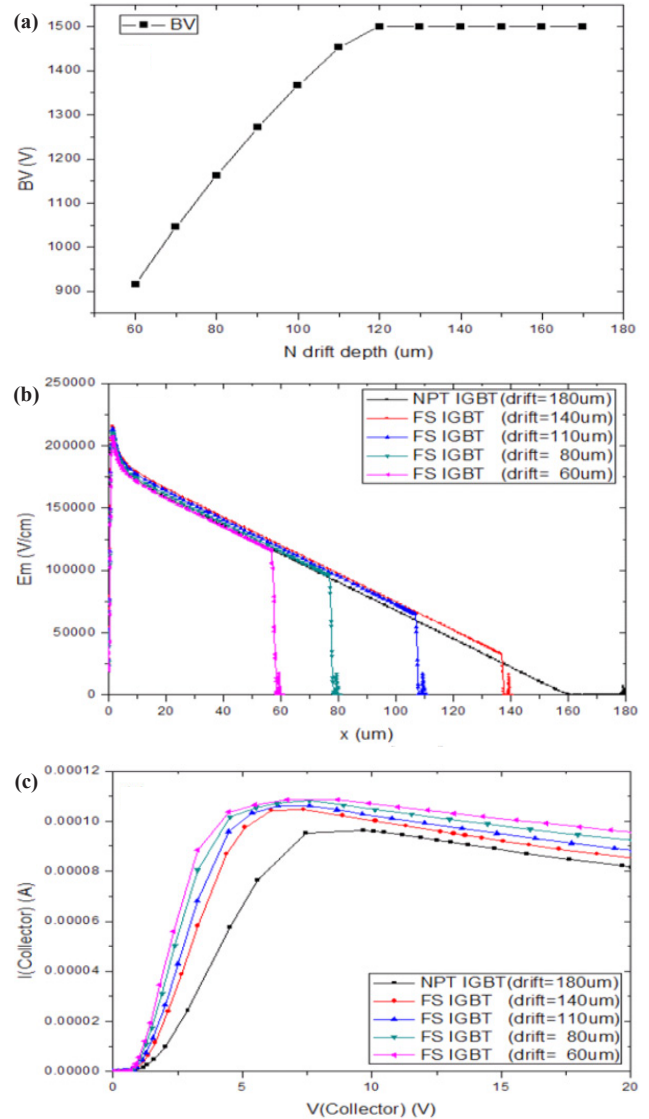


Fig. 5. The electrical characteristics of planar NPT FS IGBT according to drift depth (a) BV, (b) Field-effect, and (c) I-V Characteristics.

(a) and (b), the thickness of the buffer layer does not affect the breakdown voltage but as the thickness of the buffer layer decreases, the on-state voltage drop reduces. As shown in Fig. 5 (c) and (d), the thickness of the buffer layer meets the target breakdown voltage at 0.5, but the on-state voltage drop has a slightly higher value of 1.9 V

After changing the thickness and concentration, the hole insertion efficiency at the P+ collector significantly reduced, the conductivity modulation effect was also reduce, and the on-state voltage drop significantly increased. Accordingly, as a result of changing the P+ collector concentration in a structure of buffer concentration 0.06 Ωcm and buffer thickness 0.5 μm , the on-state voltage drop reduces due to high hole insertion efficiency. However, due to an increase in P+ collector concentration, the thickness of the N buffer layer, the internal charge capacity, the maximum point of the electric field applied to the N buffer layer, and the breakdown voltage reduces. At this time, as shown in Fig. 9, the trade-off optimum point between the breakdown voltage and the on-state voltage drop could be obtained as a result of adjusting the P+ collector concentration, and the concentration and thickness of the low N buffer was applied to

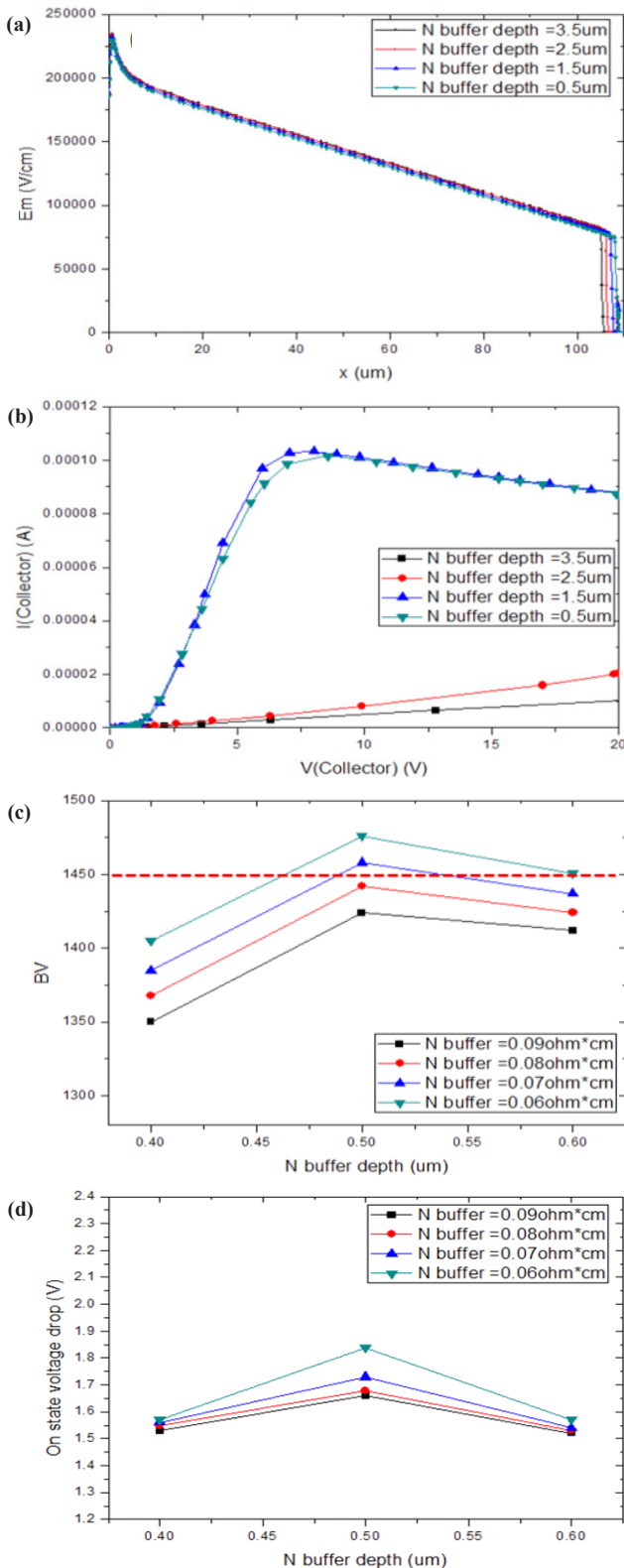


Fig. 6. The electrical characteristics of planar NPT FS IGBT according to Buffer depth and dose (a) Field-effect, (b) I-V Characteristic, (c) BV, and (d) Vce-sat.

obtain optimized properties: the drift thickness of 110 μm , buffer resistivity of 0.03 Ωcm , buffer thickness of 0.5 μm , breakdown voltage of 1,458 V at P+ collector dose $1\text{e}15 \text{ cm}^{-2}$ and on-state voltage drop of 1.55 V.

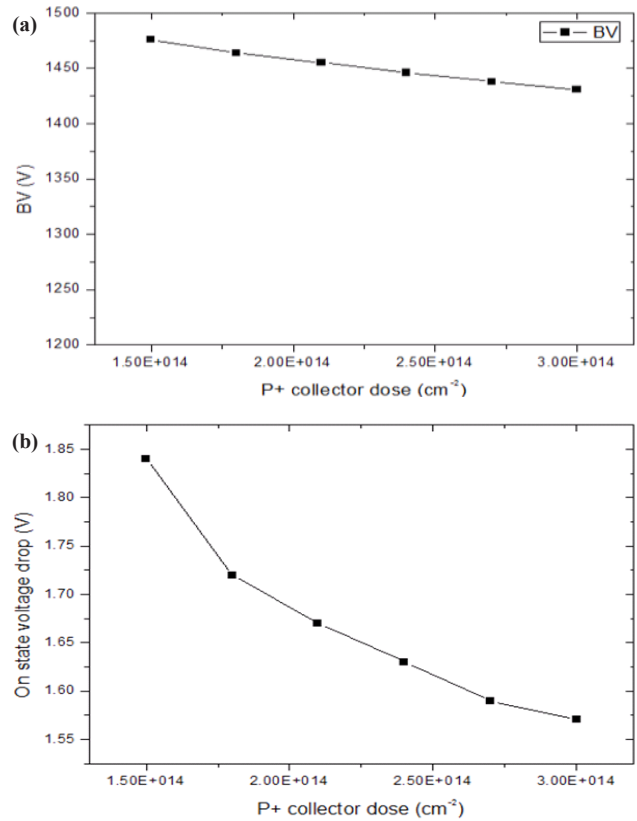


Fig. 7. The electrical characteristics of planar NPT FS IGBT according to p+ collector dose (a) BV and (b) Vce-sat.

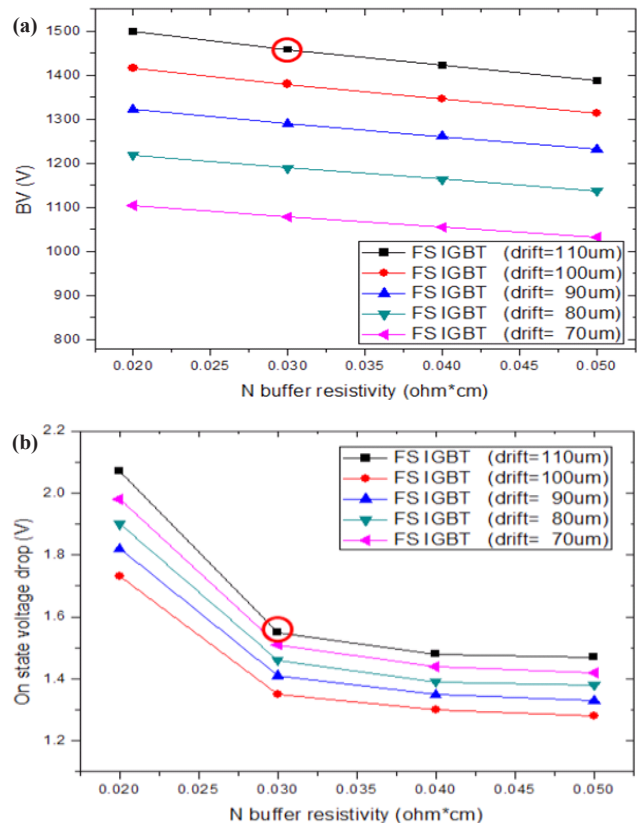


Fig. 8. The electrical characteristics of planar NPT FS IGBT according to N buffer dose and Drift depth (a) BV and (b) Vce-sat.

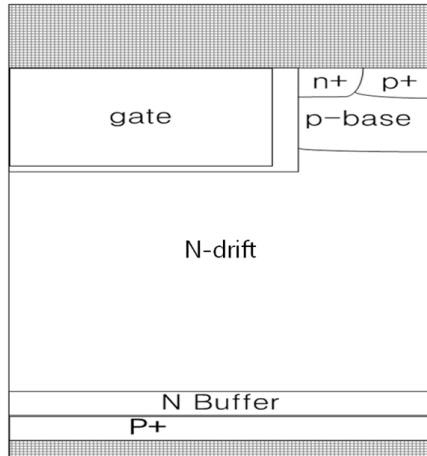


Fig. 9. The Structure of Trench Gate NPT Field Stop IGBT.

Table 4. Planar NPT IGBT Final process parameters.

| Area | Process condition |
|------------|--|
| N Buffer | Dose 1.4×10^{14} cm ⁻² , Depth $0.5 \mu\text{m}$ |
| Wafer | Resistivity $60 \Omega\text{cm}$, Depth $110 \mu\text{m}$ |
| P-Base | Dose 1.3×10^{13} cm ⁻² , Depth $2.9 \mu\text{m}$ |
| P+ Emitter | Dose 5.0×10^{14} cm ⁻² , Width $3.5 \mu\text{m}$ |
| N+ Emitter | Dose 5.0×10^{15} cm ⁻² , Width $1.5 \mu\text{m}$ |

2.7 Design of 1,200 V Trench Gate NPT Field Stop IGBT

Based on the 1,200 V Planar type FS IGBT design technology, a Trench type FS IGBT was designed and the electrical properties of the NPT IGBT and Planar type FS IGBT were compared.

At this time, the threshold voltage was set to 5.5 V, and the P-base dose for this was fixed at 8.0×10^{13} cm⁻². The buffer simulation condition of the Trench type FS IGBT is the same as the condition of the Planar type IGBT. However, the simulation depending on width and length of the trench gate executed and summarized in Table 1. At this time, the on-state voltage drop reduces as the gate depth deepens while the trench gate width remains unchanged. The electric field concentration phenomenon at the bottom of the trench gate strengthens as the gate depth deepens.

3. RESULTS AND ANALYSIS

An optimized structure has been designed for each device, and the comparison results of the electrical properties of each IGBT are shown in Table 8 below. As shown in Table 8, the threshold voltage dropped, the breakdown voltage was high and the Vce-sat reduced as compared to the Planar and Trench.

4. CONCLUSIONS

In this paper, we have analyzed the electrical characteristics of 1,200 V trench gate field stop IGBT and have compared to NPT planar type IGBT and NPT planar field stop IGBT. As a result of analyzing, we obtained superior electrical characteristics of trench gate field stop IGBT than conventional IGBT. To begin with, the breakdown voltage characteristic was showed 1,460 V and on state voltage drop was showed 0.7 V. We obtained 3.5 V threshold voltage, too. To use these results, we have extracted

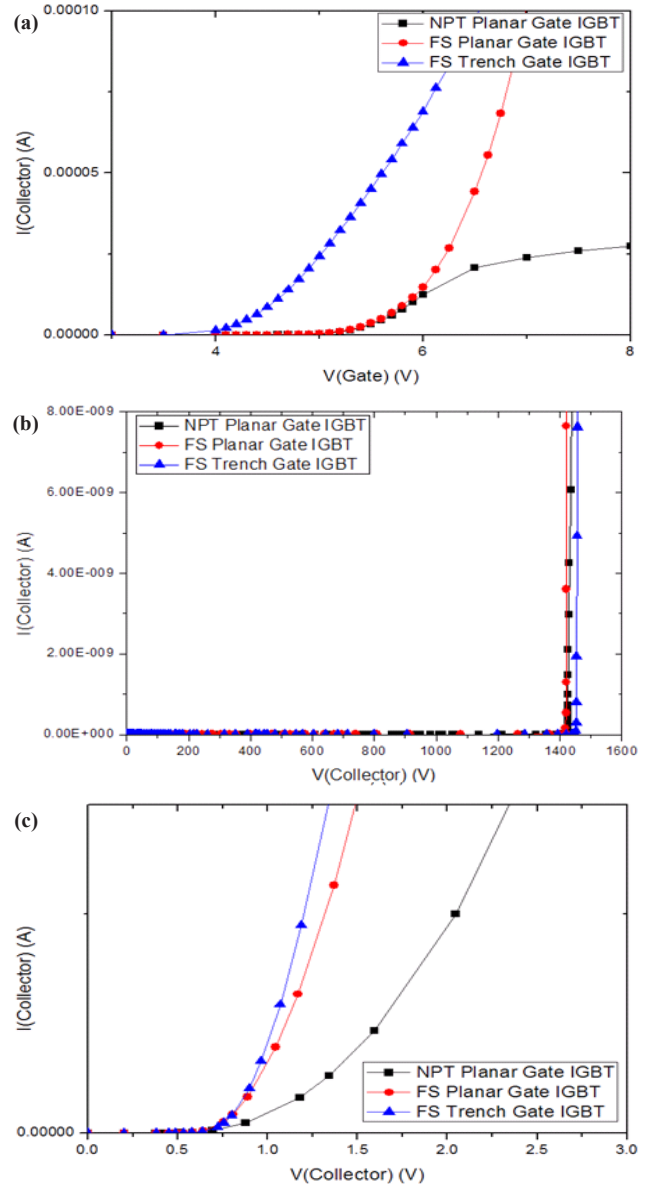


Fig. 10. The electrical characteristics of planar NPT IGBT, Planar FS IGBT and Trench FS IGBT (a) Vth, (b) BV, and (c) Vce-sat.

optimal design and process parameter and designed trench gate field stop IGBT. The designed trench gate IGBT will use to inverter of renewable energy and automotive industry.

REFERENCES

- [1] G. Majumdar and T. Minato, *Power Conversion Conference proceedings*, 355 (2007). [DOI: <http://dx.doi.org/10.1109/pc-con.2007.372992>]
- [2] B. J. Baliga, *Power Semiconductor Devices*, (PWS Publishing Company, Boston, 1996)
- [3] B. Q. Tang, Y. M. Gao, and J. S. Luo, *Solid-State Electronics*, **41**, 1821 (1997). [DOI: [http://dx.doi.org/10.1016/S0038-1101\(97\)00151-2](http://dx.doi.org/10.1016/S0038-1101(97)00151-2)]
- [4] S. M. Sze and G. Gibbons, *Solid-State Electronics*, **9**, 831, (1966). [DOI: [http://dx.doi.org/10.1016/0038-1101\(66\)90033-5](http://dx.doi.org/10.1016/0038-1101(66)90033-5)]
- [5] S. M. Sze, Kwok. K. Ng, "Physics of semiconductor devices", John Wiley & Sons, 2007

- [6] A. G. Chynoweth, *Physical Review*, **109**, 1537 (1958). [DOI: <http://dx.doi.org/10.1103/PhysRev.109.1537>]
- [7] D. C. Sheridan, G. Niu, J. N. Merrett, J. D. Cressler, C. Ellis, and C. C. Tin, *Solid-State Electronics*, **44**, 1367 (2000). [DOI: [http://dx.doi.org/10.1016/S0038-1101\(00\)00081-2](http://dx.doi.org/10.1016/S0038-1101(00)00081-2)]
- [8] G. Charitat, M. A. Bouanane, P. Rossel, *Power Semiconductor Devices and ICs, 1992. ISPSD '92. Proceedings of the 4th International Symposium*, 213 (1992). [DOI: <http://dx.doi.org/10.1109/ISPSD.1992.991268>]
- [9] J. A. Appels, et al, *Philips J. Res.*, **35**, 1 (1980)
- [10] D Jaume, G. Charitat, J. M. Reynes, and P. Rossel, *IEEE Trans. Electron Devices*, **38**, 1681 (1991). [DOI: <http://dx.doi.org/10.1109/16.85167>]
- [11] T. Matsushita, T. Mihara, H. Yamoto, H. Hayashi, M. Okayama, and Y. kawana, *Jap J. Appl. Phys. Suppl.*, **15**, 35 (1976). [DOI: <http://dx.doi.org/10.7567/JJAPS.15S1.35>]
- [12] S. Colak, B. Singer, and E. Stupp, *IEEE Electron Device Letters.*, **EDL_1**, 51, (1980). [DOI: <http://dx.doi.org/10.1109/EDL.1980.25226>]