Current Photovoltaic Research 4(4) 131-139 (2016)
DOI:https://doi.org/10.21218/CPR.2016.4.4.131
pISSN 2288-3274
eISSN 2508-125X

D-UPFC Application as the Series Power Device in the Massive Roof-top PVs and Domestic Loads

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ABSTRACT: This paper shows the series power device in the massive roof-top PVs and domestic loads. D-UPFC as the series power device controls the distribution voltage during voltage rise (or fall) condition. D-UPFC consists of the bi-directional ac-ac converter and the transformer. In order to verify the D-UPFC voltage control, the distribution model is used in the case study. D-UPFC enables the voltage control in the distribution voltage range. Dynamic voltage control from voltage rise and voltage fall conditions is performed. Scaled-down experimental test of the D-UPFC is verified the voltage control and it is well performed without high voltage spikes in the inductive load.

Key words: series power device, distribution-unified power flow controller, bi-directional ac-ac converter, roof-top PV

Nomenclature

V : voltage
D : duty cycle
P : pole transformer capacity
N : turns ratio

subscript

AE-PVC : autonomy-enhanced pv cluster
D-UPFC : distribution-unified power flow controller

1. Introduction

Japan set up the long-term R&D roadmap titled "PV2030" in June 2004. According to this scenario, it is known that mass deployment is expected up to 100 GW totally, more than 40% of which will be brought from residential roof-top PV applications. To make this story realistic, the author proposed "Autonomy-Enhanced PV Cluster" concept[1,2]. Fig. 1 illustrates a basic image of "Autonomy-Enhanced PV Cluster (AE-PVC)" by utilizing power electronic devices and battery storage stations. The former will bring network control functions to improve grid parameters along the community internal grids by utilizing shunt/series active components, meshed network, loop power controller (LPC). The existence of storage devices mainly gives higher degree autonomy control.

To realize 100% PV deployment of PV houses, it is necessary to solve voltage distribution and islanding detection restrictions[1]. This paper focuses on solving the voltage distribution restriction. To compensate voltage rise (or drop), a kind of automatic voltage regulator is introduced as the series power devices, which is called Distribution-Unified Power Flow Controller (D-UPFC)[3]. Fig. 2 gives present and proposed approach of voltage control in the distribution grid[2].

When the voltage rise happens due to reverse power flow, present step voltage regulator (SVR) has narrow allowable voltage window. However, power electronic devices based D-UPFC can have wide allowable voltage window.

D-UPFC voltage control is performed from one of distribution grid side methods. Compared with present distribution grid voltage control methods, it has some advantages. It can control the active power, fast control the distribution voltage using pwm function, linearly controls the distribution voltage during voltage rise (or drop), and it can performs in the bi-directional power flow condition[3].

In this study, the D-UPFC voltage control in the case study is shown. The simulation condition is considered the actual distribution grid as the inductive load. The scaled-down experiment of D-UPFC voltage control is performed.

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Received September 8, 2016; Revised September 13, 2016; Accepted September 25, 2016

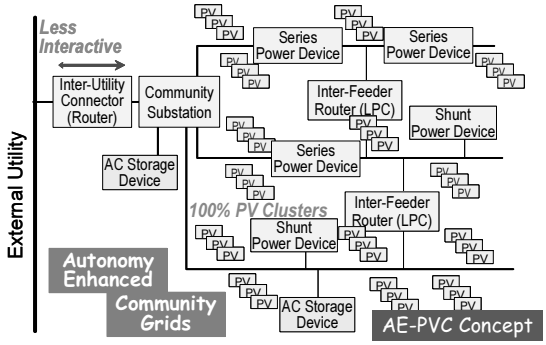
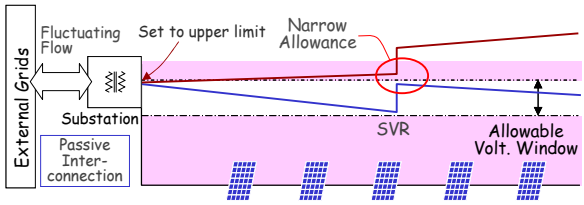
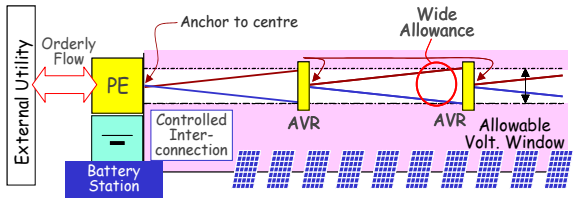


Fig. 1. Autonomy-Enhanced, Community-based PV Cluster Concept by employing active control



(a) Present approach according to existing regulations



(b) Proposed approach which accepts 100% reversal power flow from clustered PV systems

Fig. 2. 2 types concept of the voltage distribution along the grid

2. D-UPFC concept

As mentioned in Fig. 2(b), the D-UPFC controls the distribution grid voltage with the wide voltage window during voltage rise (or fall). The D-UPFC consists of the bi-directional ac-ac converter and the transformer. The transformer supplies a part of pole transformer secondary voltage and the bi-directional ac-ac converter regulates the voltage rise (or fall) in order to match the nominal pole transformer secondary voltage.

2.1 D-UPFC topology

The D-UPFC topology which consists of the bi-directional ac-ac converter and the transformer is shown in Fig. 3[3].

The operation of the D-UPFC topology is the output voltage V_{out} is controlled by the bi-directional ac-ac converter and the transformer. Thus, the equation of this topology can be written as,

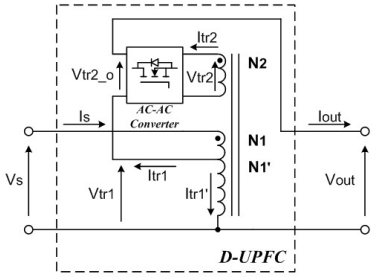


Fig. 3. D-UPFC topology

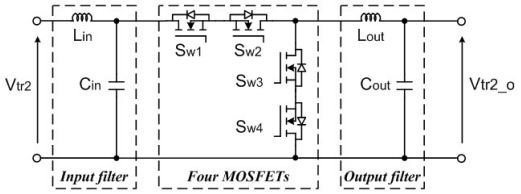


Fig. 4. Bi-directional ac-ac converter circuit

$$V_{out} = V_{tr1} + V_{tr2\_0} \tag{1}$$

The bi-directional ac-ac converter consists of four power MOSFETs, input, and output filters. It provides direct ac to ac conversion and thus, there is no energy storage device. Also, it converts the output voltage always less than input voltage. The bi-directional ac-ac converter circuit is shown in Fig. 4.

This circuit is the same as dc-dc buck converter and thus, its equation can be written as,

$$V_{tr2\_o} = V_{tr2} \times D \tag{2}$$

where, D is duty cycle of the converter.

2.2 Bi-directional ac-ac converter switching patterns

D-UPFC should be operated both forward power flow and reverse power flow condition in order to control voltage rise (or) fall. The transformer of D-UPFC can automatically transfer the ac power during bi-directional power flow condition. Thus, the ac-ac converter of the D-UPFC is required the operation during bi-directional power flow condition. The ac-ac converter with the bi-directional power flow is realized by the switching patterns. The switching patterns of the converter offer safe commutation without high-voltage spikes using intelligent PWM switching patterns. Switching patterns are decided by the polarity of input voltage V_{tr2}. When V_{tr2} is positive, S_{w1} and S_{w3} operate pwm switching, reversely. At the same time, S_{w2} and S_{w4} turn on state. Also, the switching patterns consists of active mode, dead-time mode, and freewheeling mode. If the sign of

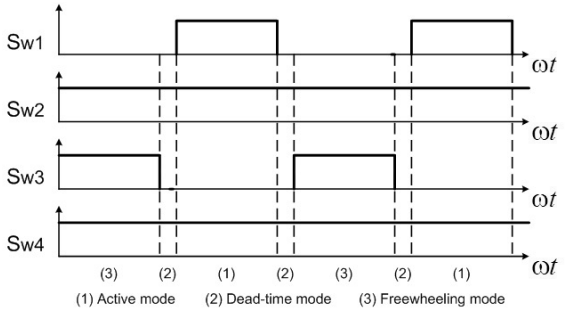


Fig. 5. Bi-directional ac-ac converter switching patterns when V_{tr2} is positive polarity

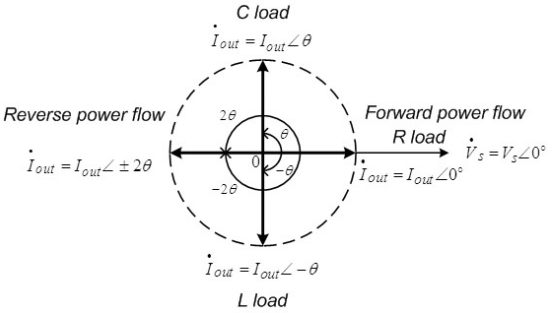


Fig. 6. Phase diagram of D-UPFC input voltage V_s and output current I_{out}

the V_{tr2} is changed, the switching patterns of four switches are reversed. Also, these switching techniques enables the power conversion without high-voltage spikes in the inductive or capacitive load[4]. Fig. 5 shows the ac-ac converter switching patterns.

The bi-directional ac-ac converter switching patterns enable the proper operation in the four-quadrant states. Thus, the phase relation between D-UPFC input voltage V_s and output current I_{out} can be drawn as Fig. 6.

In the forward power flow condition, V_s and I_{out} phase is decided by load power factor condition. If the load consists of resistive, the power factor is 1.0 and thus, the switching patterns of the bi-directional ac-ac converter are divided by V_s polarity. However, the load power factor is not the same as 1.0, which means inductive or capacitive load, the switching patterns of the converter are divided by four-quadrant states depending on V_s and I_{out} polarity.

2.3 Voltage control method and transformer tap relation

In the D-UPFC voltage control method, D-UPFC output voltage V_{out} is always controlled by reference voltage V_{ref_dc}. The D-UPFC control block is shown in Fig. 7.

The V_{ref_dc} is the same as low-voltage distribution grid voltage 202 V. The V_{error} is calculated by V_{ref_dc} and RMS value of

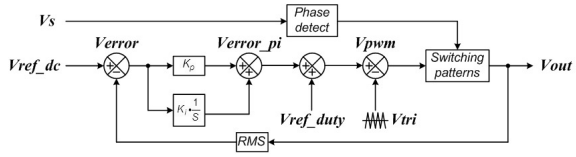


Fig. 7. D-UPFC voltage control block

V_{out}. The V_{error_pi} is calculated through PI compensator. The maximum duty cycle of bi-directional ac-ac converter is 1.0 and the reference duty cycle V_{ref_duty} is 0.5 during normal condition. If the voltage rise condition occurs, the value of V_{pwm} is decreased. Reversely, the value of V_{pwm} is increased during voltage fall condition. In the PWM control, the switching frequency of triangle signal is 20 kHz. D-UPFC input voltage V_s phase is detected and then used in the switching patterns.

As shown in Fig. 3, the transformer tap of D-UPFC is decided by bi-directional ac-ac converter in this paper. According to the Japan's voltage range regulations, the secondary voltage range of the pole transformer is 202±20 V (101±6 V). Considering the pole transformer voltage range, the ac-ac converter controls the distribution voltage ±20 V in this paper. The transformer tap of D-UPFC can be calculated by power relation of D-UPFC input and output[5].

$$P_s = P_{tr1} + P_{tr2} \tag{3}$$

where, P_s is total input power, P_{tr1} is output power in winding N_1', P_{tr2} is output power in winding N_2

$$V_s \times I_s = (V_{tr1} \times I_{tr1}) + (V_{tr2} \times I_{tr2}) \tag{4}$$

since, the transformer tap N_1 is 1.0, N_1' is 0.9, N_2 is 0.2 and the normal duty cycle D of bi-directional ac-ac converter is 0.5.

$$V_{tr1} = \frac{9}{10}V_s \;\; V_{tr2} = \frac{2}{10}V_s, \;\; \text{and} \;\; I_{tr2} = D \times (I_{out} = I_{tr1})$$

Equ. (4) can be rewritten as,

$$V_s \times I_s = \frac{9}{10}(V_{tr1} \times I_{tr1}) + \frac{2}{10}(V_{tr2} \times 0.5 \times I_{out}) \tag{5}$$

$$V_s \times I_s = \frac{9}{10}(V_{tr1} \times I_{out}) + \frac{1}{10}(V_{tr2} \times I_{out}) \tag{6}$$

$$I_s = I_{out} \tag{7}$$

D-UPFC input and output power relation is shown through the equ. (1) to (7). Here, D-UPFC only handles the output voltage during voltage rise (or fall) in the distribution grid.

3. Case study

3.1 Distribution model

In order to verify the D-UPFC voltage control during voltage rise (or fall) in the distribution grid, the distribution model is proposed[4]. The distribution model is assumed to be residential area in Japan. Total feeders of the distribution model are 8. However, the distribution model for simulation is considered only 1 feeder. The distribution model using ATP-EMTP simulation tool is shown in Fig. 8.

The length of one feeder is 10 km and the pole transformer is located in every 2 km. The T_{r1} pole transformer of is connected with 20 roof-top PVs and they are divided 4 nodes. 5 roof-top PVs are connected to each node. The distance of each node is 40 m. The distance between each node and each roof-top PV house is 15 m. The maximum output power of each roof-top PV is 3 kW. The distribution model parameters are shown in Table 1.

D-UPFC parameters in the distribution model are shown in Table 2.

D-UPFC is installed after the secondary side of the T_{r1} pole transformer and the D-UPFC reference voltage V_{ref_dc} is 202 V. The input filter reduces the input voltage and curent harmonics. At the same way, the output filter reduces the output voltage and current harmonics from 20 kHz of switching frequency[4]. In the reverse power flow, the present input filter and output filter is reversed.

In the case study, voltage fall and voltage rise conditions are simulated. In order to simulate voltage fall, the load consumption power is changed. The pole transformer secondary capacity is calculated according to the load current,

Table 1. Distribution model parameters

Substation	66 kV / 6.6 kV, 20 MVA
Pole transformer	6.6 kV / 202 V(101 V), 50 kVA
6.6 kV line impedance (Z_1 to Z_5)	0.626 + j0.754 [Ω/2 km]
202 V line impedance (Z_{d1} to Z_{d3})	0.025 + j0.02 [Ω/40 m]
Lead-in wire impedance (Z_{i1} to Z_{i20})	0.0552 + j0.037 [Ω/20 m]
Each PV system capacity	3 [kW]

Table 2. D-UPFC parameters

V_{ref_dc}	202 V	C_{in} & C_{out}	50 [μF]
$N_1 : N_1' : N_2$	1 : 0.9 : 0.2	PI gain	K_p=0.025
V_{ref_duty}	0.5		K_i=0.001
L_{in} & L_{out}	50 [μH]	Switching fre.	20 [kHz]

$$P_{capacity} = V_{secondary} \times I_{secondary} \quad (8)$$

where, $P_{capacity}$ is the pole transformer secondary capacity, $V_{secondary}$ is the pole transformer secondary voltage, $I_{secondary}$ is total load current.

The voltage fall curve from node A_1 to A_4 which is caused by load power change is shown in Fig. 9. The value of voltage difference through the node A_1 to A_4 is due to the distribution line impedance. The voltage of node A_4 decreases more than other nodes. D-UPFC voltage control during voltage fall condition from node A_1 to A_4 is shown in Fig. 10(a) to (d), respectively. Here, the pole transformer secondary capacity is 70%, which is already shown in Fig. 9. Through the voltage fall simulation, the D-UPFC controlled the distribution voltage to the reference voltage at the installation node.

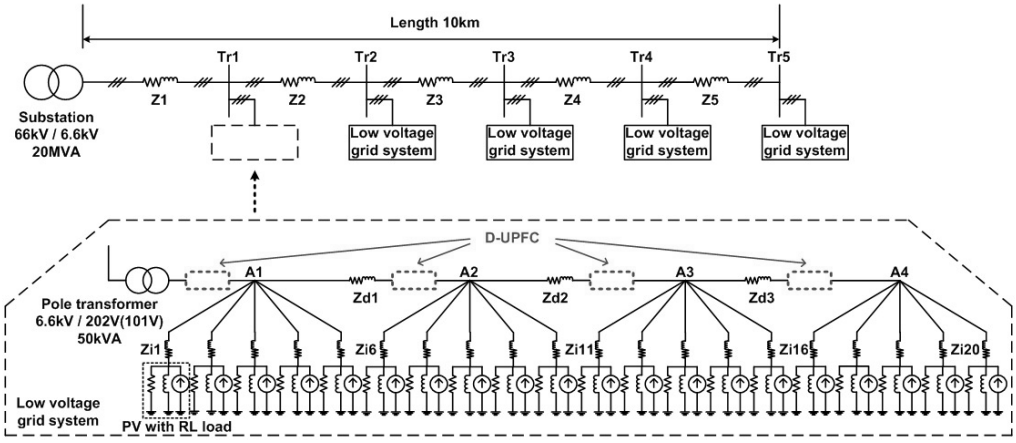


Fig. 8. Distribution model with D-UPFC installation

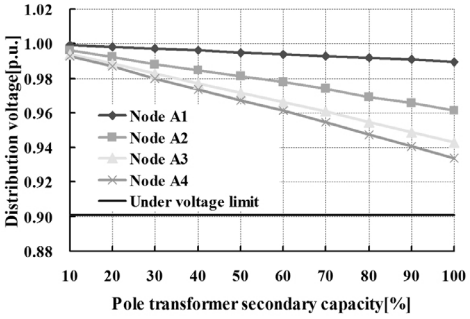


Fig. 9. Voltage fall curve due to load power change

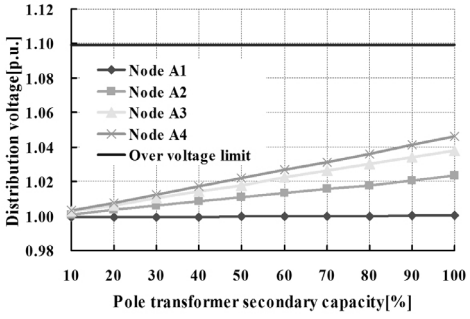


Fig. 11. Voltage rise curve due to reverse power flow from clustered PV system

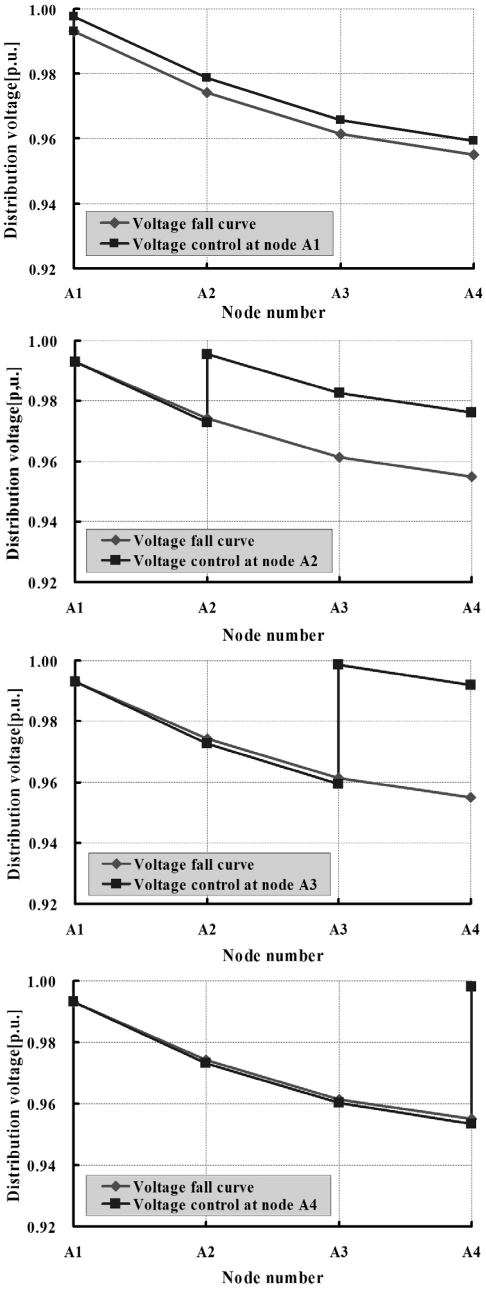


Fig. 10. D-UPFC voltage control during voltage fall at the installation site from A1 to A4

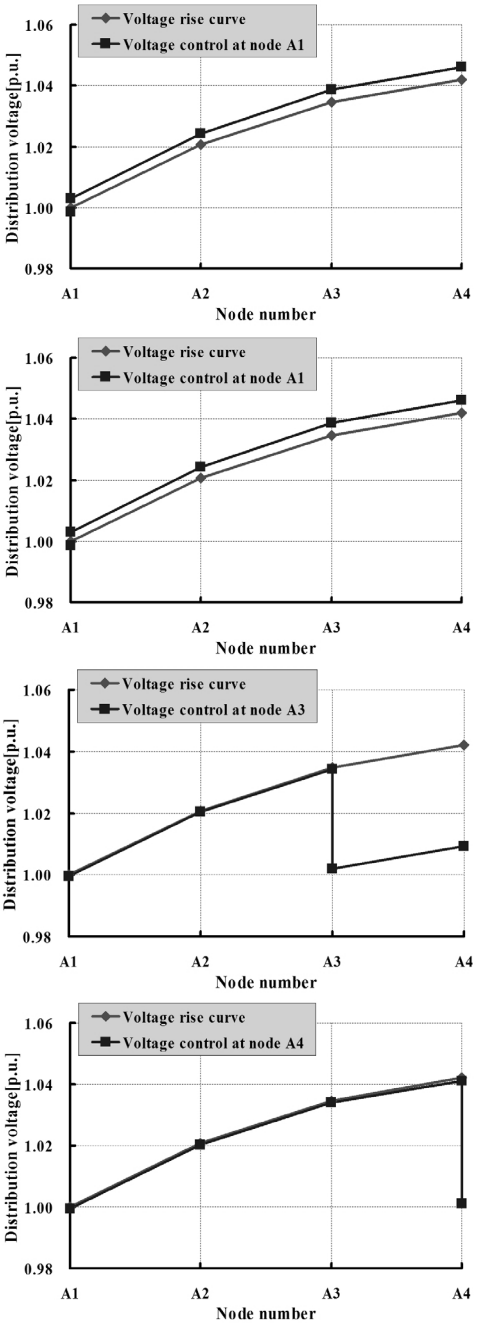
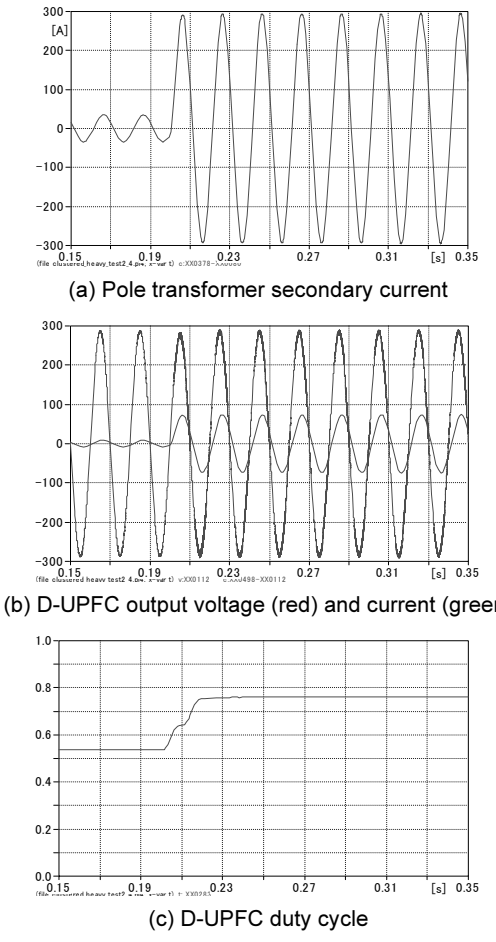


Fig. 12. D-UPFC voltage control during voltage rise at the installation site from A1 to A4

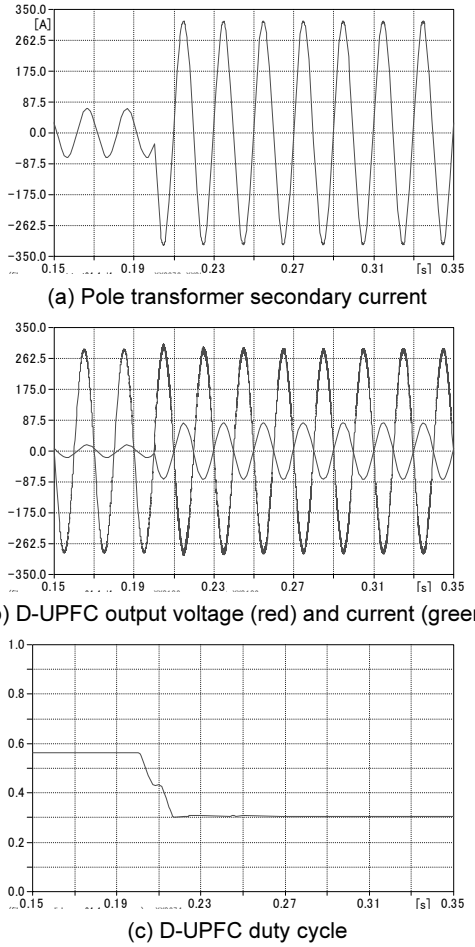


(a) Pole transformer secondary current

(b) D-UPFC output voltage (red) and current (green)

(c) D-UPFC duty cycle

Fig. 13. Dynamic test of D-UPFC during voltage fall condition



(a) Pole transformer secondary current

(b) D-UPFC output voltage (red) and current (green)

(c) D-UPFC duty cycle

Fig. 14. Dynamic test of D-UPFC during voltage rise condition

In the voltage rise condition, reverse power flow from PV systems is occurred. Here, the pole transformer secondary capacity is calculated as,

$$P_{capacity} = V_{secondary} \times (I_{total\_pv} - I_{secondary}) \quad (9)$$

where, $P_{capacity}$ is the pole transformer secondary capacity, $V_{secondary}$ is the pole transformer secondary reference voltage, I_{total_pv} is total PV output current, $I_{secondary}$ is total load current.

Distribution voltage rise due to increasing PV output current is shown in Fig. 11. As shown in equ. (9), total load current is fixed to 10% of pole transformer secondary capacity. The maximum $P_{capacity}$ is 50 kVA, which is shown in Table 2. In the Fig. 11, the voltage of node 4 increases more than other node voltages.

Fig. 12 shows the D-UPFC voltage control at the installation node These results are performed when the pole transformer secondary capacity is 90%. D-UPFC controls the distribution voltage to reference voltage in Fig. 12(b) to (d). However, the D-UPFC do not control exactly the distribution voltage at node A_1 in Fig. 12(a).

3.2 Dynamic voltage control

In the D-UPFC dynamic voltage control, voltage fall and rise conditions are simulated. The voltage fall condition is simulated under the 70% of pole transformer secondary capacity. The D-UPFC controls the distribution voltage at node A_4 which is already shown in Fig. 10(d). In the Fig. 13(a), the load consumption power increases to 70% at 0.2 s. Thus, the pole transformer current also increases.

At this time, the D-UPFC controls the voltage fall during 1 cycle from the voltage fall phenomenon. Fig. 13(b) shows the D-UPFC output voltage V_{out} and output current I_{out} at node A_4. Before the D-UPFC control, V_{out} was under 0.96 p.u. However, V_{out} was about 1.0 p.u. after D-UPFC control from 0.22 s. The D-UPFC duty cycle during voltage fall condition is shown in Fig. 13(c). Before the voltage control, the normal duty cycle of the D-UPFC is 0.5. However, the duty cycle of the D-UPFC

Table 3. The parameters of the experimental set

V_s	10 V, 50 Hz	PI gain	K_p=1, K_i=0.25
$N_1 : N_1' : N_2$	1 : 0.7 : 0.6	Switching fre.	20 [kHz]
V_{ref_duty}	0.5	V_{pv}	11 V, 50 Hz
L_{in} & L_{out}	2.6 [mH]	R_{line}	20 [Ω]
C_{in} & C_{out}	3 [μF]	L_{load}	0.26 [H]

increases during voltage fall condition.

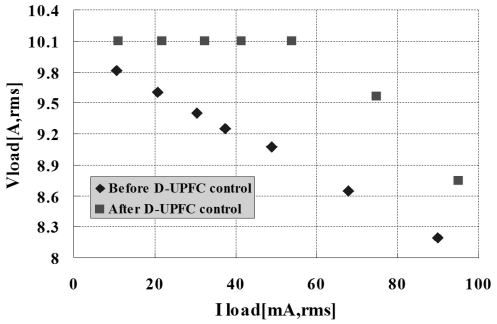
The dynamic test of D-UPFC during voltage rise condition is shown in Fig. 14. As shown in Fig. 14(a), the PV output power is 70% of the maximum pole transformer capacity from 0.2 s. D-UPFC output voltage V_{out} and current I_{out} are shown in Fig. 14(b). D-UPFC controls the rising voltage, which was 1.04 p.u. after 0.22 s. Fig. 14(c) shows the D-UPFC duty cycle and the D-UPFC decreases the duty cycle during voltage rise condition.

Through the dynamic test simulation of D-UPFC, D-UPFC using PWM control enables the fast voltage control which is less than 2 cycles.

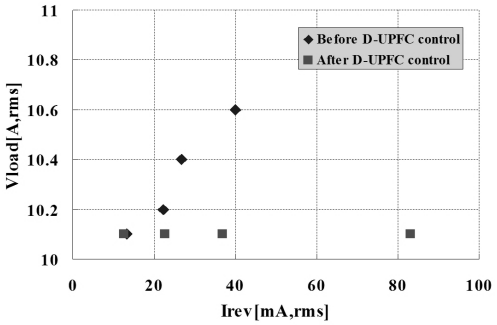
4. Experiment

In the experimental study, D-UPFC voltage control during voltage rise and voltage fall conditions is performed. The experimental set is shown in Fig. 15. Here, two bipolar sources are used. One of them is voltage source and the other is current source considering reverse power flow. The parameters of the experimental set are given in Table 3.

Fig. 16(a), (b) show the before and after D-UPFC control during voltage fall and voltage rise condition, respectively. In the voltage fall test, the load is considered only resistive load. The value R_{load} is changed 470 Ω to 90 Ω and thus, the load current I_{load} increases. Consequently, the load voltage V_{load} decreases due to R_{load}. In the experimental result of Fig. 16(a),



(a) Voltage fall condition



(b) Voltage rise condition

Fig. 16. Experimental results of before and after D-UPFC control

V_{load} decreases 9.8 V to 8.2 V. The D-UPFC controls the V_{load} to 10.1 V until I_{load} 54 mA. However, if the value of I_{load} is larger than 54 mA, V_{load} which is controlled by D-UPFC decreases because the value of transformer inner dc resistance of D-UPFC increases.

In the voltage rise test from Fig. 16(b), the R_{load} is fixed to 1 kΩ and the current source inner resistance R_{inner} is changed 47 Ω to 4.7 Ω. The current source voltage V_{pv} is 11V. Thus, the reverse power flows to the voltage source V_s. the reverse power flow from the current source increases. I_{rev} increases from 13 mA to 50 mA with the voltage rise. D-UPFC controls the V_{load} to 10.1 V during reverse power flow condition. Here, I_{rev} dramatically increases at V_{load} 10.6 V.

In the Fig. 17, the bi-directional ac-ac converter output

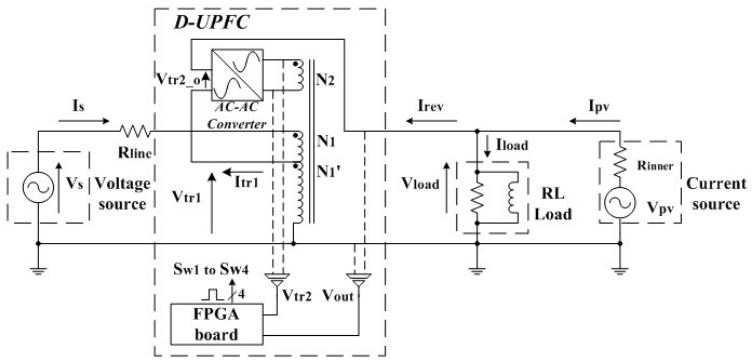
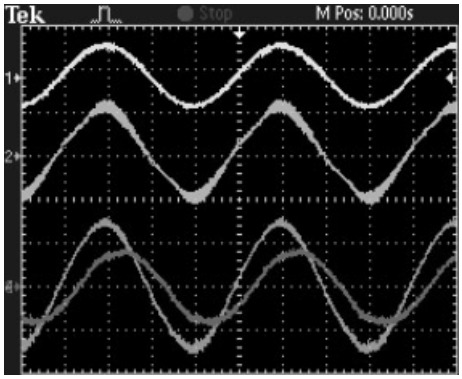


Fig. 15. Experimental set of D-UPFC control

(a) V_{tr2_o} and V_{load} waveforms during voltage fall condition
(Scale: 2 V/div., 20 V/div., 50 ms/div.)

(b) V_{tr2_o} and V_{load} waveforms during voltage rise condition
(Scale: 2 V/div., 20 V/div., 50 ms/div.)

Fig. 17. D-UPFC voltage control waveforms during voltage fall and voltage rise condition



(a) V_s, V_{tr2_o}, I_{load}, and V_{load} waveforms
(Scale: 20 V/div., 5 V/div., 500 mA/div., 10 V/div., 5 ms/div.)

(b) Voltage waveforms from S_{w1} to S_{w4}
(Scale: 5 V/div., 10 V/div., 5 V/div., 10 V/div., 25 μs/div.)

Fig. 18. D-UPFC voltage control waveforms in the inductive load condition

voltage V_{tr2_o} and load voltage V_{load} waveforms are shown when the voltage fall and rise conditions occur, respectively.

In the Fig. 17(a), V_{out} is 9.1 V before the D-UPFC control which is mentioned in Fig. 22(a). However, D-UPFC controls the V_{out} to 10.1 V after 20 cycles from the trigger start. In the Fig. 17(b), the V_{out} was 10.8 before the D-UPFC control and it is controlled to 10.1 V after 20 cycles from the trigger start.

Fig. 18 shows the D-UPFC voltage, current, and each switch voltage waveforms during inductive load condition. In this test, the R_{load} is 47 Ω and L_{load} is 0.26 H from the load parameters. The power factor is 0.86.

Fig. 18(a) shows the D-UPFC input voltage V_s, the ac-ac converter output voltage V_{tr2_o}, the load current I_{load}, and the load voltage V_{load}. During this waveform, I_{load} phase lags the V_{load} phase is confirmed due to the inductive load condition.

Fig. 18(b) shows each switch voltage of the bi-directional ac-ac converter when the converter input voltage V_{tr2} is positive polarity. The voltages from S_{w1} to S_{w4} are performed with the PWM control.

5. Conclusions

This paper shows the series power device in the massive roof-top PVs and domestic loads. D-UPFC as the series power device controls the distribution voltage during voltage rise (or fall) condition.

D-UPFC consists of the bi-directional ac-ac converter and the transformer. D-UPFC is performed in the reverse power flow condition as well as forward power flow condition using the converter switching patterns.

In order to verify the D-UPFC voltage control, distribution model is used in the case study. Through the D-UPFC voltage control simulation, D-UPFC enables the voltage control in the distribution voltage range. Dynamic voltage control from voltage rise and voltage fall conditions is performed. D-UPFC rapidly controls the voltage using the PWM control.

The scaled-down experiment of D-UPFC voltage control is performed. D-UPFC controls the load voltage during voltage fall and voltage rise test. D-UPFC is well performed without high-voltage spikes in the inductive load condition.

In the future study, D-UPFC protection methods from the short-circuit and ground fault from the distribution grid are necessary.

Acknowledgments

This works was supported by the financial support of the Korea Energy Agency (No. G10201605010004).

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