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Charge Trapping Mechanism in Amorphous Si-In-Zn-O Thin-Film Transistors During Positive Bias Stress

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The mechanism for instability under PBS (positive bias stress) in amorphous SIZO (Si-In-Zn-O) thin-film transistors was investigated by analyzing the charge trapping mechanism. It was found that the bulk traps in the SIZO channel layer and the channel/dielectric interfacial traps are not created during the PBS duration. This result suggests that charge trapping in gate dielectric, and/or in oxide semiconductor bulk, and/or at the channel/dielectric interface is a more dominant mechanism than the creation of defects in the SIZO-TFTs.

Keywords: Oxide based semiconductors, Oxide TFT, Indium zinc oxide, DC bias stress

1. INTRODUCTION

Highly TAOSs (transparent amorphous oxide semiconductors) based TFTs (thin-film transistors) have attracted considerable interest in applications including future displays, optoelectronics, and electronics [1,2]. Especially, it has been anticipated that TAOSs such as GIZO (Ga-In-Zn-O) [3], HIZO (Hf-In-Zn-O) [4], ZTO (Zn-Sn-O) [5], SIZO (Si-In-Zn-O) [6], etc. can resolve the innate drawbacks of current Si based TFTs including the poor carrier mobility of amorphous Si TFTs and the non-uniformity in electrical performances of low temperature processed poly-Si TFTs [7]. The TAOSs based TFTs provide better uniformities and electrical properties than those of the poly-Si based TFTs, since the crystallites that make the TFTs inhomogeneous are not included in the TAOSs and a high electron mobility can be achieved even in amorphous state due to the high symmetry of the s-orbitals of heavy metal ions [8]. In order to improve the stability under positive/negative bias stress, illumination stress, and temperature stress, the fundamental mechanisms for the threshold voltage shift have been intensively investigated for GIZO- [8] and HIZO-TFTs [9]. Recently, it was reported that a high field effect mobility and good stability were achieved by a very small amount of SIZO (Si incorporated In-Zn-O) TFTs fabricated at a very low process temperature of 150℃ [10]. The post annealing process with low temperature will facilitate the application of a SIZO oxide semiconductor to flexible displays. Considering the 20% change in the luminance owing to a threshold voltage shift of 0.1 V [11], much improvement can still be made in the stability in SIZO-TFTs. In earlier works, we reported that the instability under PBS (positive bias stress) of the SIZO-TFTs is attributed to the charge trapping in the semiconductor bulk and at the semiconductor/dielectric interface by extracting the density of states in TFTs using the SIZO layer [10]; the possibility of defect creation during the PBS in the SIZO-TFTs remained unproven. Thus, we first need to prove that the defect creation model is not a dominant mechanism in the SIZO-TFTs.

In this paper, the mechanism for instability of 1 wt.% Si incorporated SIZO-TFT under PBS was investigated from the charge trapping mechanism [12]. The variation of the subgap (DOSs) within the energy range from the conduction band edge (E_c) to 1.6 eV below E_c was not observed during the PBS tests. This demonstrates that the defect creation in the active channel layer bulk and at the channel/dielectric interface is not responsible for the positive VTH shift under the PBS in the SIZO-TFT.

2. EXPERIMENTAL

The direct current sputtering method was used to deposit 150 nm thick Mo gate electrode on glass substrate at room tempera-

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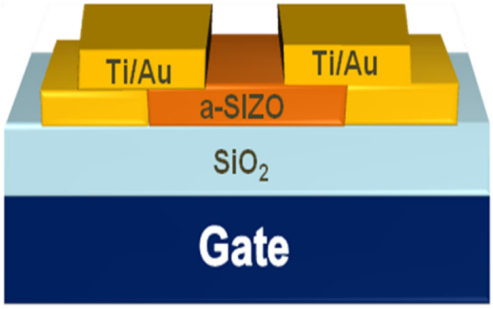

Fig. 1. Schematic of an a-SIZO (Si-In-Zn-O) thin film transistor.

ture, and 200 nm thick SiNx as a gate insulator was then grown by plasma enhanced chemical vapor deposition (PECVD). An amorphous 1 wt.% Si incorporated SIZO (In_2O_3:ZnO=3:1) active layer of 30 nm in thickness was prepared by radio frequency magnetron sputtering at room temperature. The SIZO active layer and source/drain (S/D) electrodes were well defined by the conventional photolithography and wet etching process, in which the SIZO film and S/D were etched and patterned by 99% diluted hydrochloric acid and acetone as an etchant, respectively. Ti/Au (10 nm/60 nm) as source/drain electrodes were deposited by electron beam evaporation and thermal evaporation method, respectively. The well-defined channel length and width of the SIZO-TFTs were 200 μm and 100 μm, respectively as shown in Fig. 1.

The SIZO-TFTs were annealed at 150℃ for 1 h in a thermal furnace with N2 ambience. All the transfer curves and stability tests were evaluated using a semiconductor parameter analyzer (HP 4145B) probe system in a dark and vacuum state of < 2×10^{-2} Torr. The bias for the stress tests was kept at a gate voltage of 20 V and a drain to source voltage of 10.1 V for 1,500 s at room temperature.

3. RESULTS AND DISCUSSION

Figure 2 shows the evolution of the transfer curves obtained at the drain to source voltage (V_{DS}) of 0.1 V from amorphous SIZO-TFT under PBS with increasing stress time.

The PBS was kept at a gate to source voltage (V_{GS}) of 20 V and V_{DS}=10.1 V for 1,500 sec. The transfer curves shifted toward the positive direction with increasing stress time. As a result, the threshold voltage (V_{TH}) shift for the SIZO-TFT was about 5.7 V for 1,500 sec. The square root of the drain to source current (I_{DS}) as a function of V_{GS} at V_{DS}=0.1 V is almost linear, as shown in Fig. 3.

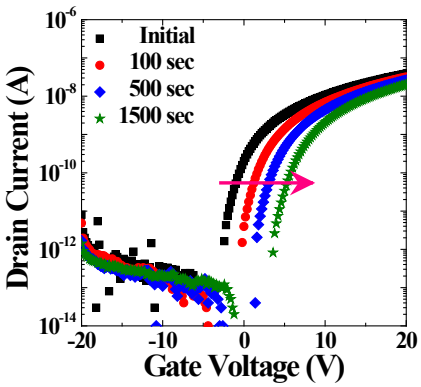

Fig. 2. Evolution of transfer curves.

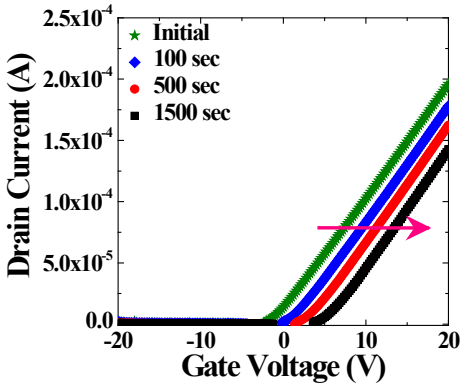

Fig. 3. Square root plots of I_{DS} with PBS duration.

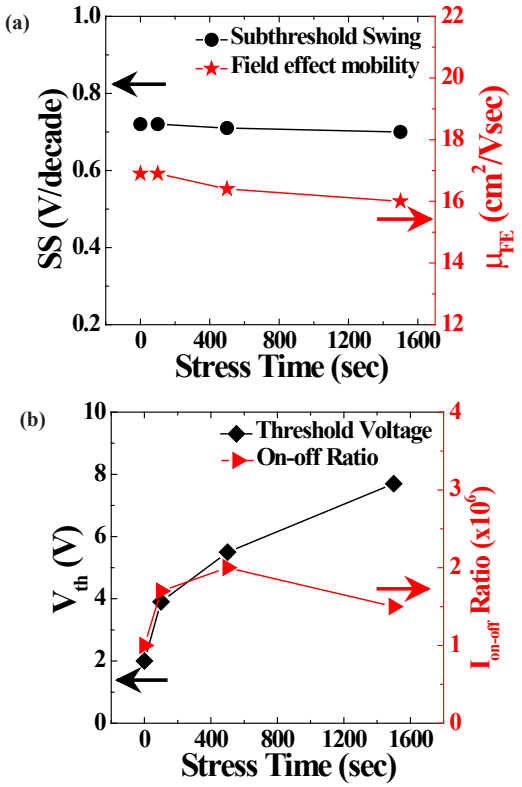

Fig. 4. (a) SS and μ_{FE} and (b) V_{th} and I_{on-off} ratio as a function of stress time.

Thus, the V_{TH} values were extracted by fitting a straight line to the plot [13]. The variations of electrical parameters such as subthreshold swing (SS), field effect mobility (μ_{FE}), VTH, and on-off current ratio (I_{on-off} ratio) with stress time are shown in Figs. 4(a) and 4(b).

The SS and μ_{FE} values only slightly changed with increasing stress duration. It has been reported that the positive shift in V_{TH} during PBS can be explained using a simple charge trapping or defect creation model [14-16]. In the case of SIZO-TFT, the SS values did not significantly change during PBS duration. This result suggests that charge trapping in gate dielectric, and/or in oxide semiconductor bulk, and/or at the channel/dielectric interface is a more dominant mechanism than the creation of defects in the SIZO-TFTs [3,14].

4. CONCLUSIONS

In summary, by directly analyzing SS values and V_{th} shift in SIZO-TFTs during PBS tests, it was found that the V_{TH} shift under PBS tests originated by charge trapping in the SIZO channel bulk and/or at the channel/dielectric interface rather than due to defect creation. This was confirmed by the constant SS value and reduced hysteresis loop as PBS time increased. In the case of SIZO-TFT, the SS values did not significantly change during the PBS duration. This result suggests that charge trapping in the gate dielectric, and/or in oxide semiconductor bulk, and/or at the channel/dielectric interface is a more dominant mechanism than the creation of defects in the SIZO-TFTs.

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