High-Performance Amorphous Multilayered $ZnO-SnO_2$ Heterostructure Thin-Film Transistors: Fabrication and Characteristics

Su-Jae Lee, Chi-Sun Hwang, Jae-Eun Pi, Jong-Heon Yang, Chun-Won Byun, Hye Yong Chu, Kyoung-Ik Cho, and Sung Haeng Cho

Multilayered $ZnO-SnO_2$ heterostructure thin films consisting of ZnO and SnO_2 layers are produced by alternating the pulsed laser ablation of ZnO and SnO_2 targets, and their structural and field-effect electronic transport properties are investigated as a function of the thickness of the ZnO and SnO_2 layers. The performance parameters of amorphous multilayered $ZnO-SnO_2$ heterostructure thin-film transistors (TFTs) are highly dependent on the thickness of the ZnO and SnO_2 layers. A highest electron mobility of 43 $cm^2/V\cdot s$, a low subthreshold swing of a 0.22 V/dec, a threshold voltage of 1 V, and a high drain current on-to-off ratio of 10^{10} are obtained for the amorphous multilayered ZnO(1.5 nm)-SnO_2(1.5 nm) heterostructure TFTs, which is adequate for the operation of next-generation microelectronic devices. These results are presumed to be due to the unique electronic structure of amorphous multilayered ZnO-SnO_2 heterostructure film consisting of ZnO, SnO_2, and ZnO-SnO_2 interface layers.

Keywords: ZnO, SnO_2, oxide semiconductor, heterostructure, transistor.

Manuscript received June 22, 2014; revised July 20, 2015; accepted Aug. 10, 2015.

This work was supported by the ICT R&D Program of MSIP/IITP (10041416, the core technology development of light and space adaptable energy-saving I/O platform for future advertising service).

Su-Jae Lee (corresponding author, leesujae@etri.re.kr), Chi-Sun Hwang (hwang-cs@etri.re.kr), Jae-Eun Pi (jepi@etri.re.kr), Jong-Heon Yang (delmo@etri.re.kr), Chun-Won Byun (cwbyun@etri.re.kr), Hye Yong Chu (hychu@etri.re.kr), Kyoung-Ik Cho (kicho@etri.re.kr), and Sung Haeng Cho (helloshcho@etri.re.kr) are with the Information & Communications, Core Technology Research Laboratory, ETRI, Daejeon, Rep. of Korea.

I. Introduction

Thin-film transistors (TFTs) based on wide bandgap amorphous oxide semiconductors, including zinc tin oxide (ZTO), indium gallium zinc oxide (IGZO), indium zinc oxide, and indium zinc tin oxide have been intensively studied in the field of thin-film electronics during the past decades [1]–[7], and are rapidly approaching commercialization as a replacement for amorphous Si in high-performance electronics applications, such as active-matrix organic light-emitting diodes, active-matrix liquid-crystal displays, and flexible displays [7]. In particular, IGZO is one of the most promising channel materials because of its high carrier mobility, good TFT performance, low processing temperature, excellent environmental stability, and high transparency. Thus far, there have been significant attempts to find a new oxide semiconductor as an alternative to indium/gallium-based semiconducting oxides, owing to their rarity, high cost, and toxicity. Still, for TFTs and next-generation microelectronic device applications with low power consumption and higher performance, it is necessary to develop new eco-friendly semiconducting oxide materials exhibiting better transistor properties; that is, higher mobility, a smaller subthreshold swing (ss), a higher ratio of on-to-off drain current (I_{on}/I_{off}), and longer stability. Multilayer thin films have been widely studied because their properties are different from those of conventional thin films and bulk materials owing to the two-dimensional film and high-density interface. Since the recent observation of high-mobility two-dimensional electron gas

© 2015 ETRI

(2DEG) at the interface between the two insulating oxides in a $LaTiO_3/SrTiO_3$ heterostructure [8], a high mobility 2DEG behavior has been seen in semiconductor ZnO-based ZnO/ $Zn_{1-x}Mg_xO$ heterostructures. Thus far, several studies regarding the formation of 2DEG and the performance of field-effect transistors (FETs) with a single crystalline or polycrystalline semiconducting ZnO/MgZnO heterostruture have been carried out [9]–[12]. K. Koike and others reported high-performance ZnO-based FETs that were designed to take advantage of a high-mobility electron channel formed in the ZnO/ZnMgO heterostructure, and demonstrated a transconductance of 0.7 mS/mm with a very high field-effect mobility of 140 $cm^2/V \cdot s$ at room temperature [9]. Such interfacial electron gases in a two-oxide heterostructure can be used to design innovative oxide electronic devices. Thus, the electronic structure of a two-oxide heterointerface is important for its stability, function, and improved performance in many devices. Among the ZnO-based semiconducting oxides, the binary ZnO-SnO_2 systems that possess high electron conductivity and high electron mobility have currently attracted significant attention as low-cost indium/gallium-free alternative transparent conducting and amorphous semiconducting oxide materials for applications in many devices, such as transparent electrodes for solar cells, electronics, flat panel displays (FPDs), sensors, photocatalysts, and the active channel layer of TFTs [3]–[4], [13]. ZnO and SnO_2 are generic n-type semiconductors with wide band gaps of 3.2 eV and 3.6 eV, respectively. ZnO and SnO_2 have different crystal structures; namely, wurtzite and rutile structures, respectively. In addition, they also have different semiconducting properties. Multilayered ZnO-SnO_2 heterostructure thin films consisting of two ZnO and SnO_2 layers that are expected to have an unusual property owing to the formation of unusual charge states at the interface, which are inaccessible in conventional thin films and bulk materials, may be realized, which will enhance the efficiency and performance of many electronic and optical devices. Thus, one motive of this study is to observe the effects of a high-mobility two-dimensional electron channel in multilayer ZnO-SnO_2 heterostructure TFTs such as a 2DEG in a heterointerface.

In this work, multilayered ZnO-SnO_2 heterostructure thin films were produced by alternating the pulsed laser ablation of ZnO and SnO_2 targets, and their structural and field-effect electronic transport properties were investigated as a function of the thickness of the ZnO and SnO_2 layers.

II. Experiments

Multilayered ZnO-SnO_2 heterostructure films were grown by the alternating deposition of ZnO and SnO_2 layers using pulsed laser deposition (PLD) on SiO_2/Si and pre-patterned source-drain (ITO)/gate insulator (Al_2O_3)/gate electrode (ITO)/glass substrates. After a base pressure of lower than 1×10^{-6} Torr was achieved, the ZnO and SnO_2 targets were ablated with a KrF excimer laser ($\lambda = 248$ nm) at a laser energy density of 2 J/cm^2 and a pulsed laser frequency of 2 Hz. The deposition process was carried out at room temperature under an oxygen pressure of 30 mTorr, and then annealed at 350°C in air. The crystallographic structure, microstructures, and elemental composition analysis of the multilayered ZnO-SnO_2 heterostructure films were investigated using glancing-angle X-ray diffraction (GXRD), a Cs-corrected scanning transmission electron microscope (STEM), and an electron dispersive spectroscopy (EDS) embedded in the STEM, respectively. To investigate the field-effect electronic transport properties of multilayered ZnO-SnO_2 heterostructure thin films, field-effect TFTs were fabricated, which have a bottom gate TFT configuration. A lithographically patterned 150 nm-thick indium tin oxide (ITO) film on a glass substrate was used as the bottom gate electrode (BG). A 176 nm-thick Al_2O_3 film as a gate insulator (GI) was deposited at a temperature of 150°C by means of atomic layer deposition (ALD) with trimethylaluminum [TMA, $Al(CH_3)_3$] as precursors and H_2O as the oxidant. A 150 nm-thick ITO as a source–drain (S/D) electrode was deposited by DC sputtering at room temperature, and then annealed at 200°C. After ITO (S/D) patterning, 30 nm-thick multilayered ZnO-SnO_2 heterostructure films, as a channel layer, were deposited using a shadow mask by PLD. The channel width (W) and length (L) were 40 µm and 20 µm, respectively. The field-effect transport properties were measured at room temperature in air using a Keithley 4200 semiconductor parameter analyzer.

III. Results and Discussion

The crystalline phase formation of multilayered ZnO-SnO_2 heterostructure thin films was analyzed using GXRD. Figure 1 shows the GXRD pattern of a 350°C annealed multilayered ZnO-SnO_2 heterostructure film stacked onto 1.5 nm-thick ZnO and 1.5 nm-thick SnO_2 layers grown on a SiO_2/Si substrate. The total thickness of the film is 114 nm. The film exhibited no diffraction peaks related to the hexagonal wurtzite ZnO or tetragonal rutile SnO_2 phases, and exhibited only a broad diffraction peak, which indicates that the film is in an amorphous phase. These results indicate that ZnO-SnO_2 film has an amorphous multilayered heterostructure, consisting of amorphous ZnO and SnO_2 layers.

Figure 2(a) shows a high-resolution cross-sectional STEM image of a multilayered ZnO-SnO_2 heterostructure film grown on a SiO_2/Si substrate and annealed at 350°C. The film has a multilayer heterostructure in which the ZnO and SnO_2 layers

http://dx.doi.org/10.4218/etrij.15.0114.0743

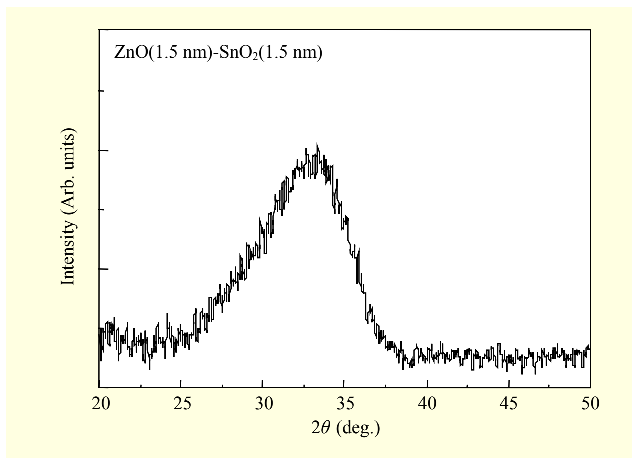

Fig. 1. GXRD patterns of multilayered ZnO(1.5 nm)-SnO_2(1.5 nm) heterostructure thin film grown on SiO_2/Si substrate.

are stacked periodically, and do not show any crystallinity. The thickness of the ZnO and SnO_2 layers was observed to be about 2.0 nm. The interface between the ZnO layer and SnO_2 layer cannot be clearly discerned. The inset of Fig. 2(a) shows the selected area electron diffraction (SAED) patterns of the film, which exhibited only broad diffuse diffraction rings, indicating the characteristics of an amorphous phase. Based on the XRD, STEM, and SAED results, we can confirm that multilayered ZnO-SnO_2 films annealed at 350°C have an amorphous heterostructure consisting of amorphous ZnO and SnO_2 layers. The chemical composition of the amorphous multilayered ZnO-SnO_2 heterostructure film was analyzed using an elemental line profile of EDS embedded in the STEM. Figure 2(b) shows the EDS results obtained for the direction normal to the surface. The inset in Fig. 2(b) is a bright field STEM image. It shows only peaks for oxygen, zinc, and tin elements, which show periodic peaks corresponding to ZnO and SnO_2 layers.

To investigate the field-effect electronic transport properties of amorphous multilayered ZnO-SnO_2 heterostructure thin films, the bottom-gate TFTs were fabricated and electrically characterized at room temperature. To study how the thickness of the ZnO and SnO_2 layers influences the transistor properties, the amorphous multilayered ZnO-SnO_2 heterostructure films acting as channel layers were deposited by varying the thickness of the ZnO and SnO_2 layers. The following films were prepared: ZnO(0.5 nm)-SnO_2(0.5 nm), ZnO(1.0 nm)-SnO_2(1.0 nm), ZnO(1.5 nm)-SnO_2(1.5 nm), ZnO(2.0 nm)-SnO_2(2.0 nm), ZnO(2.5 nm)-SnO_2(2.5 nm), and ZnO(3.0 nm)-SnO_2(3.0 nm). For example, in the multilayered ZnO(1.5 nm)-SnO_2(1.5 nm) heterostructure film, the thickness of the ZnO and SnO_2 layers was 1.5 nm. To obtain an active channel layer with a total thickness of 30 nm, 1.5 nm-thick ZnO and SnO_2 layers were alternately deposited ten times, and stacked to a

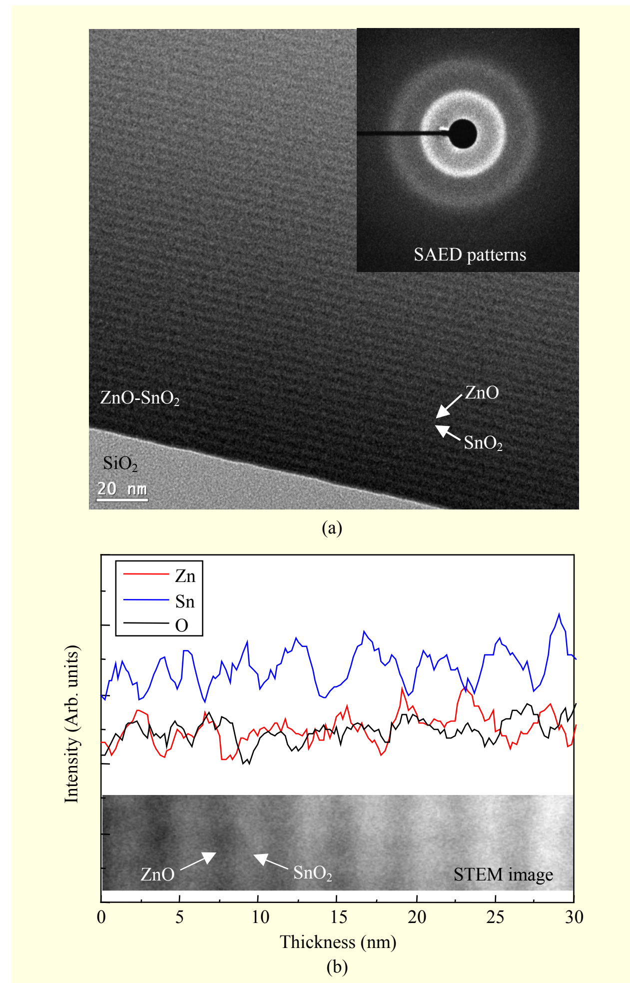

Fig. 2. (a) High-resolution cross-sectional STEM images and (inset) SAED patterns, and (b) elemental line profile of EDS for multilayered ZnO-SnO_2 heterostructure film grown on SiO_2/Si substrate.

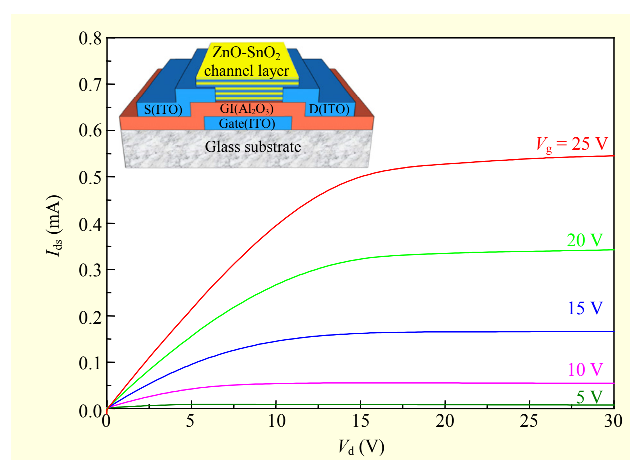

Fig. 3. Representative drain current (I_{ds}) vs. drain–source voltage (V_d) output curves of amorphous multilayered ZnO (1.5 nm)-SnO_2(1.5 nm) heterostructure TFTs, and (inset) schematic layout of fabricated TFT structure.

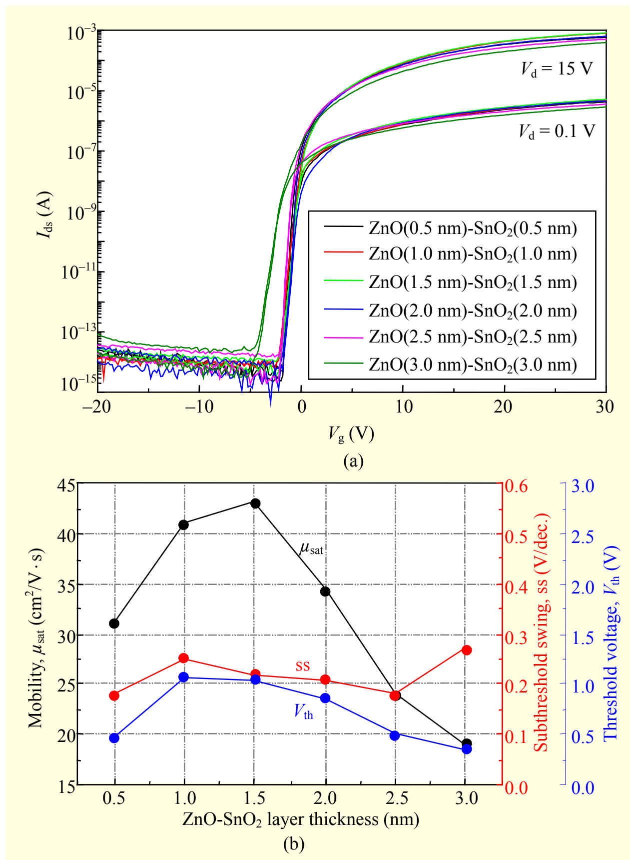

Fig. 4. (a) Transfer I_{ds}–V_g characteristics of amorphous multilayered ZnO–SnO$_2$ heterostructure TFTs with various ZnO and SnO$_2$ layer thicknesses, and (b) performance parameters including saturation mobility (μ_{sat}), subthreshold swing (ss), and threshold voltage (V_{th}) of TFTs as function of ZnO and SnO$_2$ layer thicknesses.

total of 20 layers. Figure 3 shows the representative drain current versus drain-to-source voltage (I_{ds}–V_d) output curves for a transistor with an amorphous multilayered ZnO(1.5 nm)-SnO$_2$(1.5 nm) heterostructure film channel at various gate voltages (V_g). The inset in Fig. 3 shows a schematic layout of the fabricated bottom-gate TFT structure. The n-type transistor behavior with a pinch-off and drain current saturation can clearly be seen from the output curve, which indicates that the electron transportation in the active channel is totally controlled by the gate and drain voltages as in conventional metal–oxide–semiconductor FETs.

The field-effect electronic transport properties of the amorphous multilayered ZnO-SnO$_2$ heterostructure thin films were investigated as a function of the ZnO and SnO$_2$ layer thickness. Figure 4(a) shows the transfer characteristics of the drain current versus gate voltage (I_{ds}–V_g) at drain voltages (V_d) of 0.1 V and 15 V of amorphous multilayered ZnO-SnO$_2$ nanostructure TFTs for various ZnO and SnO$_2$ layer thicknesses.

The total thickness of the ZnO-SnO$_2$ channel layer is 30 nm. All of the TFTs show typical transfer curves of well-behaved transistors. The TFT with the ZnO(1.5 nm)-SnO$_2$(1.5 nm) channel layer exhibits the highest drain on-current (I_{on}) at V_d of 0.1 V and 15 V, and at V_g of 30 V. The drain on-current (I_{on}) shows a clearly decreasing trend with increasing ZnO and SnO$_2$ layer thicknesses. The drain off-current (I_{off}) is in the range of 10^{-13} A to 10^{-15} A for all TFTs, which is below the maximum level of 10^{-12} A for an FPD [5]. The drain current on-off ratio (I_{on}/I_{off}) derived from the transfer curve for a V_d of 15 V was as high as approximately 10^{10} for all TFTs, which is a superior property compared with those of the other reports for amorphous ZTO TFTs (approximately 10^8) [3]–[4], [13]–[15]. These very low off currents and high on-off ratio may result from a small number of channel interface traps and mobile ions in an amorphous multilayered ZnO-SnO$_2$ heterostructure film. In addition, the turn-on voltage, which is the gate voltage at the onset of the initial sharp increase in current in the transfer curve, was in the range of 0 V to –1.5 V except for the ZnO(3.0 nm)-SnO$_2$(3.0 nm) transistor, which was negatively shifted (–3 V). The negative V_{on} shift is attributed to the increasing of free carrier concentration at the thicker ZnO and SnO$_2$ layers, which contributes to the channel conductivity. The performance parameters of the TFTs, including the field-effect saturation mobility (μ_{sat}) and the threshold voltage (V_{th}), were calculated from the transfer curves in the saturation region using $I_{ds} = (WC_i/2L)\mu_{sat}(V_g-V_{th})^2$, where W and L are the channel width and length, respectively; C_i is the capacitance per unit area of the Al$_2$O$_3$ gate insulator, and V_{th} is the threshold voltage. The saturation mobility (μ_{sat}) was obtained through the transconductance in the saturation region of the I_{ds}–V_g curves for a V_d of 15 V. The threshold voltage (V_{th}) was determined from the interception with the V_g axis of the slope of the $I_{ds}^{1/2}$ versus V_g plot. In addition, the subthreshold swing $(\mathrm{ss} = \mathrm{d}V_g / \mathrm{d}(\log I_{ds})[\mathrm{V/decade}])$ was extracted from the linear part of the log (I_{ds}) versus V_g plot. Figure 4(b) shows the extracted saturation mobility (μ_{sat}), threshold voltage (V_{th}), and subthreshold swing (ss) as a function of the ZnO and SnO$_2$ layer thicknesses. The thickness of the ZnO and SnO$_2$ layers clearly influences the mobility of the transistors. It can be seen that the mobility is largely dependent on the ZnO and SnO$_2$ layer thickness in the channel layer. The mobility increased with the increased thickness of the ZnO and SnO$_2$ layers at up to 1.5 nm, and then significantly decreased with further thickness increases. The highest saturation mobility of 43 cm^2/V·s was observed for the amorphous multilayered ZnO(1.5 nm)-SnO$_2$(1.5 nm) heterostructure TFTs. This value is larger than those reported for conventional TFTs with an

http://dx.doi.org/10.4218/etrij.15.0114.0743

amorphous ZTO channel layer [3]–[4], [13]–[15]. It is speculated that the high mobility of the TFTs is due to the effect of the interface layer related to a high-mobility electron channel formed in a ZnO-SnO_2 heterostructure. Three ZnO, SnO_2, and ZnO/SnO_2 interface channels in amorphous multilayered ZnO-SnO_2 heterostructure TFTs can be formed. The cause of the decrease in mobility at the thicker ZnO and SnO_2 layers might be understood as the ZnO and SnO_2 layers playing a role as the dominant active channel in the TFTs, and that the number of ZnO-SnO_2 interface layers decreased with an increase in the ZnO and SnO_2 layer thicknesses at the same channel thickness of 30 nm. These results indicate that the mobility of the TFTs can be controlled by optimizing the thickness of the ZnO and SnO_2 layers. The subthreshold swing (ss) is an important parameter for determining the quality of a TFT. As shown in Fig. 4(b), the ss did not show a specific trend according to the thickness of the ZnO and SnO_2 layers, and showed a value ranging from 0.18 V/dec. to 0.27 V/dec. for all transistors. These values are comparable or better than those reported for ZTO transistors [3]–[4], [13]–[15]. The ss value is related to the total density of the trap states (N_t) in the bulk channel layer (N_{bulk}) and at the interface between the channel/dielectric layer (N_{it}). From the ss, the density of the trap states (N_t) can be calculated using $N_t = N_{bulk} + N_{it} = [\{(q \times ss)/k_B T\} - 1]C_i/q$, where q, k_B, T, and C_i are the electron charge, the Boltzmann constant, absolute temperature, and capacitance of the dielectric layer, respectively [16]–[18]. The calculated trap-charge density (N_t) of the TFTs has a small value of 4.83×10^{11} cm^{-2} to 8.44×10^{11} cm^{-2}. In spite of the high mobility of the TFTs, a low subthreshold swing for all transistors is attributed to the low density of the trap states in the ZnO, SnO_2, and ZnO-SnO_2 interface channel layer and at the interface between the channel and dielectric layer. In addition, the threshold voltage (V_{th}), corresponding to the V_g for which an accumulation layer is formed did not show a specific dependence on the thickness of the ZnO and SnO_2 layers. The threshold voltage V_{th} has positive values between 0.35 V and 1.1 V for all transistors, indicating that the amorphous multilayered ZnO-SnO_2 heterostructure TFTs operate in enhancement mode on a positive bias.

Figure 5(a) shows the transfer I_{ds}–V_g characteristics of amorphous multilayered ZnO-SnO_2 heterostructure TFTs with various ZnO layer thicknesses for a fixed SnO_2 layer thickness (1.5 nm). The I_{on} showed a decreasing trend with increasing ZnO layer thickness. The minimum I_{off} was generally in the range of 10^{-13} A to 10^{-14} A, which is below the maximum level of 10^{-12} A. The I_{on}/I_{off} ratio derived from the transfer curves for V_d of 15 V was as high as approximately 10^{10} for all transistors. The turn-on voltage (V_{on}) was in the range of 0 V to –1 V except for the ZnO(1.0 nm)-SnO_2(1.5 nm) transistor, which was negatively shifted (–2.4 V). Figure 5(b) shows the extracted field-effect saturation mobility (μ_{sat}), subthreshold swing (ss), and threshold voltage (V_{th}) as a function of the ZnO layer thickness with a fixed SnO_2 layer thickness. The μ_{sat} increased to a peak value of 43 cm^2/V·s at ZnO(1.5 nm)-SnO_2(1.5 nm) TFTs, and then significantly decreased at a higher thickness of the ZnO layer. It can be seen that the mobility is largely dependent on the ZnO layer thickness in the channel layer. The subthreshold gate swing (ss) did not show a specific trend according to the thickness of ZnO for a fixed SnO_2 layer thickness, and showed a value ranging from 0.17 V/decade to 0.27 V/decade for all transistors. In addition, the threshold voltage (V_{th}) did not show a specific dependence on the thickness of ZnO for a fixed SnO_2 layer thickness, which has positive values between 0.36 V and 1.35 V for all transistors. Variation in the ZnO layer thickness with a fixed SnO_2 layer thickness clearly influenced the electrical

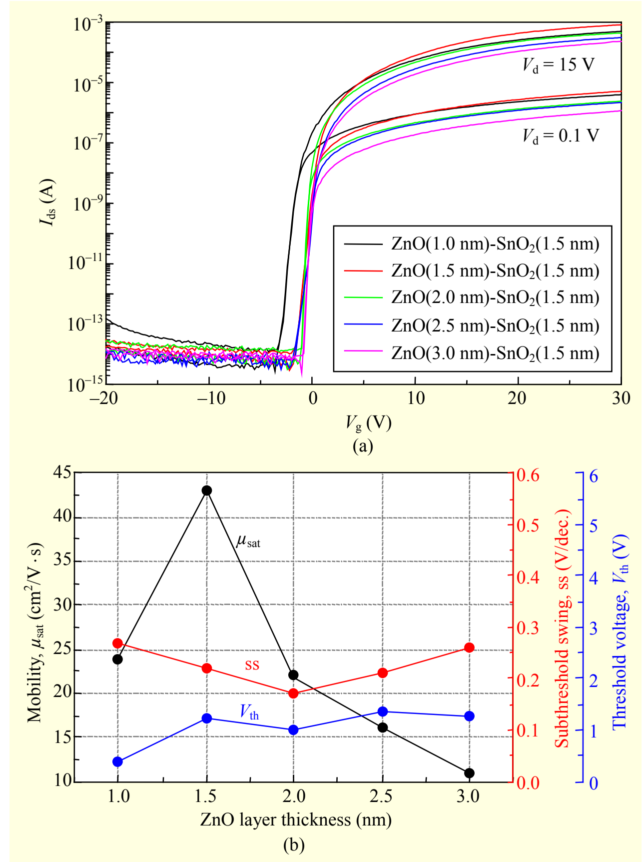

Fig. 5. (a) Transfer I_{ds}–V_g characteristics of amorphous multilayered ZnO-SnO_2 heterostructure TFTs with various ZnO layer thicknesses for fixed SnO_2 layer thickness (1.5 nm), and (b) performance parameters including saturation mobility (μ_{sat}), subthreshold swing (ss), and threshold voltage (V_{th}) of TFTs as function of ZnO layer thickness for 1.5 nm thick SnO_2 layer.

parameters of the transistors. Several investigations have demonstrated that the mobility of ZTO TFTs depends on the Zn/Sn composition ratio in active materials. M.G. McDowell and others reported a decreasing trend of mobility with a decrease in the Zn/Sn ratio in a film formed using a sputtering method [15]. Recently, J.H. Heo and others reported on ZTO TFTs grown by repeating a deposition cycle of ZnO and SnO_2 layers using ALD [4]. It was shown that the mobility of ALD-based ZTO TFTs can be increased by increasing the number of ZnO layer deposition cycles with a constant SnO_2 layer thickness; it was concluded that a higher Zn content leads to a higher mobility when the Zn/Sn ratio is larger than one. Our results show that mobility decreases rapidly with an increase in the thickness of the ZnO layer, which contradicts the conclusions of previous works [4], [15] reporting that the mobility was found to increase with an increase in the Zn/Sn ratio. The thickness of the ZnO layer in a ZnO-SnO_2 heterostructure channel significantly impacts on the electronic transport properties of the TFT. Based on these observations, it was concluded that a higher ZnO layer thickness leads to a lower mobility.

Figure 6(a) shows the transfer I_{ds}–V_g characteristics of amorphous multilayered ZnO-SnO_2 heterostructure TFTs with various SnO_2 layer thicknesses for a fixed ZnO layer thickness (1.5 nm). As shown in Fig. 6(a), the I_{on}/I_{off} ratio derived from the transfer curve for a V_d of 15 V was as high as approximately 10^{10} for all transistors. The turn-on voltage (V_{on}) was in the range of 0 V to –1 V except for the ZnO(1.5 nm)-SnO_2(2.5 nm) and ZnO(1.5 nm)-SnO_2(3.0 nm) transistors, which were largely negatively shifted (–4.8 V and –9.2 V, respectively), dependent on the thickness of the SnO_2 layer, and shifted toward to the negative voltage with an increase in the thickness of the SnO_2 layer. Generally, the V_{on} shift of oxide semiconducting TFTs can be explained by various factors, such as defects, carrier concentration, and charge trapping in oxide channel layers and interface between channel and gate dielectrics. The V_{on} shifts of TFTs with thicker SnO_2 layer are attributed to the increase in the carrier concentration with an increase in the thickness of the SnO_2 layer, which contributes to the channel conductivity. Figure 6(b) shows the extracted saturation mobility (μ_{sat}), subthreshold swing (ss), and threshold voltage (V_{th}) as a function of SnO_2 thickness for a fixed ZnO layer thickness (1.5 nm). The μ_{sat} increased to a peak value of 43 $cm^2/V \cdot s$ at ZnO(1.5 nm)-SnO_2(1.5 nm) TFTs, and then decreased at a higher thickness of the SnO_2 layer. The ss did not show a specific trend according to the thickness of the SnO_2 layer for a fixed ZnO layer thickness, and showed a value ranging from 0.12 V/dec. to 0.27 V/dec. for all transistors. However, the threshold voltage has a negative value for a high thickness of the SnO_2 layer (2.5 nm and 3.0 nm). The thickness of the SnO_2 layer in a ZnO-SnO_2 heterostructure channel significantly impacts on the performance parameters of the TFT, such as mobility and threshold voltage. Based on these results, it was concluded that a higher SnO_2 layer thickness leads to a lower mobility and a negative V_{th} shift.

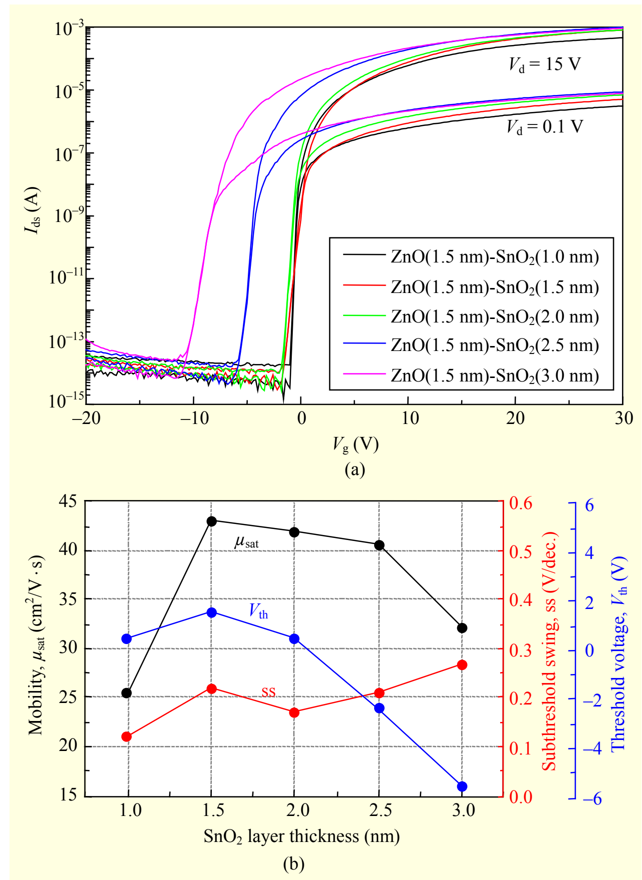

Fig. 6. (a) Transfer I_{ds}–V_g characteristics of amorphous multilayered ZnO-SnO_2 heterostructure TFTs with various SnO_2 layer thicknesses for fixed ZnO layer thickness (1.5 nm), and (b) performance parameters including saturation mobility (μ_{sat}), subthreshold swing (ss), and threshold voltage (V_{th}) of TFTs as function of SnO_2 layer thickness for 1.5 nm thick ZnO layer.

IV. Conclusion

In conclusion, amorphous multilayered ZnO-SnO_2 heterostructure thin films were produced using a pulsed laser ablation of ZnO and SnO_2 oxides targets, and their field-effect electronic transport properties were investigated as a function of the thickness of the ZnO and SnO_2 layers. The films have an amorphous multilayered heterostructure consisting of ZnO and SnO_2 layers. The thicknesses of the ZnO and SnO_2 layers have a significant impact on the electronic transport properties of the TFTs. Based on our observations, it was concluded that the mobility of the TFTs can be controlled by optimizing the

thickness of the ZnO and SnO_2 layers. The highest field-effect mobility of 43 $cm^2/V\cdot s$, a subthreshold swing of 0.22 V/dec., a threshold voltage of 1 V, and a drain current on-to-off ratio of 10^{10} were obtained for the amorphous multilayered ZnO (1.5 nm)-SnO_2(1.5 nm) heterostructure TFTs. These results reflect the fact that the high mobility of a TFT is attributed to a unique electronic structure owing to the advantageous combination of three ZnO, SnO_2, and ZnO-SnO_2 interface layers related to a high-mobility electron channel formed in a ZnO-SnO_2 heterostructure film. Our results suggest that an amorphous multilayered ZnO-SnO_2 heterostructure system as an oxide semiconductor can be a potential candidate for the fabrication of high-performance field-effect transistors. Future work is needed to investigate the proper device stability.

References

[1] K. Nomura et al., "Room-Temperature Fabrication of Transparent Flexible Thin-Film Transistors Using Amorphous Oxide Semiconductors," *Nature*, vol. 432, Nov. 2004, pp. 488–492.

[2] E. Fortunato et al., "Amorphous IZO TTFTs with Saturation Mobility Exceeding 100 $cm^2/V\cdot s$," *Physica Status Solidi (RRL)*, vol. 1, no. 1, Jan. 2007, pp. R34–R37.

[3] H.Q. Chiang et al., "High Mobility Transparent Thin-Film Transistors with Amorphous Zinc Tin Oxide Channel Layer," *Appl. Physics Lett.*, vol. 86, no. 1, 2005, pp. 013503-1–013503-3.

[4] J. Heo, S.B. Kim, and R.G. Gordon, "Atomic Layer Deposited Zinc Tin Oxide Channel for Amorophous Oxide Thin Film Transistors," *Appl. Physics Lett*, vol. 101, 2012, pp. 113507-1–113507-5.

[5] T. Kamiya, K. Nomura, and H. Sosono, "Present Status of Amorphous In-Ga-Zn-O Thin Film Transistors," *Sci. Technol. Adv. Mater.*, vol. 11, no. 4, Sept. 2010, pp. 044305-1–044305-23.

[6] W.S. Cheong, J. Park, and J.-H. Shin, "Effect of Oxygen Binding Energy on the Stability of Indium-Gallium-Zinc-Oxide Thin-Film Transistors," *ETRI J.*, vol. 34, no. 6, Dec. 2012, pp. 966–969.

[7] J.F. Wager, "Flat-Panel-Display Backplanes: LTPS or IGZO for AMLCDs or AMOLED Displays?" *Inf. Display*, vol. 30, no. 2, Mar. 2014, pp. 26–29.

[8] A. Ohtomo and H.Y. Hwang, "A High-Mobility Electron Gas at the $LaAlO_3/SrTiO_3$ Heterointerface," *Nature*, vol. 427, Jan. 2004, pp. 423–426.

[9] K. Koike et al., "Characteristics of a $Zn_{0.7}Mg_{0.3}O$/ZnO Heterostructure Field-Effect Transistor Grown on Sapphire Substrate by Molecular-Beam Epitaxy," *Appl. Physics Lett.*, vol. 87, no. 11, 2005, pp.112106-1–112106-3.

[10] H. Tampo et al., "Polarization-Induced Two-Dimensional Electron Gases in ZnMgO/ZnO Heterostructures," *Appl. Physics Lett.*, vol. 93, no. 20, 2008, pp. 202104-1–202104-3.

[11] M. Nakano et al., "Electronic-Field Control of Two-Dimensional Electrons in Polymer-Gated–Oxide Semiconductor Heterostructures," *Adv. Mater.*, vol. 22, no. 8, Apr. 2010, pp. 876–879.

[12] H.A. Chin et al., "Two-Dimensional Electron Gases in Polycrystalline MgZnO/ZnO Heterostructures Grown by rf-Sputtering Processes," *J. Appl. Physics*, vol. 108, no. 5, 2010, pp. 054503-1–054503-4.

[13] S.J. Lee et al., "Characterization of ZnO-SnO_2 Nanocomposite Thin Films Deposited by Pulsed Laser Ablation and their Field Effect Electronic Properties," *Mater. Lett.*, vol. 122, May 2014, pp. 94–97.

[14] W.B. Jackson, R.L. Hoffman, and G.S. Herman, "High-Performance Flexible Zinc Tin Oxide Field-Effect Transistors," *J. Appl. Physics Lett.*, vol. 87, 2005, pp. 193503-1–193503-3.

[15] M.G. McDowell, R.J. Sanderson, and I.G. Hill, "Combinational Study of Zinc Tin Oxide Thin-Film Transistors," *J. Appl. Physics Lett.*, vol. 92, 2008, pp. 013502-1–013502-3.

[16] D.W. Greve, "*Field Effect Devices and Application: Devices for Portable, Low Power, and Imaging Systems*," 1st ed. Englewood Cliffs, NJ, USA: Prentice-Hall, 1998.

[17] R. Martins et al., "Role of Order and Disorder on the Electronic Performance of Oxide Semiconductor Thin Film Transistors," *J. Appl. Physics*, vol. 101, no. 4, 2007, pp. 044505-1–044505-7.

[18] M.G. Yun et al., "Effects of Channel Thickness on Electrical Properties and Stability of Zinc Tin Oxide Thin-Film Transistors," *J. Physics D: Appl. Physics*, vol. 46, no. 47, Oct. 2013, pp. 475106-1–475106-5.

Su-Jae Lee received his BS degree in physics from Kyungsung University, Busan, Rep. of Korea, in 1986 and his MS and PhD degrees in physics from Pusan National University, Rep. of Korea, in 1988 and 1997, respectively. Since he joined ETRI in 1997, he has been involved in the development of ferroelectric thin-film/microwave tunable devices and oxide nanofiber electronics. His research interests include the development of new functional superlattice oxides, high mobility semiconducting oxides, and oxide TFTs for next-generation nano-oxide electronics and displays.

Chi-Sun Hwang received his BS degree from Seoul National University, Rep. of Korea, in 1991 and his PhD degree from the Korea Advanced Institute of Science and Technology, Daejeon, Rep. of Korea, in 1996, both in physics. From 1996 to 2000, he worked to make DRAM devices with 0.18 μm technology at Hyundai Semiconductor Inc., Incheon, Rep. of Korea. In the year 2000, he joined ETRI. Since then, his research has focused on display technology based on active-matrix flat-panel displays using TFTs, especially oxide TFTs. His recent research interests are environment adaptive displays, digital holography, and novel switching devices.

Jae-Eun Pi received his BS and MS degrees in electronic engineering from Konkuk University, Seoul, Rep. of Korea, in 2009 and 2011, respectively. In 2011, he joined the Smart I/O Control Device Research Section of ETRI. His main research interests include transparent and flexible electronics and the design of driving circuits for flat-panel and digital holographic displays.

Jong-Heon Yang received his BS degree in electrical engineering from the Korea Advanced Institute of Science And Technology, Daejeon, Rep. of Korea, in 2000 and his MS degree in electronic engineering from Pohang University of Science and Technology, Rep. of Korea, in 2002. He is currently a senior engineer with the Convergence Technology Research Division of ETRI.

Chun-Won Byun received his BS and MS degrees in electrical and computer engineering from Hanyang University, Seoul, Rep. of Korea, in 2002 and 2007, respectively. From 2007 to 2010, he worked for ETRI, and from 2011 to 2013, he worked for Samsung Display, Giheung, Rep. of Korea. Since 2013, he has returned to ETRI and is now working for their Smart I/O Control Device Research Section. His research interests include non-volatile memory devices and their applications; driving methods for new displays; and circuits for flat-panel displays.

Hye Yong Chu received her BS and MS degrees in physics from Kyung Hee University, Seoul, Rep. of Korea, in 1987 and 1989, respectively. She joined ETRI in 1989. She earned her PhD degree in information displays from Kyung-Hee University, in 2008. Her current research interests include novel device architectures in organic light-emitting devices and next-generation displays.

Kyoung-Ik Cho received his BS degree in materials science from the Ulsan Institute of Technology, Rep. of Korea, in 1979 and his MS and PhD degrees in material science and engineering from the Korea Advanced Institute of Science and Technology, Daejeon, Rep. of Korea, in 1981 and 1991, respectively. He joined ETRI in 1981. He has been working on the development of advanced display devices, and new electronic devices and materials. His current research interests include oxide TFTs and transparent displays; environment adaptable displays; and flexible electronic devices.

Sung Haeng Cho received his BS, MS, and PhD degrees from Seoul National University, Rep. of Korea, in 1996, 1998, and 2003, respectively, all in physical chemistry. From 2005 to 2012, he worked to develop LTPS TFTs on a Si backplane for gate driver integration and oxide semiconductor TFTs for large-sized high-resolution high-speed displays at Samsung Display, Giheung, Rep. of Korea. In 2012, he joined ETRI. His current research focusses on high-mobility and high-speed oxide TFT backplane technology for super high-resolution displays.

http://dx.doi.org/10.4218/etrij.15.0114.0743