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Single-Phase Multilevel PWM Inverter Based on H-bridge and its Harmonics Analysis

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Abstract

The efficient electric power demand management in electric power supply industry is currently being changed by distributed generation. Meanwhile, small-scale distributed generation systems using renewable energy are being constructed worldwide. Several small-scale renewable distributed generation systems, which can supply electricity to the grid at peak load of the grid as per policy such as demand response programs, could help in the stability of the electric power demand management. In this case, the power quality of the small-scale renewable distributed generation system is more significant. Low prices of power semiconductors and multilevel inverters with high power quality have been recently investigated. However, the conventional multilevel inverter topology is unsuitable for the small-scale renewable distributed generation system, because the number of devices of such topology increases with increasing output voltage level. In this paper, a single-phase multilevel inverter based on H-bridge, with DC_Link divided by bi-directional switches, is proposed. The proposed topology has almost half the number of devices of the conventional multilevel inverter topology when these inverters have the same output voltage level. Double Fourier series solution is mainly used when comparing PWM output harmonic components of various inverter topologies. Harmonic components of the proposed multilevel inverter, which have been analyzed by double Fourier series, are compared with those of the conventional multilevel inverter. An inverter prototype is then developed to verify the validity of the theoretical analysis.

Keywords: Double Fourier series, Multilevel inverter, Single-phase inverter, Single-phase multilevel inverter

I. INTRODUCTION

The demand for electricity has been increasing because of industrial structures acceleration as a result of economic development. An effort to reduce green-house gases caused by the climate change has also led to the development of renewable power industry, but such task has resulted in an increased cost. Accordingly, the electric power industry is focusing on saving through efficiency and quality improvement.

The operating philosophy of the electricity supply industry has been changing from the unilateral supply way, with respect to the entire demand, to the demand management. Distributed generation is very important to conduct efficient demand management. If renewable power system exists as small-scale distributed generation universally, then such system is advantageous in terms of the stability of electricity. In this case, the power quality of small-scale renewable distributed generation system is much significant [1]-[3]. A few advantages of the multilevel inverter include high-quality generated output voltage waveform, reduced dv/dt stress, low electro-magnet compatibility, and improved system efficiency. As a result, several researchers have studied the multilevel inverter for the small-scale renewable distributed generation system [4]-[6].

Residential electricity consumption in leading contries has reached approximately 30% of the total electricity consumption. Households installed with a renewable generation system have increased drastically. In terms of demand management, distribution generation system is proposed to have an increased power capacity and an energy storage mean. Moreover, many distributed generation systems would frequently supply electricity to the grid at peak load of the grid as per policy to help with the stable electric power demand management [1]-[3]. Therefore, applying multilevel inverter is necessary to improve power quality. A company recently launched a five-level inverter in

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the market. However, research on single-phase multilevel inverter is few compared with that on multilevel inverter of middle power capacity [4], [7], [8].

This paper proposes a single-phase multilevel inverter topology based on H-bridge. A proposed topology based on H-bridge uses bi-directional switches that divide the DC_Link into infinite numbers. The advantage of this topology includes having a number of devices lower than that of devices of a conventional multilevel inverter, but having the same quality of output voltage waveforms. In this paper, the proposed inverter topology is compared with that of the conventional multilevel inverters. The proposed inverter is also verified the performance of an output voltage waveform through analysis using the double Fourier series.

II. MULTILEVEL INVERTER

Conventional multilevel inverter topology mainly includes diode clamped multilevel inverter, flying capacitor multilevel inverter, and H-bridge multilevel inverter. To mainly use high voltage of middle power capacity, the topologies contain the switch groups. The switch groups, which are proportional to the number of the output voltage level, connect with each other in a series. Thus, each switch group has a reduced voltage as much as the number of series connection of the switch groups. However, as single-phase multilevel inverter topology is usually used in low in-output voltage application, research of this topology has been performed to lower cost by reducing the number of devices rather than reducing the collector-emitter voltage of the switch. The single-phase multilevel topology could be categorized as based on two types of basic structures, namely, H-bridge and half-bridge. Commercialized low-voltage multilevel inverter based on half-bridge is known as five-level inverter, as shown in Fig. 1 (a). Conventional five-level diode clamped inverter is depicted in Fig. 1 (b) [4]-[6].

Multilevel inverter topology mostly uses an LS-PWM scheme to generate the output voltage waveform. The LS-PWM scheme has one less carrier waveforms than the number of the output voltage level, and the carrier waveforms are arranged between each output voltage level. Each carrier signal of the LS-PWM scheme could promote phase shift between neighboring carrier signals. These phase shift techniques could be PD, POD, and APOD. Fig. 2 shows PD, POD, and APOD. Each of the output voltage waveforms by PD, POD, and APOD has different total harmonic components [6].

Output voltage waveform of inverter is represented as the synthesis of square waveforms. A square waveform can be described as an infinite series of harmonic components by the Fourier analysis. In the double Fourier series, a point of a reference waveform of the LS-PWM can be corresponding to a square waveform, which appears about a reference

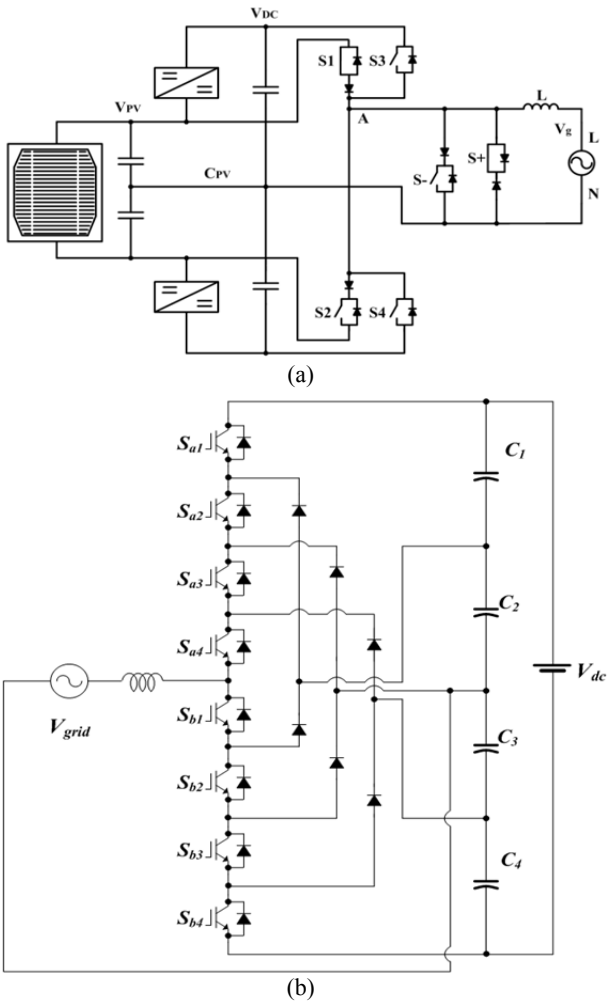


Fig. 1. Conventional Single-Phase multilevel inverter topologies. (a) Commercialized five-level inverter. (b) Five-level diode clamped inverter.

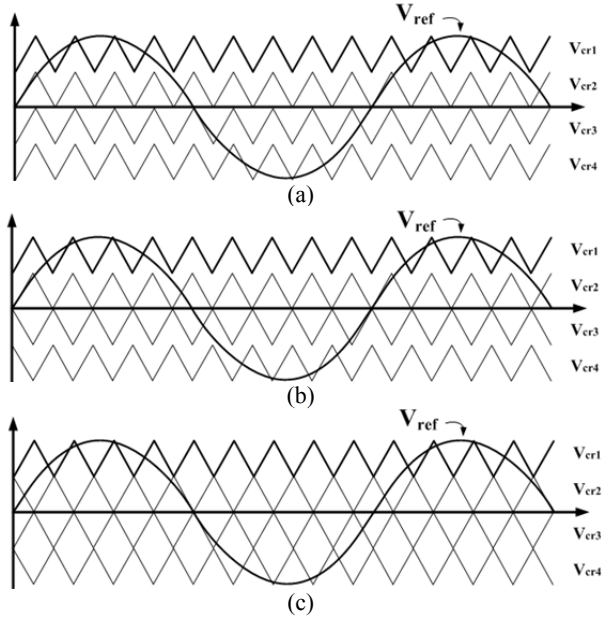


Fig. 2. Reference waveform and carrier waveforms of LS-PWM scheme.(a) PD, (b) POD, (c) APOD.

waveform periodically. Thus, the output voltage waveform represents the total harmonic components in Equation (1). The first line defines the DC components, the fundamental component, and baseband harmonic components. This baseband harmonic components are integer multiples of the fundamental component. The second line defines carrier harmonic components as multiples of the modulation frequency. The third line defines sideband harmonic components displaced on either side of the main carrier harmonics by integer multiples of the fundamental frequency component. The coefficient of Equation (1) is determined by Equation (2). As the double Fourier series analysis exactly identifies the harmonic components of a PWM waveform, this method has been mostly used when comparing the output voltage waveform of various topologies [9]-[13].

$$\begin{aligned} f(t) &= \frac{A_{00}}{2} + \sum_{n=1}^{\infty}\{A_{0n}\cos(n\omega_o t) + B_{0n}\sin(n\omega_o t)\} \\ &+ \sum_{m=1}^{\infty}\{A_{m0}\cos(m\omega_c t) + B_{m0}\sin(m\omega_c t)\} \\ &+ \sum_{m=1}^{\infty}\sum_{n=-\infty,n\neq 0}^{\infty}\{A_{mn}\cos(m\omega_c t + n\omega_o t) + B_{mn}\sin(m\omega_c t + n\omega_o t)\} \end{aligned} \tag{1}$$

$$A_{mn} + jB_{mn} = \frac{1}{2\pi^2}\int_{-\pi}^{\pi}\int_{-\pi}^{\pi} f(x,y)e^{j(mx+ny)}dxdy \quad \text{where } x = \omega_c t,\ y = \omega_o t. \tag{2}$$

III. Proposed Topology

Fig. 3 shows the proposed single-phase multilevel inverter topology. The proposed single-phase multilevel inverter based on H-bridge uses bi-directional switches, which split the DC_Link into as much as the number of the bi-directional switch. The divided DC_Link determines the number of level of the output voltage waveform. The B-arm of the proposed inverter is a series connection of the two switches. The output ports of A-arm and B-arm are connected by a bi-directional switch, and this topology has two capacitor voltage sources in the upper and lower sections of both arms. Maximum output voltage of the inverter is obtained by Equation (3), given the capacitor voltage sources between the arms. The modulation ratio is given by Equation (4).

$$V_{MAX} = (p-1)\cdot V_C \tag{3}$$

$$M = \frac{V_{ref_{peak}}}{V_{MAX}} \tag{4}$$

Equation (5) shows the collector-to-emitter voltage rating of S1 and S2 on the A-arm. Equation (6) is the collector-to-emitter voltage rating of all bi-directional switches in A-arm. The collector-to-emitter voltage rating of S3 and S4 in the B-arm is $p \cdot V_C$.

$$V_{S_n} = (p-2)\cdot V_C \tag{5}$$

$$V_{Q_x} = \left(\left|x - \left\lceil\frac{p}{2}-1\right\rceil\right| + \left\lceil\frac{p}{2}-1\right\rceil\right)\cdot V_C \quad x = 1\cdots\cdots p-3 \tag{6}$$

The proposed n-level inverter has k, the number of switches, and p, the number of capacitor voltage sources, as shown in Equations (7) and (8).

$$k = n+1 \tag{7}$$

$$p = \frac{n+1}{2} \tag{8}$$

The comparison results are given in Table I (this table is

$$\begin{aligned} v_{an} &= \frac{V_c}{\pi}\left[6\sin\psi + M\{\pi - 6\psi - 3\sin 2\psi\}\right]\cos\omega_o t \\ &+ \frac{V_c}{\pi}\sum_{n=1}^{\infty}\left[\frac{6\sin(2n+1)\psi}{2n+1} - 3M\left\{\frac{\sin 2(n+1)\psi}{n+1} + \frac{\sin 2n\psi}{n}\right\}\right]\cos(2n+1)\omega_o t \\ &+ \frac{4V_c}{\pi^2}\sum_{m=1}^{\infty}\left[\frac{A_{m_{odd}0}}{2m-1}\cos(2m-1)\omega_c t\right] + \frac{2V_c}{\pi^2}\sum_{m=1}^{\infty}\sum_{\substack{n=-\infty \\ n\neq 0}}^{\infty}\left[\frac{A_{m_{odd}n_{even}}}{2m-1}\cos\left((2m-1)\omega_c t + 2n\omega_o t\right)\right] \\ &+ \frac{V_c}{\pi^2}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\left[\frac{1}{2m}\left\{\cos n\pi\cdot \mathrm{J}_{2n+1}[4m\pi M]\left\{\pi - 6\psi - \frac{3\sin 2(2n+1)\psi}{2n+1}\right\} + 3A_{m_{even}n_{odd}}\right\}\right]\cos\left(2m\omega_c t + (2n+1)\omega_o t\right) \end{aligned} \tag{7a}$$

$$\text{where} \quad \psi = \cos^{-1}\left(\frac{1}{2M}\right)$$

$$A_{m_{odd}0} = \sum_{k=1}^{\infty}\left[\frac{1}{2k-1}\mathrm{J}_{2k-1}[(2m-1)2\pi M]\{1 + 3\cos k\pi\sin(2k-1)\psi\}\right] \tag{7b}$$

$$A_{m_{odd}n_{even}} = \sum_{k=1}^{\infty}\left[\mathrm{J}_{2k-1}[(2m-1)2\pi M]\left\{\frac{\cos n\pi + 3\cos k\pi\sin(2n+2k-1)\psi}{2n+2k-1} + \frac{\cos n\pi + 3\cos k\pi\sin(2k-1-2n)\psi}{2k-1-2n}\right\}\right] \tag{7c}$$

$$A_{m_{even}n_{odd}} = \sum_{k=1}^{\infty}\left[\cos k\pi\cdot \mathrm{J}_{2k-1}[4m\pi M]\left\{\frac{\sin 2(n+k)\psi}{n+k} + \frac{\sin 2(n-k+1)\psi}{n-k+1}\right\}\right] \tag{7d}$$

TABLE I
COMPARISON OF COMPONENT REQUIREMENT

Converter Type	Proposed Inverter	Diode Clamp	Flying Capacitors	Cascaded Inverter
Main switching devices	(n+1)	(n-1)x2	(n-1)x2	(n-1)x2
Main diodes	(n+1)	(n-1)x2	(n-1)x2	(n-1)x2
Clamping diodes	0	(n-1)x(n-2)	0	0
Dc bus capacitors	(n+1)/2	(n-1)	(n-1)	(n-1)/2
Balancing capacitors	0	0	(n-1)x(n-2)/2	0

$$
\begin{aligned}
v_{bn} &= \frac{V_c}{\pi}\left[6\sin\psi + M\left\{3\pi - 6\psi - 3\sin 2\psi\right\}\right]\cos\omega_o t \\
&+ \frac{V_c}{\pi}\sum_{n=1}^{\infty}\left[\frac{6\sin(2n+1)\psi}{2n+1} - 3M\left\{\frac{\sin 2(n+1)\psi}{n+1} + \frac{\sin 2n\psi}{n}\right\}\right]\cos(2n+1)\omega_o t \\
&+ \frac{12V_c}{\pi^2}\sum_{m=1}^{\infty}\left\{\frac{A_{m_{odd}0}}{2m-1}\cos(2m-1)\omega_c t\right\} + \frac{6V_c}{\pi^2}\sum_{m=1}^{\infty}\sum_{\substack{n=-\infty \\ n\neq 0}}^{\infty}\left\{\frac{A_{m_{odd}n_{even}}}{2m-1}\right\}\cos\left((2m-1)\omega_c t + 2n\omega_o t\right) \\
&+ \frac{3V_c}{\pi^2}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\left[\frac{1}{2m}\left\{\cos n\pi\cdot \mathrm{J}_{2n+1}\left[4m\pi M\right]\left\{\pi - 2\psi - \frac{\sin 2(2n+1)\psi}{2n+1}\right\} + A_{m_{even}n_{odd}}\right\}\right]\cos\left(2m\omega_c t + (2n+1)\omega_o t\right)
\end{aligned}
\tag{8a}
$$

$$
A_{m_{odd}0} = \sum_{k=1}^{\infty}\left[\frac{1}{2k-1}\mathrm{J}_{2k-1}\left[(2m-1)2\pi M\right]\left\{1 + \cos k\pi\sin(2k-1)\psi\right\}\right] \tag{8b}
$$

$$
A_{m_{odd}n_{even}}\sum_{k=1}^{\infty}\left[\mathrm{J}_{2k-1}\left[(2m-1)2\pi M\right]\left\{\frac{\cos n\pi + \cos k\pi\sin(2n+2k-1)\psi}{2n+2k-1} + \frac{\cos n\pi + \cos k\pi\sin(2k-1-2n)\psi}{2k-1-2n}\right\}\right] \tag{8c}
$$

$$
A_{m_{even}n_{odd}} = \sum_{\substack{k=1 \\ k\neq -n, k\neq n+1}}^{\infty}\left[\cos k\pi\cdot \mathrm{J}_{2k-1}\left[4m\pi M\right]\left\{\frac{\sin 2(n+k)\psi}{n+k} + \frac{\sin 2(n-k+1)\psi}{n-k+1}\right\}\right] \tag{8d}
$$

$$
\begin{aligned}
v_{az}(t) &= 2V_c M\cos(\omega_o t) \\
&+ \frac{8V_c}{\pi^2}\sum_{m=1}^{\infty}\frac{1}{2m-1}\sum_{k=1}^{\infty}\frac{1}{2k-1}J_{2k-1}\left[(2m-1)2\pi M\right]\left\{1 + 2\sin\left(\left[2k-1\right]\psi\right)\cos k\pi\right\}\cos(2m-1)\omega_c t \\
&+ \frac{2V_c}{\pi}\sum_{m=1}^{\infty}\frac{1}{2m}\sum_{n=-\infty}^{\infty}J_{2n+1}\left[4m\pi M\right]\cos n\pi\cos\left(2m\omega_c t + (2n+1)\omega_o t\right) \\
&+ \frac{4V_c}{\pi^2}\sum_{m=1}^{\infty}\frac{1}{2m-1}\sum_{\substack{n=-\infty \\ (n\neq 0)}}^{\infty}\sum_{k=1}^{\infty}\left[J_{2k-1}\left(\left[2m-1\right]2\pi M\right)\left[\frac{\cos n\pi + 2\cos k\pi\sin\left(\left[2k-1-2n\right]\psi\right)}{\left[2k-1-2n\right]}\right.\right. \\
&\qquad\left.\left. + \frac{\cos n\pi + 2\cos k\pi\sin\left(\left[2k-1+2n\right]\psi\right)}{\left[2k-1+2n\right]}\right]\right]\cos\left(\left[2m-1\right]\omega_c t + 2n\omega_o t\right)
\end{aligned}
\tag{9}
$$

$$
\begin{aligned}
v_{ab} &= 2MV_c\cos\omega_o t \\
&+ \frac{8V_c}{\pi^2}\sum_{m=1}^{\infty}\frac{1}{2m-1}\sum_{k=1}^{\infty}\frac{1}{2k-1}\mathrm{J}_{2k-1}\left[(2m-1)2\pi M\right]\cos(2m-1)\omega_c t \\
&+ \frac{2V_c}{\pi}\sum_{m=1}^{\infty}\frac{1}{2m}\sum_{n=-\infty}^{\infty}\mathrm{J}_{2n+1}\left[4m\pi M\right]\cos n\pi\cos\left(2m\omega_c t + (2n+1)\omega_o t\right) \\
&+ \frac{4V_c}{\pi^2}\sum_{m=1}^{\infty}\frac{1}{2m-1}\sum_{n=-\infty, n\neq 0}^{\infty}\sum_{k=1}^{\infty}J_{2k-1}\left[(2m-1)2\pi M\right]\left\{\frac{\cos n\pi}{2k-1-2n} + \frac{\cos n\pi}{2k-1+2n}\right\}\cos\left((2m-1)\omega_c t + 2n\omega_o t\right)
\end{aligned}
\tag{10}
$$

TABLE II
SWITCHING FUNCTION OF THE FIVE-LEVEL SINGLE-PHASE PWM INVERTER

$f(x,y)$	Phase A	
	When $-\pi \le x \le 0$	When $0 < x \le \pi$
$\frac{V_C}{2}$	$M\cos y < -\frac{1}{2}\left(1-\frac{x}{2\pi}\right)$	$M\cos y < -\frac{1}{2}\left(1+\frac{x}{2\pi}\right)$
$-\frac{V_C}{2}$	$-\frac{1}{2}\left(1-\frac{x}{2\pi}\right) < M\cos y < -\frac{1}{2}\left(1+\frac{x}{\pi}\right)$	$-\frac{1}{2}\left(1+\frac{x}{\pi}\right) < M\cos y < -\frac{1}{2}\left(1-\frac{x}{\pi}\right)$
High Imp.	$-\frac{1}{2}\left(1+\frac{x}{\pi}\right) < M\cos y < -\frac{x}{2\pi}$	$-\frac{1}{2}\left(1-\frac{x}{\pi}\right) < M\cos y < \frac{x}{2\pi}$
$\frac{V_C}{2}$	$-\frac{x}{2\pi} < M\cos y < 1+\frac{x}{2\pi}$	$\frac{x}{2\pi} < M\cos y < 1-\frac{x}{2\pi}$
$-\frac{V_C}{2}$	$1+\frac{x}{2\pi} < M\cos y$	$1-\frac{x}{2\pi} < M\cos y$
$f(x,y)$	Phase B	
	When $-\pi \le x \le 0$	When $0 < x \le \pi$
$-\frac{3V_C}{2}$	$M\cos y < -\frac{1}{2}\left(1+\frac{x}{\pi}\right)$	$M\cos y < -\frac{1}{2}\left(1-\frac{x}{\pi}\right)$
High Imp.	$-\frac{1}{2}\left(1+\frac{x}{\pi}\right) < M\cos y < -\frac{x}{2\pi}$	$-\frac{1}{2}\left(1-\frac{x}{\pi}\right) < M\cos y < \frac{x}{2\pi}$
$\frac{3V_C}{2}$	$-\frac{x}{2\pi} < M\cos y$	$\frac{x}{2\pi} < M\cos y$

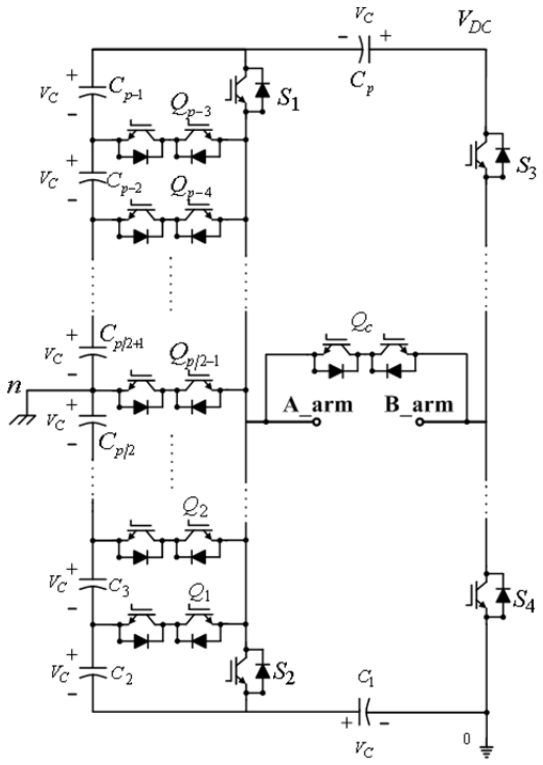


Fig. 3.Proposed single-phase multilevel inverter topology.

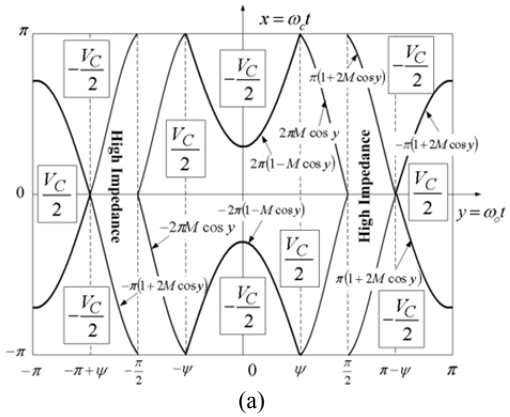
shown at the top of the next page). The number of devices of conventional multilevel inverters and that of the proposed multilevel inverter are also shown in Table I. The proposed inverter has about half of the switches and diodes of the other inverters. The number of DC bus capacitors of the proposed inverter and that of the cascaded multilevel inverter have about twice less than the other inverters.

IV. HARMONIC ANALYSIS OF THE PROPOSED FIVE-LEVEL INVERTER

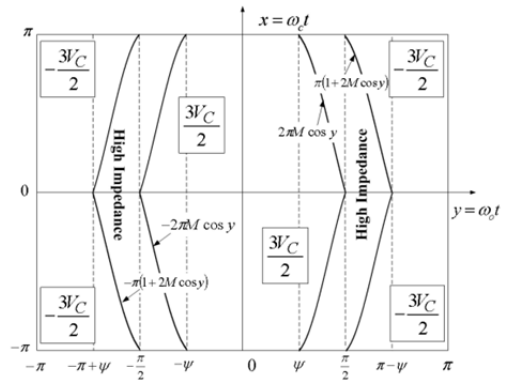
In this section, the switching function of the proposed single-phase five-level inverter is presented in Table II. Fig. 4 shows the reference waveforms in axis of the two time variables (x, y). This figure also shows the harmonic components of the proposed inverter, which are analyzed by the double Fourier series and simulated using MATLAB software. These harmonic components are compared with those of the conventional five-level diode clamped inverter and weighted total harmonic distortion (WTHD) [8].

A. Proposed Single-Phase Five-Level Inverter

In Table II, x is $\omega_C t$ and y is $\omega_O t$. Fig. 4 shows the reference waveforms of A-arm and B-arm for each period of x-axis and y-axis, but carrier waveforms are omitted. A reference waveform is a $2M\cos y$ at the five-level. M is the modulation index. A period reference waveform is all represented at the unit Cartesian coordinate system of Fig. 4. Meanwhile, the reference waveforms are represented symmetrically according to the y-axis along the x-axis infinitely. Table II also shows the output voltage magnitude about the range of the reference waveform at the Cartesian coordinate system.



(a)



(b)

Fig. 4. PWM contour plot of f(x, y) for the proposed five-level inverter. (a) A-arm, (b) B-arm.

Equations (7) and (8) are used to obtain the output voltage harmonic components of the proposed five-level inverter by the double Fourier series. In Equations (7a) and (8a), the first line defines the fundamental component. The second line defines baseband harmonic components. The third line and Equations (7b), (7c), (8b), and (8c) define carrier harmonic components as multiples of the modulation frequency and odd carrier/even fundamental harmonic components. The fourth line and Equations (7d) and (8d) define even carrier/odd fundamental sideband harmonic components. The fundamental component of the proposed inverter is 2*M*cos*y* according to the difference between Equations (7) and (8), and its baseband harmonic component is 0. Other harmonic components have significantly diminished as a result of the difference.

B. Comparison between the Proposed Inverter and Conventional Inverter

Equations (9) and (10) define total harmonic components of the five-level output voltage of the conventional diode clamped inverter and the proposed inverter. Equations (9) and (10) each show the same magnitude of the fundamental component and even carrier/odd fundamental sideband harmonic components. The carrier harmonic components of Equation (9) are also largely represented as much as possible

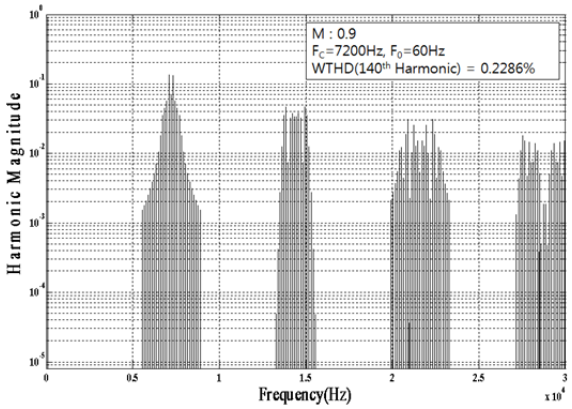


Fig. 5. Harmonic components of output voltage for the proposed inverter.

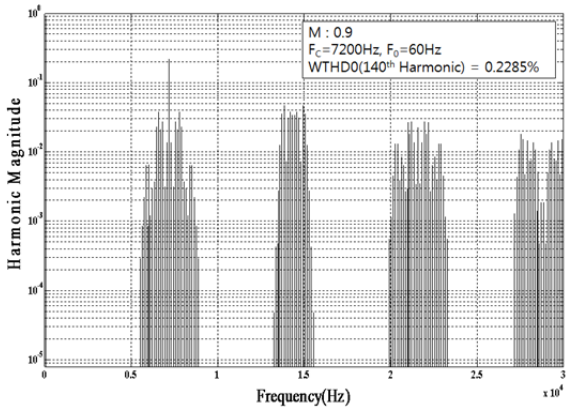


Fig. 6. Harmonic components of output voltage for the conventional diode clamped inverter.

to multiply the carrier harmonic components of Equation (10) by Equation (11). Equation (12) is the difference between the odd carrier/even fundamental sideband harmonic components of Equations (9) and (10). Equation (12) owing to *k*, at 1 or 2 or 3, has the value of approximate different sign when the *n* of the Bessel Function, $\boldsymbol{J}_n$, has 1 or 3 or 5. Therefore, the odd carrier/even fundamental sideband harmonic components of Equation (9) has been influenced by *k* summation term ($\sum$) of its fourth line with the result of Equation (12). Figs. 5 and 6 show the simulation results using MATLAB software. In Figs. 5 and 6, the odd carrier/2nd, 4th fundamental sideband harmonic components of the diode clamped inverter are lower than the harmonic components of the proposed inverter. However, the 1st and 3rd carrier harmonic components of the proposed inverter are much lower than the harmonic components of the diode clamped inverter. The WTHD of output voltage waveform of the two inverters are both about 0.229%, and are obtained by Equation (13).

$$\left\{1+2\sin\left(2k-1\right)\cos k\pi\right\} \tag{11}$$

$$\frac{2\cos k\pi\sin\left(2k-1-2n\right)\psi}{2k-1-2n}+\frac{2\cos k\pi\sin\left(2k-1+2n\right)\psi}{2k-1+2n} \tag{12}$$

$$\text{WTHD}=\sqrt{\sum_{n=2}^{\infty}\frac{1}{n^2}\left(\frac{V_n}{V_1}\right)^2}\,,\quad V_n:\text{RMS Value} \tag{13}$$

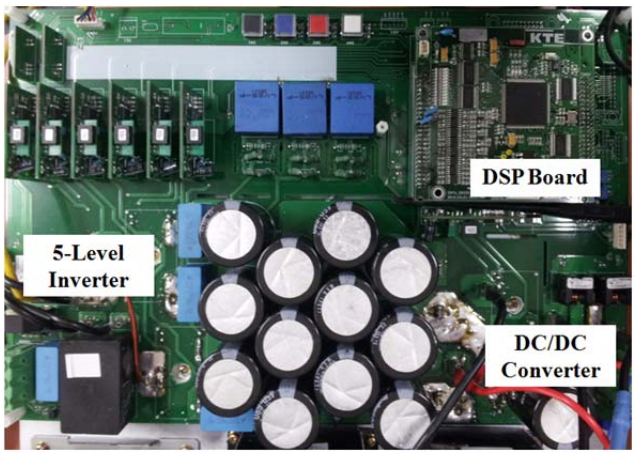
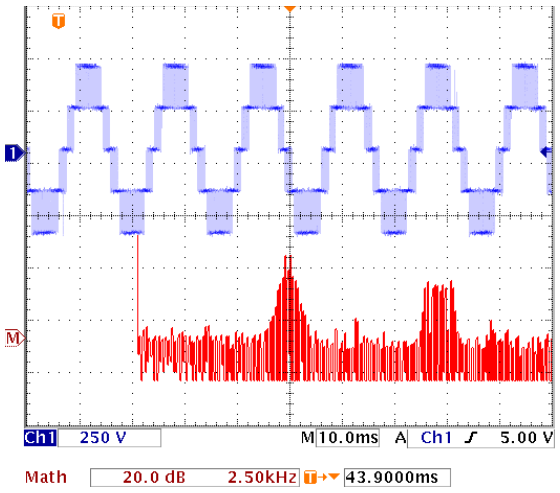
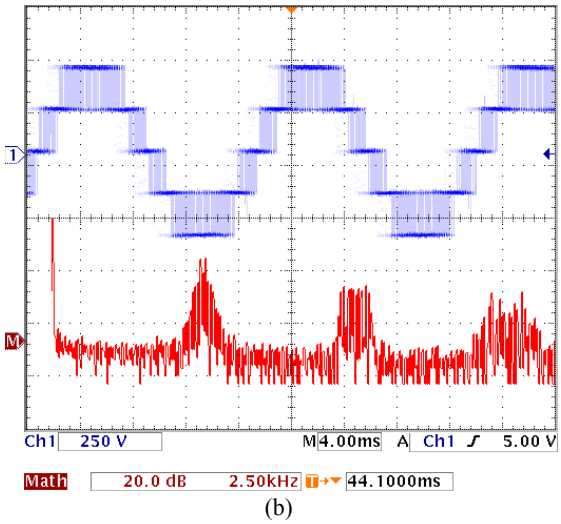


Fig. 7. Proposed five-level single-phase inverter prototype.



(a)



(b)

Fig. 8. Output voltage waveform and frequency spectrum of the proposed inverter. (a) Time/Div: 10ms, (b) Time/Div: 4ms.

V. Experimental Results

Fig. 7 shows the proposed single-phase five-level inverter prototype. To verify this topology, a 3kWp prototype has been constructed, and then used for experiment. Unidirectional switch of the prototype applied SK75GB12T4 IGBT module designed by SEMIKRON. The prototype also applied a SK80GM063 IGBT bi-directional switch module in between both arms. The TMS320F28335 DSP designed by TI is applied on the main controller.

TABLE III
Experimental Condition

Modulation Ratio	0.9
Carrier Frequency	7.2kHz
Fundamental Frequency	60Hz

Table III shows the experimental condition. Fig. 8 shows the output voltage waveform and the frequency spectrum of the proposed inverter.

VI. Conclusion

This paper proposed a single-phase multilevel inverter based on H-bridge that has the infinite output voltage level in accordance with divided DC_Link. This DC_Link was divided infinitely by bi-directional switches. The proposed topology has almost half the number of each device, switch, and diode and DC bus capacitor of the conventional multilevel inverters when these inverters have the same output voltage level.

As a double Fourier series exactly identifies the harmonic components of a PWM waveform, this method is mainly used when comparing various PWM strategies. Thus, in this paper, the output voltage harmonic components of the proposed inverter have been analyzed by double Fourier series, and then compared with those of the conventional diode clamped inverter. These results are also represented as frequency spectrum by using MATLAB software. As a result, the proposed inverter topology and the conventional inverter topology ensure that these output PWM waveforms have the same WTHD performance, when the proposed topology has almost half the number of switch and diode and DC bus capacitor of the conventional diode clamped inverter.

Finally, an inverter prototype is developed to verify the validity of the theoretical analysis result. The experimental result has been compared with the simulation result of the proposed inverter topology. This comparison confirms that both experimental and simulation results showed the same frequency spectrum.

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